Robust FinFET SRAM design based on dynamic back-gate voltage adjustment

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ABSTRACT

In this paper, we propose a robust SRAM design which is based on FinFETs. The design is performed by dynamically adjusting the back-gate voltages of pull-up transistors. For the write operation, we use an extra write driver which sets the desired back-gate voltages during this operation. This approach considerably increases the write margin. During the hold state, the back-gates are precharged to the supply voltage using an extra precharge circuit. This decreases the static power. Finally, we use nMOS switches to provide the optimum back-gate voltages during the read state. To minimize the area and power overheads, an instance of the circuitry is used for each column. The performance of the proposed technique is assessed using mixed mode device/circuit simulations for a physical gate length of 22 nm. The results show that the minimum operating voltage for six-sigma read and write yield is about 0.15 V lower than that of the recently proposed structures. In addition, the suggested SRAM shows significantly higher write margin and lower static power compared to the recently proposed structures. The minimum operating voltage of our proposed structure can be lowered down to 0.5 V through some work function tunings to balance the read and write stability. This minimum voltage is 0.1 V lower than the minimum operating voltage of the other structures with similar work function tunings.

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1. Introduction

To maximize the density, SRAM cells are realized using minimum sized transistors in each technology [1]. On the other hand, the shrinkage of the technology feature size to nano-scale regime has adversely impacted the SRAM yield due to uncertainty in the device parameters induced by process variations. In addition, in this regime, short channel effects more severely deteriorate the performance of the SRAM cells. To overcome these problems, new device structures may be invoked. Among them, double gate transistors have superior short channel characteristics and better immunity to process variations when compared to conventional bulk CMOS transistors. These originate from the use of a thin silicon film, lightly doped channel, and two gates for a better channel control [2]. Among double gate transistors, FinFET structure is one of the promising devices thanks to similarity of its fabrication process to that of the planar bulk CMOS [3]. Two gates of FinFET can be tied together or used independently. The independent use of gates offers dynamic or static performance tunability yielding a great flexibility for designers [4]. With a clever configuration, independent-gate structure may be used to merge series or parallel transistors in the logic reducing the number of transistors improving some of the characteristics (please see e.g., [5,6]). For example, in Ref. [5], the proposed gates with independent-gate implementations have lower input capacitance, number of Fins, and power consumption when compared to conventional tied-gate implementations while achieving about the same performance. In addition, recent advances in the manufacturing process permit the selective cut of the upper part of the gate allowing the implementation of both independent-gate and tied-gate double gate FinFETs on the same die [7]. This feature can also be utilized for the performance improvement of SRAM cells based on FinFETs. These improvements include both stability and static power improvement. In Ref. [8], the authors proposed connecting the back-gate of access transistors to the adjacent bit-cell storage nodes. Using this technique, the access transistor corresponding to the node storing “0” (“1”) becomes weak (strong) during the read (write) operation and the cell stability is increased using the built-in feedback [8]. In Ref. [9], a write wordline connected to the back-gate of pull-up transistors was used to weaken the transistors during the write operation, improving the write margin. In Ref. [10], an approach for finding the static back-gate voltages which maximize
the yield has been proposed. The fixed back-gate voltages were obtained for read, write, and hold modes of SRAM operation. Finally, the use of back-gate voltage for the leakage reduction has been proposed in Ref. [11]. It should be noted that the successful fabrication of FinFET SRAM cells using both independent and tied-gate devices has been reported in Ref. [12].

In this work, we propose the use of back-gates of pull-up transistors to enhance the stability of a SRAM cell. The voltages of these back-gates are determined such that the read and write stabilities are maximized and the static power is minimized. We also propose a circuit for the dynamic biasing of the pull-up transistors. To minimize the area overhead, the circuit for generating the dynamic voltages is shared among all the cells in a column. The contributions of this paper are as follows:

- Proposing a new dynamic back-gate biasing for improving SRAM cell performance metrics in double gate FinFET technology.
- Presenting a comparative analysis of the read SNM, read current, write margin and standby power of the proposed design versus the schemes in Refs. [8,9], and demonstrating significant improvements in write margin and standby power while maintaining competitive read SNM and read current.
- Providing a comparative analysis of process variation sensitivity of the proposed scheme versus the recently proposed schemes, proving significantly enhanced write margin yield and a competitive and satisfactory read SNM yield enabling us to lower the minimum operating voltage.

The rest of this paper is organized as follows. The FinFET structure is described in Section 2. In Section 3, the SRAM design considerations are reviewed. Section 4 discusses the existing dynamic back-gate voltage schemes while Section 5 describes the proposed dynamic back-gate voltage technique. The results are discussed in Section 6 while Section 7 concludes the paper.

2. FinFET structure

In FinFET devices, the gates on either side of the fin can be tied together or electrically isolated to allow an independent biasing scheme. This is achieved by removing the gate material in the region directly on top of the fin [7,13]. In the tied-gate operating mode (Fig. 1a), the two gates are biased together while in the independent-gate operating mode (Fig. 1b), they are biased independently.

We use a 22 nm FinFET technology with device parameters similar to those used in Ref. [9]. The parameters are listed in Table 1. The terminal contact resistances, which were included in the simulations, were calculated based on the model presented in Ref. [14]. In this paper, the results were obtained using 2D Sentaurus Device Simulator [15] with the temperature $T = 300 \text{ K}$. In the simulations, the density gradient model along with high field saturation for transport was used. The mobilities were calibrated using the experimental data given in Ref. [16].

The results of the $I$–$V$ characteristics obtained from these simulations were in good agreement with the results reported in Ref. [9]. Also, it should be noted that, in (100) wafers, for typical channel orientation of (110), the difference between the electron and hole mobilities decreases compared to that of the conventional bulk case. Thus, the midgap work function of 4.6 eV for both nFET and pFET results in comparable strengths for both nFET and pFET. Using this work function for both n- and p-type transistors with equal sizes, the threshold voltage of about 0.4 V was obtained for both devices (results of device simulations). The strength ratio of pFET–nFET was also obtained to be about 0.75. One also should notice that the use of the high aspect ratio for the FinFETs makes the midgap orientation of (110), the difference between the electron and hole mobilities decreases compared to that of the conventional bulk case. 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3. SRAM design considerations

In this section, we describe different operational modes of the conventional 6T SRAM cell shown in Fig. 2 along with the desired back-gate voltage of the transistors.

3.1. Read state

Consider the case that $V_L = 1$” and $VR = 0$” (see Fig. 2). During the read operation, bitlines are precharged to $V_{dd}$ and the wordline is set to $V_{ad}$. This operation raises $VR$ to a value that is determined by the voltage division between NR and AR. This voltage is denoted by $V_{read}$. If $V_{read}$ becomes greater than the trip point voltage of $PL$ and $NL$ ($V_{trip}$), the value of the cell flips and a destructive read occurs. The stability in the read state is measured by the read static noise margin (SNM) [18].

To increase the read SNM, $NR$ should be stronger than $AR$ in order to decrease $V_{read}$. Also, the leakage current of $PR$ which is in the OFF state may increase the $V_{read}$ value decreasing the read...
stability. To minimize the leakage, the absolute value of the threshold voltage of PR should be high. On the other hand, PL and AL should be stronger than NL to increase $V_{\text{trip}}$. Based on this discussion, the desired back-gate voltages of the transistors from the read stability perspective are $V_{\text{dd}}$, 0, $V_{\text{dd}}$, and 0 for NR, AR, PR, PL, AL, and NL, respectively. It is worth noting that, in addition to $V_{\text{trip}}$ and $V_{\text{read}}$, the gain of the inverter transfer characteristics also impacts the read SNM (higher gains would result in higher read SNMs) [18].

Another parameter in the read state is the access time for which the read current is used as a metric [9]. The read current is the current of the access transistor (AR) whose source is at $V_{\text{read}}$. From this aspect, if NR and AR become strong and PR becomes weak, the read current increases decreasing the access time [10]. While this parameter is not included in our optimization in favor of the read stability, it will be included in our comparative study.

3.2. Write state

While writing a “1” into the cell that stores “0” (Fig. 2), the voltage of BL is set to 0 and that of BR is set to $V_{\text{dd}}$, and the wordline is asserted. In this case, the node L is discharged through AL. If VL, which is determined by the voltage division between PL and AL, becomes lower than the trip point voltage of PR and NR, the write operation will be accomplished. The stability in the write state is measured by the write margin [19]. To increase the write margin, AL should be stronger than PL and $V_{\text{trip}}$ of PR–NR should be high. Hence, PR and AR should be stronger than NR. Also, the leakage current of NL which is in the OFF state may help the discharge of the node L increasing the write margin. To maximize the leakage, the threshold voltage of NL should be low. Thus, the desired back-gate voltages of the transistors from the write stability perspective are $V_{\text{dd}}$, $V_{\text{dd}}$, 0, $V_{\text{dd}}$, and 0 for AL, PL, NL, PR, AR, and NR, respectively.

3.3. Hold state

In most of the time, no read or write operation is performed placing the array cells in the hold mode where the bitlines are pre-charged to $V_{\text{dd}}$ and the wordline is set to 0. In this mode, the most important parameter is the standby power [20]. In the case of Fig. 2, the transistors AR, PR, and NL are in the subthreshold regions of operation, and hence, their subthreshold currents contribute to the static power. In this state, to minimize the static power, the absolute value of the threshold voltage of these transistors should be high. Hence, the desired back-gate voltages of the transistors from the static power view are 0, $V_{\text{dd}}$, and 0 for AR, PR, and NL, respectively. The back-gate voltages of other transistors are not important.

To summarize our discussion, in Table 2, the bitline voltages and the desired back-gate voltages of different transistors in the SRAM cell of Fig. 2 are listed. In this table, BPX, BNX and BAX are used to resemble the back-gate voltages of the pull-up (P), pull-down (N), and access (A) transistors, respectively, in the side storing the logic X which can be “0” or “1”. Also, BLX denotes the bitline voltage near the node storing the logic X. NI stands for not important.

### 4. Existing dynamic back-gate voltage techniques

The FinFET device has a superior short channel control compared to the planar bulk transistor. However, to have acceptable read and write stabilities in the SRAM cells implemented using these devices, the number of fins of the transistors should be increased (e.g., increasing the fin numbers of pull-down (access) for increasing read (write) stability [9]). Another approach for increasing the stabilities is to use the back-gate of transistors [8–11]. Using the back-gate, one also can lower the static power. This approach has been invoked in Refs. [8,9] where the back-gate of the access transistors are connected to the adjacent bit-cell storage nodes as shown in Fig. 3. This scheme is referred to as ABG structure here. For the ABG SRAM cell, the read SNM increases compared to the structure which is only composed of tied-gate FinFETs, referred to as DG structure here. In the ABG cell, however, the read current degrades owing to the zero back-gate bias of the discharging access transistor. In the ABG cell, the desired back-gate voltages for the read stability and static power (see Table 2) are applied to the back-gates of all six transistors of the SRAM cell.

It has been shown that the read SNMs of the ABG and DG SRAM cells may become equal if the work functions of the gates in the DG structure are increased compared to those in the ABG structure [9]. In this case, the write margin also improves in the ABG cell as compared to that of the DG structure especially at low $V_{\text{dd}}$’s due to the stronger access transistor [9]. For the area comparison, the layouts for the structures are shown in Fig. 4 where we used the design rules for the FinFET technology reported in Ref. [21]. Similar to [9], we assumed the SOI FinFET technology where n-well to p-well spacing rules can be avoided and the nFET and pFET drains can be directly connected. Compared to increasing the number of fins, the approach connecting the back-gate of access transistors to the adjacent bit-cell storage nodes has the advantage of not increasing the area [9,22]. This is also evident from Fig. 4b and c where there is no extra contact for the back-gate. More specifically, there is one contact for the back-gate of the access transistor and the gates of the pull-down and pull-up transistors.
The authors in Ref. [9] suggested connecting the back-gate of pull-up transistors to a Write Wordline (WWL). In this method, whose layout is shown in Fig. 4c, the area increases by about 12.5% compared to that of the ABG structure with tied-gate pull-up due to the additional contact space required for WWL [22]. This line was assumed to route horizontally in a different metal layer than that of the WL [9]. The WWL has been suggested to be set to \( V_{dd} \) during the write state and 0 or an intermediate value during the read and hold states [9]. One of the problems with this approach, as implied from Table 2, is that same back-gate voltage bias is used for both BP0 and BP1 in read and hold states [9]. Assuming NI can be 0, the desired back-gate voltages are \( V_{dd} \) for BP0 and 0 for BP1. Therefore, to have one fixed value for both pull-up transistors in both the operation modes, we should choose a compromising value. In Ref. [9], the authors suggested 0.48 V for a technology of 22 nm gate length when the supply voltage varied from 0.4 V to 1.2 V. Moreover, the approach in Ref. [9] sets the back-gate bias of both pull-up transistors to \( V_{dd} \) during the write mode irrespective of the data being written to the cell, whereas based on the results presented in Table 2, it is most optimal for write margin enhancement to set the back-gate of the pull-up on the node storing logic “0” (BP0) at zero bias and that of the pull-up on the node storing logic “1” (BP1) at \( V_{dd} \). Additionally, the implementation of this approach requires some circuitry (which has some overhead) for the generation and distribution of the fixed voltage along with setting the WWL to \( V_{dd} \) during the write and 0.48 V during the read and hold states.

5. Proposed dynamic back-gate voltage technique

In this work, we suggest a technique in which the back-gate voltages of the pull-up transistors are dynamically adjusted. The values of the voltages are set based on the desired values of each state. Table 2 suggests that, in the hold state, the back-gate voltage of the pull-up transistor whose drain stores logic “0” should be \( V_{dd} \) and the back-gate voltage of the other pull-up transistor is not important. Hence, in our design the back-gates are precharged to \( V_{dd} \) (as is done for the bitlines) to have the highest threshold voltage for the pull-up transistors. In the write state, the pull-up transistor whose drain stores logic “1”, should be weak, and hence, its back-gate voltage should be set to \( V_{dd} \). In this case, the other pull-up transistor should be strong to have a high \( V_{trip} \), and hence, its back-gate voltage should be set to 0. The bias, however, turns on the OFF state pull-up with the back-gate during the write operation increasing the power consumption. First, note that, the use of the midgap work function metals for the gates yields high threshold voltage transistors with rather small ON current (high resistance). Second, turning on the pull-up helps the write operation reducing its required operation time. Thus, the time that we are required to apply this bias is reduced. Table 2 also suggests in the read state, the pull-up transistor whose drain stores logic “1” should have the back-gate voltage of 0. The back-gate voltage of the other pull-up transistor should be \( V_{dd} \). These values are complement of the desired values for the write operation. Hence, we cannot fix the connection of the back-gates of the pull-up transistors to the corresponding storage nodes to avoid detrimental degradation of the write stability. Since the stored value is not known a priori, we need to choose a fixed value for the back-gate voltages of the pull-up transistors regardless of the stored value. In this work, we propose to set the value based on maximizing the read SNM.

We also leave pull-down transistors in the tied-gate mode, because it is the favorable mode from read stability and static power perspective as shown in Table 2. Also, write margin sensitivity to pull-down threshold voltage is much smaller compared to those of access and pull-up transistors [19]. The back-gates of the access transistors are also connected to the adjacent storage nodes (similar to the other ABG structures). This is the favorable case from read stability and static power perspectives as shown in Table 2.

To set the desired back-gate voltages of the pull-up transistors based on the operation state of the SRAM cell, we propose the circuit diagram for the SRAM array which is shown in Fig. 5. In the proposed scheme, the pull-up back-gate biases are data dependent and set based on the input data to be written to the cell using an added write driver circuitry as shown in Fig. 5. In this case, proper values of the bitlines and pull-up back-gate voltages should be set.
before the wordline is activated, while in the case of the conventional SRAM cell, the setting of the voltages are performed only for the bitlines. Since the interconnect used for the back-gate voltage has the same length (interconnect dominant capacitance [22]) as that of the bitline, the setting of the voltages should be performed at about the same time. Sharing the added circuitry among the cells of each column makes its area and power overhead negligible. The extra write driver typically induces a very small area penalty [23] (about 0.5% for an array of 128 cells per column [24]). The hold state biasing of the back-gates, which lowers the standby power as well, is performed by an extra precharge circuit, as shown in Fig. 5. As a rule of thumb, the area overhead of the extra precharge circuit should be much less than that of the write driver circuit [25]. An optimum pre-generated back-gate voltage bias ($V_{opt}$) for the read state is applied to the back-gate lines via a pair of nMOS switches (Fig. 5). These nMOS sizes are determined to achieve the required voltage swing on the back-gate lines from the precharged value of $V_{dd}$ set during the hold state (initial state) to the optimum value ($V_{opt}$) required for the read operation, within the read cycle. Therefore, these nMOS switches are expected to occupy less area than that of the extra write driver due to the lower voltage swing required on the back-gate lines and the longer time available for this voltage swing to be completed. The optimum back-gate voltage bias ($V_{opt}$) can also be generated by a low $V_{dd}$ voltage reference (e.g., [26,27]). As the voltage reference is shared for the whole chip, its area and power penalty is negligible [26,27].

It should be noted that the layout of the proposed SRAM cell remains similar to Fig. 4c. The difference is that the pull-up back-gate lines are assumed to route vertically (on contrary to horizontally in the approach of [9]) in a different metal layer than that of the bitlines to eliminate the cross talk noise to the parallel bitlines.

### 6. Results and discussion

In this part, we study the efficacy of the proposed scheme by comparing its performance with those of the DG structure, the ABG structure proposed in Ref. [8] where the independent-gate mode is used only for the access transistors, the ABG structure with back-gate voltage of 0 and $V_{dd}$ for the pull-up transistors during the read/hold and write states, respectively [9], and the ABG structure with back-gate voltage of 0.48 V and $V_{dd}$ for the pull-up transistors during the read/hold and write states, respectively [9]. In the case of the DG structure, to increase the read stability, we increase the gate work function to 4.75 eV. By increasing the gate work function further, the read stability decreases instead of increasing due to the severe subthreshold leakage current increase of the pMOS pull-up as discussed in Section 3. Next, we present the static characteristics of one SRAM cell in each structure with the corresponding back-gate bias conditions.

#### 6.1. Nominal study

First, we consider the write stability metric (write margin) for which different definitions have been suggested in the literature [19]. In this work, we use the difference between $V_{dd}$ and the minimum wordline voltage, namely, combined wordline margin (CWLM), that can cause a successful write operation as a metric [19]. It has been shown that this metric has a Gaussian distribution in the presence of process variations [19,29]. The write margin of different structures versus the supply voltage is depicted in Fig. 6. The results reveal that our proposed structure has the highest write margin among different structures even more than the ABG structure, in which the back-gate of the pull-up transistors are connected to $V_{dd}$. It should be noticed out the proposed structure has an acceptable write margin even for $V_{dd}$'s as low as 0.5 V...
while the area is compact due to using FinFETs with one fin. Additionally, to avoid the half-selected issue for the cells in the selected row, it has been suggested that the whole row is simultaneously written [30]. Using this approach, in this work, we assume 8 cells (one byte) in each row for each SRAM sub-block [31]. On the other hand, the half-selected cells in the same column as that of the cell being written have their wordlines deactivated. Hence, during the short time of the write operation, the storage node voltages of the half-selected cells do not change considerably yielding high half-selected cell stability.

As discussed in Section 3.3, the static power is the most important metric in the hold state. In Fig. 7, we compare the static powers of the structures. The results demonstrate that the DG structure has about one order of magnitude higher static power than that of the ABG structure with tied-gate mode pull-up. This may be justified by noting that, due to the higher gate work function in the DG structure, the pull-up transistor has higher subthreshold leakage current. In the case of the independent-gate mode pull-up, if the back-gate voltages of the pull-up transistors are set to 0, the subthreshold leakage current will increase considerably at high supply voltages. The results indicate that our proposed structure and ABG structure with tied-gate pull-up transistors have the least static power. The reason for the lower static power for these structures is that the back-gate voltage of the OFF state pull-up transistors is $V_{dd}$ resulting in a higher absolute value for the threshold voltage.

In Fig. 8, we have plotted the nominal (without considering process variation impacts) read SNM versus the supply voltage for all the structures. As evident from the figure, for the supply voltages larger than 0.6 V, the ABG structure [8] has a higher read SNM than that of the DG structure in spite of increasing the gate work function for the DG structure. Using the independent-gate mode operation for the pull-up transistors decreases the read SNM. This may be attributed to the smaller transconductance of independent-gate FinFET compared to that of the tied-gate one [4]. The smaller transconductance leads to a smaller gain for the inverter determining the transfer characteristic and consequently the read SNM becomes smaller [18]. If the back-gate of the pull-up transistors is connected to the ground, the read SNM decreases due to the increase in the subthreshold leakage current of the pull-up transistors, especially at higher supply voltages. The back-gate of the pull-up transistors may be connected to an intermediate fixed voltage. The back-gate voltages of the pull-up transistors are set to 0 and 0.48 V for the supply voltages between 0.4 V and 0.9 V while lower than those of the DG and ABG structures for the supply voltages between 0.7 V and 0.9 V. The lower read stability may be attributed to the less transconductance of the independent-gate pull-up transistor with respect to the tied-gate one which causes better stability for the DG and ABG structures at high supply voltages. In addition, the read SNM of the proposed technique, similar to that of the ABG [8], is the highest for the supply voltages from 0.4 V to 0.6 V.

The read currents for different structures are compared in Fig. 9. As is evident from the figure, the read currents of the ABG structures (including our proposed structure) are more than that of DG structure for lower $V_{dd}$’s. This may be attributed to the fact that the lower gate work function effect (lower threshold voltage) dominates the zero back-gate bias of the access transistor (higher threshold voltage) in the case of the ABG structures. At higher supply voltages, the read current of the ABG structure, in which the back-gates of the pull-up transistors are connected to ground, decreases because the subthreshold leakage of the OFF state pull-up transistor increases. This raises the value of $V_{read}$ (the source voltage of the access transistor) leading to a lower overdrive voltage for the (discharging) access transistor, and hence, a smaller read current. At the highest supply voltage ($V_{dd} = 0.9$ V), the read circuit shown in Fig. 5, we can choose an optimum back-gate voltage based on the supply voltage for the read state. We used simulations to find the optimum values for the maximum read SNM by sweeping the back-gate voltage between 0 and $V_{dd}$ for each supply voltage. The optimum values considering the read stability are listed in the inset of Fig. 8. Due to the process variations, the optimum value for a given $V_{dd}$ may vary. To study the sensitivity of the read SNM to the optimum value, we changed the optimum values for all the supply voltages studied in this work by 20% and measured the read SNM. The results showed at most 2.5% change in the value of the SNM. Hence, the preciseness of the voltage generator is not of a critical concern. The results indicate that the read stability of our design is higher than those of the ABG structures with fixed pull-up back-gate voltages of 0 and 0.48 V for the supply voltages between 0.4 V and 0.9 V while lower than those of the DG and ABG structures for the supply voltages between 0.7 V and 0.9 V. The lower read stability may be attributed to the less transconductance of the independent-gate pull-up transistor with respect to the tied-gate one which causes better stability for the DG and ABG structures at high supply voltages. In addition, the read SNM of the proposed technique, similar to that of the ABG [8], is the highest for the supply voltages from 0.4 V to 0.6 V.
currents of the ABG structures are lower than that of the DG structure because the zero back-gate bias dominates the lower gate work function. This implies that the use of the independent-gate structure only slightly lowers the read speed for the highest $V_{dd}$.

It should be noted that the midgap work function values used in this work are more appropriate for low power applications. For example, the read current values are very close to those of a SRAM array fabricated using a 28 nm low power SOC process [32].

### 6.2. Study of process variation effect

Now, we study the impact of the process variation on the SRAM cell structures discussed in this work. In addition to channel length and silicon thickness variations due to the line-edge roughness, there are other sources of variations including random dopant fluctuations as well as work function, fin height, and oxide thickness variations. As the experimental results presented in e.g., [33,34] show, the random dopant fluctuation can be ignored due to the fact that the body is lightly doped. Also, the work function variation can be suppressed by using gate-last process where amorphous metal gate are deposited after the high-temperature annealing and activation process steps [35]. On the other hand, since the real values of fin height and oxide thickness are not determined by the lithography process steps [35].

There are other sources of variations including random dopant fluctuations as well as work function, fin height, and oxide thickness variances such as the standard variations, namely, $\sigma_{\eta_1}$ and $\sigma_{\eta_2}$, respectively, are 7% $I_{dd}$ [9]. The variation of read SNM and CWLM may be very well modeled by a normal distribution [19,29]. Therefore, we assume that these metrics have Gaussian distributions which are functions of twelve random variables. Denoting the metric by $y$, we may write

$$y = f(x_1, \ldots, x_{12}),$$

where $x_1, \ldots, x_{12}$ are the Gaussian random variables with the averages of $\eta_1, \ldots, \eta_{12}$ and standard deviations of $\sigma_1, \ldots, \sigma_{12}$. These twelve random variables are channel lengths and silicon thicknesses of six transistors of the SRAM cell, hence, we can use the following expression to find their statistical characteristics using bivariate Taylor Series as [36]:

$$\mu_y = f(\eta_1, \ldots, \eta_{12})$$

$$\sigma_y^2 = \sum_{i=1}^{12} \left( \frac{\partial f}{\partial x_i} \right)^2 \sigma_i^2$$

Here, we used the cell sigma, the yield figure of merit of the SRAM, which is defined as the minimum amount of variation needed to cause a read or write failure. The cell sigma is given by the mean ($\mu$) divided by the standard deviation ($\sigma$) [9]. Nowadays, six-sigma ($6\sigma$) yield or larger is required for large SRAM arrays [9].

In Fig. 10, we have plotted the read SNM and CWLM cell sigma yields versus the supply voltage obtained from simulations and using Eqs. (2) and (3). It should be noted that $\mu_y$’s in Eq. (2) were approximated by their nominal values which were presented in Figs. 6 and 8. Also, since the variations of the read SNM and CWLM were linearly proportional to the variations of the random variables ($\eta_i$) [19,29], the derivatives in (3), $\partial f/\partial \eta_i$, were easily found by using the metric values through the simulations at some values of $x_i$ near the nominal values ($\eta_i$). As is evident from the figure, our proposed structure and the ABG structure with pull-up back-gate voltages equal to 0 have over six-sigma read yield for supply voltages as low as 0.5 V. This is due to the high nominal read SNM and less sensitivity to device parameters especially at low supply voltages. As expected the write yield degrades considerably for low supply voltages. Among these structures, only our proposed structure has over six-sigma write yield down to $V_{dd}$ equal to 0.55 V (0.15 V below the minimum of the other structures). For our structure, at $V_{dd} = 0.5$ V, the write margin cell sigma is slightly lower than six. To have six-sigma write yield, one may lower gate work function of the transistors to 4.57 eV to increase the writability. This work function tuning makes the access (as well as pull-down) nMOS stronger while making the pull-up pMOS weaker. These strength changes improves the write yield such that both the read and write cell sigma yields becomes above six. In this case, the read current increases by 56% while the static power also increases by 47% compared to the case of no work function tuning. The static power is still 23% lower than that of the structure (without work function tuning) when the supply voltage of 0.6 V is used. Therefore, if a proper work function tuning can be performed, one may use $V_{dd} = 0.5$ V to lower the static power (as well as the dynamic power due to a lower supply voltage). With similar work function tuning, we used the gate work function of 4.61 eV, 4.54 eV, 4.49 eV, and 4.61 eV for the DG, ABG, ABG with pull-up back-gate voltage of 0 during the read/hold states, and ABG with pull-up back-gate voltage of 0.48 V during the read/hold states, respectively. This resulted in the minimum operating voltage of 0.65, 0.65, 0.6, and 0.7 V, respectively. These numbers suggest that the proposed structure still could operate with the supply voltage which is 0.1 V lower than that of the other structures. Next, we consider the SNM cell sigma yield for the half-selected cells in the same column of the selected cell shown in Fig. 11. For the read operation (Fig. 11b), the yields for all the structures are very high. In the case of the write operation, while the half-selected disturb is the worst for our proposed structure, it is still higher than six.

It should be noted that as the wordlines of half-selected cells are inactive, the storage node voltages of the half-selected cells do not have enough time for changing their values for threatening
In this part, we study the energy consumptions of the structures per read and write operations. In the structures considered in this work, the main sources of the dynamic power consumption are the voltage changes of the long wordline, bitlines, and pull-up back-gate lines. The increased static currents of the cells during the read and write operations (including those induced due to the application of the back-gate biases) can be neglected as the cells are in the hold state most of the time while the read and write times are very short. To perform this study, we assumed a SRAM block with 8 cells in each row and 128 cells in each column and the line short. To perform this study, we assumed a SRAM block with 8 cells in each row [31] and 128 cells in each column [24] and the line capacitance was taken as 0.25 fF/μm to account for the dominant interconnect capacitance as well as the drain/gate contact capacitance [22]. Hence, we included the additional parasitic capacitances for the pull-up back-gate lines as well as the bitlines. The results for the energy consumptions of all the structures versus the supply voltage are plotted in Fig. 12. As is observed from the results the proposed structure consumes more dynamic energy compared to those of the other structures. This is due to the more voltage switchings of the lines connected to the back-gates of the pull-up transistors. Since the main contributor to the total power of SRAM is the static power [20,33], the larger dynamic energy for the proposed structure may not be considered as major shortcoming. It should be noticed that since our structure could operate at lower minimum supply voltages, the dynamic power may be lowered by lowering the supply voltage wherever the corresponding speed reduction can be tolerated. The supply voltage reduction also lowers the static power.

7. Conclusions

We proposed a dynamic back-gate design for the pull-up transistors of SRAM cells to increase the cell stability during the read and write states while decreasing the static power during hold state. The optimization was performed by dynamically adjusting the voltages of the back-gates of the pull-up transistors in the cell. The voltages were determined in order to have maximum stability during the read and write states and minimum static power during the hold state. During the write operation, we used an extra write driver which sets the desired back-gate voltage of pull-up transistors to considerably increase the write margin. During the hold state, to decrease the static power, the back-gates were precharged to the supply voltage using an extra precharge circuit. The read stability degradation was prevented using proper back-gate voltages generated using nMOS switches. To reduce the area and power overheads, the added circuitry was shared for each column. Also, the proposed structure had the highest write margin among the structures considered in this work. The half-selected issue for the cells in the selected row has been avoided by writing the whole row simultaneously. The half-selected cells in the same column of the selected cell had high stability during read and write operations. Therefore, the proposed cell may be used for the applications where writing the whole row simultaneously is possible. For the cell with single fin FinFETs, the minimum operating voltage for six-sigma yield obtained to be about 0.55 V which was 0.15 V lower than that of a recently proposed structure. In addition, our structure had much less static power. The minimum operating voltage of the proposed structure could be lowered to 0.5 V by some work function tuning while the minimum operating voltage for all other structure was 0.6 V or higher using similar work function tunings.

Acknowledgement

The first two authors acknowledge the financial support by the Iranian National Science Foundation (INSF).

References


