Ultra Low-Power Clocking Scheme Using Energy Recovery and Clock Gating

Hamid Mahmoodi, Member, IEEE, Vishy Tirumalashetty, Matthew Cooke, and Kaushik Roy, Fellow, IEEE

Abstract—A significant fraction of the total power in highly synchronous systems is dissipated over clock networks. Hence, low-power clocking schemes are promising approaches for low-power design. We propose four novel energy recovery clocked flip-flops that enable energy recovery from the clock network, resulting in significant energy savings. The proposed flip-flops operate with a single-phase sinusoidal clock, which can be generated with high efficiency. In the TSMC 0.25-μm CMOS technology, we implemented 1024 proposed energy recovery clocked flip-flops through an H-tree clock network driven by a resonant clock-generator to generate a sinusoidal clock. Simulation results show a power reduction of 90% on the clock-tree and total power savings of up to 83% as compared to the same implementation using the conventional square-wave clocking scheme and flip-flops. Using a sinusoidal clock signal for energy recovery prevents application of existing clock gating solutions. In this paper, we also propose clock gating solutions for energy recovery clocking. Applying our clock gating to the energy recovery clocked flip-flops reduces their power by more than 1000× in the idle mode with negligible power and delay overhead in the active mode. Finally, a test chip containing two pipelined multipliers one designed with conventional square wave clocked flip-flops and the other one with the proposed energy recovery clocked flip-flops is fabricated and measured. Based on measurement results, the energy recovery clocking scheme and flip-flops show a power reduction of 71% on the clock-tree and 39% on flip-flops, resulting in an overall power savings of 25% for the multiplier chip.

Index Terms—Clock gating, energy recovery, flip-flop, low power, sinusoidal clock.

I. INTRODUCTION

TRADITIONALLY, the demand for high performance was addressed by increasing clock frequencies with the help of technology scaling. However, in deep sub-micrometer generations, the increasing trend in clock frequency has slowed down and instead higher performance is obtained by increasing parallelism at the architectural level. A very clear example of this trend is the recent move towards multi-core architectures for processors [1]. With the continuing increase in the complexity of high-performance VLSI system-on-chip (SOC) designs, the resulting increase in power consumption has become the major obstacle to the realization of high-performance designs. Such increase in the complexity of synchronous SOC systems, increases the complexity of the clock network and hence increases the clock power even if the clock frequency may not scale anymore. Hence, the major fraction of the total power consumption in highly synchronous systems, such as microprocessors, is due to the clock network. In the Xeon Dual-core processor, a significant portion of the total chip power is due to the clock distribution network [1]. Thus, innovative clocking techniques for decreasing the power consumption of the clock networks are required for future high performance and low power designs.

Energy recovery is a technique originally developed for low-power digital circuits [2]. Energy recovery circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors by using an ac-type (oscillating) supply voltage [2]. In this paper, we apply energy recovery techniques to the clock network since the clock signal is typically the most capacitive signal in a chip. The proposed energy recovery clocking scheme recycles the energy from the capacitance in each cycle of the clock. For an efficient clock generation, we use a sinusoidal clock signal. The rest of the system is implemented using standard circuit styles with a constant supply voltage. However, for this technique to work effectively there is a need for energy recovery clocked flip-flops that can efficiently operate with a sinusoidal clock. A pass-gate energy recovery clocked flip-flop has been proposed in [3] that works with a four-phase sinusoidal clock. The main disadvantage of the pass-gate energy recovery clocked flip-flop is that its delay takes a major fraction of the total cycle time; therefore, the time allowed for combinational logic evaluation is significantly reduced. In addition, it requires four phases of the clock, adding considerable overhead to clock generation and routing. In this paper, we propose four high-performance and low-power energy recovery clocked flip-flops that operate with a single-phase sinusoidal clock. The proposed flip-flops exhibit significant reduction in delay, power, and area as compared to the four-phase pass-gate energy recovery clocked flip-flop.

Clock gating is another popular technique for reducing clock power [10]. Even though energy recovery clocking results in substantial reduction in clock power, there still remains some energy loss on the clock network due to resistances of the clock network and the energy loss in the oscillator itself due to non-adiabatic switching. Hence, it is still desirable to apply clock gating to the energy recovery clock for further reducing the clock power during idle periods. The existing clock gating solutions are based on masking the local clock signal using masking logic gates (NAND/NOR) [10]. These methods of clock gating do not work for energy recovery clocking. This is because insertion of masking logic gates eliminates energy recovery from the
remaining capacitances in downstream fan-out. To the best of our knowledge, there have not been any clock gating solutions proposed for the energy recovery clocking.

In this paper, we propose clock gating solutions for the energy recovery clock. We modify the design of the existing energy recovery clocked flip-flops to incorporate a power saving feature that eliminates any energy loss on the internal clock and other nodes of the flip-flops. Applying the proposed clock gating technique to the flip-flops reduces their power by a substantial amount (1000×) during the sleep mode. Moreover, the added feature has negligible power and delay overhead when flip-flops are in the active mode.

The remainder of this paper is organized as follows. In Section II, the conventional four-phase pass-gate energy recovery clocked flip-flop is reviewed and the proposed energy recovery clocked flip-flops are described. In Section III, extensive simulation results of individual flip-flops and their comparisons are presented. Section IV includes system integration, clock generation and the clock-tree implementation. In Section V, the clock gating approaches are proposed for energy recovery clocked flip-flops. Section VI includes the design of an energy recovery clocked pipelined multiplier chip. The test and measurement results of the chip are presented in Section VII. Finally, the conclusion of this paper appears in Section VIII.

II. ENERGY RECOVERY CLOCKED FLIP-FLOPS

In this section, our proposed flip-flops, as well as the conventional energy recovery clocked flip-flop, are presented and their operations are discussed. The conventional energy recovery clocked flip-flop is a four-phase transmission-gate (FPTG) flip-flop [3]. FPTG is similar to the conventional transmission-gate flip-flop (TGFF) [4] except that it uses four-transistor pass-gates designed to conduct during a short fraction of the clock period. The main disadvantages of this flip-flop are the need for four sinusoidal clock signals and its long delay. In addition, transistors required for the pass-gates are large, resulting in large flip-flop area.

Another approach for energy recovery clocked flip-flops is to locally generate square-wave clocks form a sinusoidal clock [3]. This technique has the advantage that existing square-wave flip-flops could be used with the energy recovery clock. However, extra energy is required in order to generate and possibly buffer the local square waves. Moreover, energy is not recovered from gate capacitances associated with clock inputs of flip-flops.

Recovering energy from internal nodes of flip-flops in a quasi-adiabatic fashion would also be desirable. However, storage elements of flip-flops cannot be energy recovering because we assume that they drive standard (non-adiabatic) logic. Due to slow rising/falling transitions of energy recovery signals, applying energy recovery techniques to internal nodes driving the storage elements can result in considerable short-circuit power within the storage element. Taking these factors into consideration, we developed flip-flops that enable energy recovery from their clock input capacitance only, while internal nodes and storage elements are powered by regular (constant) supply. Employing our flip-flops in system designs enables energy recovery from clock distribution networks and clock input capacitances of flip-flops.

The first proposed energy recovery clocked flip-flop, sense amplifier energy recovery (SAER) flip-flop, is shown in Fig. 1. This flip-flop, which is based on the sense amplifier flip-flop proposed in [4], is a dynamic flip-flop with precharge and evaluate phases of operation. In [5], this flip-flop is used to operate with a low-voltage-swing clock. We use this flip-flop to operate with an energy recovery clock. When the clock voltage exceeds the threshold voltage of the clock transistor (MN1), evaluation occurs. At the onset of evaluation, the difference between the differential data inputs (D and DB) results in an initial small voltage difference between SET and RESET nodes. This initial small voltage difference is then amplified by the cross coupled inverter and as a result either SET or RESET switches to low. This state transition is captured by the set/reset latch (cross coupled NAND gates) and retained for the rest of the cycle time until next evaluation occurs. The SET and RESET nodes are precharged high when the clock voltage falls below Vdd − Vtp, where Vtp is the threshold voltage of the precharging transistors (MP1 and MP2).

The energy is recovered from the clock input capacitance (gate capacitances of MN1, MP1, and MP2) by applying a sinusoidal clock generated using a resonant clock generator circuit which will be explained in Section IV (see Fig. 11). Notice that there is no energy recovered form the internal nodes of the flip-flop (such as nodes SET and RESET). Since the energy recovery clock has slow rising and falling transitions, there can be overlap between evaluation and precharge phases. This overlapping results in short-circuit current. In order to reduce the amount of this short-circuit current, the threshold voltages of the precharging transistors can be increased. In scaled dual-threshold voltage (dual-Vt) CMOS technologies, high-Vt devices can be used for the precharging transistors. Fig. 2 shows typical simulated waveforms of this flip-flop designed in a 0.25-μm CMOS technology.

Input data (D) switches to high when the clock is low (before the clock starts rising) and SET and RESET are both pre-charged to high. When the clock starts rising, since D is high, SET is discharged which consequently results in a change of state of the latch output (Q and QB). In the following falling
Although the SAER flip-flop is fast and uses fairly low power at high data switching activities, its main drawback is that either the SET or RESET node is always charged and discharged every cycle, regardless of the data activity. This leads to substantial power consumption at low data switching activities where the data is not changing frequently. We consider two approaches to address this problem.

One approach is to use a static flip-flop, and the other is to employ conditional capturing [6]. Fig. 3 shows the static differential energy recovery (SDER) flip-flop. This flip-flop is a static pulsed flip-flop similar to the dual-rail static edge-triggered latch (DSETL) [7]. The energy recovery clock is applied to a minimum-sized inverter skewed for fast high-to-low transition. Such skewing creates a sharp high-to-low transition on CLKB to ensure correct timing for the flip-flop operation. The minimum sizing of the inverter reduces its short circuit power caused by slow rising of the input clock. The clock signal and the inverter output (CLKB) are applied to transistors MN1 and MN2 (MN3 and MN4). The series combination of these transistors conducts for a short period of time during the rising transition of the clock when both the CLK and CLKB signals have voltages above the threshold voltages of the nMOS transistors. Since the clock inverter is skewed for fast high-to-low transitions, the conducting period occurs only during the rising transition of the clock, but not on the falling transition. In this way, an implicit conducting pulse is generated during each rising transition of the clock. A cascade of three inverters instead of one can give a slightly sharper falling edge for the inverted clock (CLKB).

The second approach for minimizing flip-flop power at low data switching activities is to use conditional capturing to eliminate redundant internal transitions. Fig. 4 shows the differential conditional-capturing energy recovery (DCCER) flip-flop. Similar to a dynamic flip-flop, the DCCER flip-flop operates in a precharge and evaluate fashion. However, instead of using the clock for precharging, small pull-up pMOS transistors (MP1 and MP2) are used for charging the precharge nodes (SET and RESET). The DCCER flip-flop uses a NAND-based set/reset latch for the storage mechanism. The conditional capturing is implemented by using feedback from the output (Q and QB) to the control transistors MN3 and MN4 in the evaluation paths. Therefore, if the state of the input data (D and DB) is same as that of the output (Q and QB), both left and right evaluation paths are turned off preventing SET and RESET from being discharged. This results in power saving at low data switching activities when input data remains idle for more than one clock cycle.

Due to its sinusoidal nature, the CLK signal is generally less than \( V_{dd}/2 \) during a significant part of the conducting window. Therefore, a fairly large transistor is used for MN1. Moreover,
since there are four stacked transistors in the evaluation path, significant charge sharing may occur when three of them become on simultaneously. Having properly sized pull-up pMOS transistors (MP1 and MP2) instead of clock controlled precharge transistors ensures a constant path to $V_{dd}$, which helps to reduce the effect of charge sharing. Although MP1 and MP2 are statically on, they do not result in static power dissipation because as soon as the data sampling finishes and Q obtains the values of D, the pull down paths get turned off and the SET and RESET nodes are pulled back high without any static power being dissipated. Another property of the circuit that helps reduce charge sharing is that the clock transistor (MN1), which is the largest transistor in the evaluation path, is placed at the bottom of the stack. Therefore, the diffusion capacitance of the source terminal of MN1 is grounded and does not contribute to the charge sharing.

Fig. 5 shows a single-ended conditional capturing energy recovery (SCCER) flip-flop. SCCER is a single-ended version of the DCCER flip-flip. The transistor MN3, controlled by the output QB, provides conditional capturing. The right-hand side evaluation path is static and does not require conditional capturing. Placing MN3 above MN4 in the stack reduces the charge sharing.

III. SIMULATION RESULTS AND COMPARISONS

All the flip-flops were designed and laid-out using TSMC 0.25-μm process technology with a supply voltage of 2.5 V. Netlists with parasitic capacitances were extracted from layouts and simulated using HSPICE. The designs were optimized at a temperature of 25 °C for a clock frequency of 200 MHz. However, since the FPTG flip-flop is a dual-edge triggered flip-flop, it was designed to operate at a clock frequency of 100 MHz. A load capacitance of 30 fF was used for all outputs. Fig. 6 illustrates our timing definitions for energy recovery clocked flip-flops. Delay is measured between 50% points of signal transitions. Setup time is the time from when data becomes stable to the rising transition of the clock. Hold time is the time from the rising transition of the clock to the earliest time that data may change after being sampled. Setup and hold times are measured with reference to the 50% point of the rising transition of the clock.

The proposed flip-flops are compared with the FPTG flip-flop. For individual flip-flop simulations, an ideal sinusoidal clock was used. Fig. 7(a) shows clock-to-output (CLK-Q) delay and data-to-output (D-Q) delay versus setup time for all the flip-flops. It is apparent that the delays of the FPTG flip-flop
are much larger as compared to the proposed flip-flops. Fig. 7(b) shows a clearer illustration of the behavior of the proposed flip-flops in the minimum delay region. For any flip-flop, there is an optimum setup time that results in a minimum D-Q delay. This optimum setup time is used for comparisons of setup time. As shown in Fig. 7, the CLK-Q delay becomes independent of setup time for long setup times. We use this value of CLK-Q delay for comparisons of CLK-Q delay. The SCCER flip-flop exhibits the smallest minimum D-Q delay, while the SAER flip-flop shows the smallest CLK-Q delay. The SDER flip-flop has the shortest setup time among the proposed flip-flops. Fig. 8 shows the dependence of D-Q and CLK-Q delays on clock frequency. Flip-flops were simulated from a frequency of 50 MHz to their maximum frequency of operation. The flip-flops were not reoptimized for each frequency. Although all the proposed flip-flops fail at frequencies above 400 MHz, they can easily be resized to operate at higher frequencies. The proposed flip-flops show a higher range of operational frequency, and their delays are much less dependent on the clock frequency as compared to the FPTG flip-flop.

Fig. 9 shows power as a function of data switching activity for different flip-flops. The SAER flip-flop has the lowest power consumption at high switching activities; however, it has the maximum power at low switching activities. The SDER and conditional capturing (DCCER and SCCER) flip-flops show less power consumption at low switching activities. The SDER and conditional capturing flip-flops, however, consume more power than that of SAER flip-flop at high switching activities. This is because of the fact that at high switching activities there is much less opportunity for energy savings by using a static flip-flop or employing conditional capturing.

Table I summarizes the numerical results for the flip-flops. The proposed flip-flops exhibit more than 80% delay reduction, a power reduction of up to 46%, and an area reduction of up to 77%, as compared to the FPTG flip-flop.

### Table I

<table>
<thead>
<tr>
<th>Flip-flop</th>
<th>min D-Q delay (ps)</th>
<th>setup time (ps)</th>
<th>hold time (ps)</th>
<th>CLK-Q delay (ps)</th>
<th>Power* (µW)</th>
<th>PDP* (D)</th>
<th>Norm. PDP</th>
<th>Area (µm²)</th>
<th>Transistor count</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPTG</td>
<td>2401</td>
<td>-135*</td>
<td>740</td>
<td>2619.7</td>
<td>156.4</td>
<td>389.59</td>
<td>-1</td>
<td>580.8</td>
<td>16</td>
</tr>
<tr>
<td>SDER</td>
<td>391.6</td>
<td>35</td>
<td>270</td>
<td>268.2</td>
<td>120.8</td>
<td>47.305</td>
<td>0.1214</td>
<td>133.9</td>
<td>14</td>
</tr>
<tr>
<td>SAER</td>
<td>434.8</td>
<td>355.3</td>
<td>-190</td>
<td>79.5</td>
<td>106.4</td>
<td>46.293</td>
<td>0.1188</td>
<td>139.2</td>
<td>18</td>
</tr>
<tr>
<td>DCCER</td>
<td>373.1</td>
<td>115.7</td>
<td>150</td>
<td>174.3</td>
<td>101.7</td>
<td>37.944</td>
<td>0.0974</td>
<td>136.9</td>
<td>18</td>
</tr>
<tr>
<td>SCCER</td>
<td>285.9</td>
<td>125</td>
<td>0</td>
<td>123.3</td>
<td>83.88</td>
<td>23.981</td>
<td>0.0616</td>
<td>196.8</td>
<td>17</td>
</tr>
</tbody>
</table>

*Power is for long setup time; Power-Delay-Product (PDP) is the product of this power and the minimum D-Q delay.

As measured from the first phase clock (CLK0).

### IV. Energy Recovery Clocking

In order to demonstrate the feasibility of energy recovery clocking, we integrated 1024 energy recovery clocked flip-flops distributed across an area of 4 mm x 4 mm and clocked them by a single-phase sinusoidal clock through an H-tree clocking network. The flip-flops were grouped into registers of 32 flip-flops, and the registers were evenly spaced in this area. A common data input was used for all flip-flops to easily control the data switching activity of the system. The clock was distributed using an H-tree network on the metal-5 layer, which has the smallest parasitic capacitance to the substrate. The width of the clock-tree interconnects was selected to be the maximum (35 µm in our 0.25 µm process) to minimize parasitic resistances. Wider wires also minimize clock skew [11]. The study in [11] shows that with proper sizing and spacing of clock wires, the clock skew of a resonant clock can be comparable or even better than a square wave clock network. A lumped II-type resistance–capacitance (RC) model for each interconnect of the clock-tree was extracted and then connected together to make a distributed RC model of the clock-tree, as shown in Fig. 10. The energy recovery clock generator drives the source node of the clock-tree (node CLK in Fig. 10), and each final node of the clock-tree (CLK1 to CLK16) is connected to two 32-bit flip-flop registers.
Fig. 10. Distributed RC model of clock-tree.

Fig. 11. (a) Resonant energy recovery clock generator. (b) Non-energy recovery clock driver.

The energy recovery clock generator is a single-phase resonant clock generator as shown in Fig. 11(a). Transistor M1 receives a reference pulse to pull-down the clock signal to ground when the clock reaches its minimum; thereby maintaining the oscillation of the resonant circuit. This transistor is fairly large, and therefore, driven by a chain of progressively sized inverters. The natural oscillation frequency of this resonant clock driver is determined by

\[ f = \frac{1}{2\pi\sqrt{LC}} \]  

(1)

where \( C \) is the total capacitance connected to the clock-tree including parasitic capacitances of the clock-tree and gate capacitances associated with clock inputs of all flip-flops. In order to have an efficient clock generator, it is important that the frequency of the REF signal be the same as the natural oscillation frequency of the resonant circuit. In order to find the value of \( C \), first with a given \( L \) and with the REF signal at zero, the whole system, including the flip-flops, is simulated. The clock signal shows a decaying oscillating waveform settling down to \( V_{dd}/2 \). From this waveform, the natural decaying frequency is measured, and then by using (1), the value of \( C \) is calculated. For the system with each proposed flip-flop, this experiment is carried out to determine the value of \( C \). Having the value of \( C \), the value of \( L \) for the frequency of 200 MHz can again be determined from (1). The system consisting of the energy recovery clock generator, clock-tree, and flip-flops was simulated at the frequency of 200 MHz (for all the proposed energy recovery clocked flip-flops) with different data switching activities.

Fig. 12 shows a typical waveform of the generated energy recovering-clock. In order to compare with the square wave clocking, three flip-flops that operate with the square-wave clock were also designed. These flip-flops are hybrid latch flip-flop (HLFF) [8] and conditional capturing flip-flop (CCFF) [6], which are high-speed flip-flops, and transmission-gate flip-flop (TGFF) [4], which is a low-power flip-flop. For square wave clocking, the clock-tree is driven by a chain of progressively sized inverters as shown in Fig. 11(b). The whole system of clock buffers, clock-tree, and flip-flops was simulated at a frequency of 200 MHz with different data switching activities. Fig. 13 shows the results of this experiment. The system power is plotted versus data switching activity for the systems with different flip-flops. Among the square-wave flip-flops, the TGFF system shows the lowest power consumption for all switching activities.

The HLFF system has the highest power consumption at low switching activities, and the CCFF system shows the highest power consumption at high switching activities. Among the energy recovery clocked flip-flops, the systems with conditional capturing flip-flops (DCCER and SCCER) exhibit the lowest power consumption at low switching activities (below 66%). For high switching activities, the system with SAER flip-flops has the minimum power consumption. The energy recovery systems show less power consumption at all switching activities compared to the square-wave clocking, except for the energy recovery system with SDER flip-flops at switching activities.
The power is broken down into three components: flip-flop power, clock tree power, and clock generator power. Flip-flop power represents the power dissipated on the internal nodes of the flip-flops (including the power dissipated by the skewed inverter on the clock input). Notice that the clock tree power is due to the energy dissipated on the resistances of the wires in the clock tree (see Fig. 10). This power is measured by measuring the power drawn from the \( V_{dd}/2 \) supply in Fig. 11(a). Clock generator power represents the power dissipated by the resonant clock generator circuitry [see Fig. 11(a)], which is needed to generate the sinusoidal clock. Clock generator power is basically the power dissipated by the inverter buffer chain driving the gate of transistor M1 in Fig. 11(a). The energy recovery clocking scheme reduces the power due to clock distribution (clock-tree) by more than 90% compared to non-energy recovery (square-wave) clocking. The clock generator power overhead in the energy recovery scheme is very small (less than 2% of total power), which indicates that the clock generator is very efficient. As compared to the HLFF system, the SCCER system shows power savings of 83%, 65%, and 49% at data switching activities of 0%, 25%, and 50%, respectively. When compared to the TGFF system (the lowest power square-wave system), the SCCER system shows power savings of 75%, 50%, and 31% at data switching activities of 0%, 25%, and 50%, respectively.

Table II shows the numerical results of the power dissipated on the clock tree in each system and the percentage of energy recovered from the clock network of the energy recovery clocked flip-flops. The clock tree capacitance shown includes the wiring capacitance of the clock network and the gate capacitance shown by the flip-flop clock inputs. It is observed that although their capacitance of the clock network is about same or greater, the energy recovery clocking systems show significant reduction in the clock power compared to the square-wave clocking systems. To make the comparison fair, the clock power is normalized per pico-farad of the clock capacitance and shown in a separate column in Table II. It is observed that the energy recovery systems not only consume less clock tree power but also significantly less clock power per PF of load. The percentage of energy recovery from the clock network in all energy recovery clocked cases exceeds 93%.

It is also important to compare the energy recovery and square wave clocked flip-flops in terms of their delay characteristics. Table III shows the results for delay comparison between the energy recovery and square wave clocked flip-flops. Among

![Fig. 13. Total power versus switching activity at 200 MHz.](image)

![Fig. 14. Power breakdown.](image)
TABLE III
DELAY COMPARISON BETWEEN ENERGY RECOVERY AND SQUARE WAVE CLOCK FLIP-FLOPS

<table>
<thead>
<tr>
<th>Flip-Flop</th>
<th>Data to output delay (pS)</th>
<th>Clock to output delay (pS)</th>
<th>Setup time (pS)</th>
<th>Worst case delay change from SS to FF process corner (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TGFF</td>
<td>397</td>
<td>226</td>
<td>135</td>
<td>28</td>
</tr>
<tr>
<td>HLFF</td>
<td>247</td>
<td>229</td>
<td>-65</td>
<td>45</td>
</tr>
<tr>
<td>CCFF</td>
<td>217</td>
<td>196</td>
<td>-27</td>
<td>44</td>
</tr>
<tr>
<td>SDER</td>
<td>391.6</td>
<td>268.2</td>
<td>35</td>
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<td>434.8</td>
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<td>40</td>
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<td>373.1</td>
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<tr>
<td>SCCER</td>
<td><strong>285.9</strong></td>
<td>123.3</td>
<td>125</td>
<td>33.3</td>
</tr>
</tbody>
</table>

In this section, we propose techniques for applying clock gating to the energy recovery clocking system in order to obtain additional power savings in the idle mode. All the results presented in this paper are obtained in a 0.25-μm CMOS technology with the supply voltage of 2.5 V and at room temperature.

The energy recovery clocked flip-flops (see Figs. 1 and 3–5) cannot save power during sleep mode if the clock is still running. There are two components of power dissipation inside flip-flops: internal clock circuit power (power of logic gates connected to the clock) and the remaining circuit power (power of the rest of the flip-flop circuit). We separated the clock circuit power from the remaining circuit power in our power measurements. Disabling the clock circuit (inverter gates connected to the clock input in Figs. 3–5) can eliminate both the clock circuit and remaining circuit power. Hence, disabling of the inverter gates is the proposed approach to implementing clock gating inside energy recovery clocked flip-flops. This can be done by replacing the inverter gate with a NOR gate as shown in Fig. 15. Notice that this clock gating approach is not applicable to the SAER flip-flop since it does not use an inverter in the clock path.

Fig. 15(a) shows SCCER with clock gating. Clock gating was implemented by replacing the inverter with a NOR gate. The NOR gate has two inputs: the clock signal and the enable signal. In the active mode, the enable signal is low so the NOR gate behaves just like an inverter and the flip-flop operates just like the original flip-flop. In the idle state, the enable signal is set to high which disables the internal clock by setting the output of the NOR gate to be zero. This turns off the pull down path (MN2) and prevents any evaluation of the data. Hence, not only the internal clock is stopped (clock power saving) but also all the internal switching is prevented (power saving on the remaining circuit). Typical waveforms for SCCER flip-flop with clock gating are shown in Fig. 16. A similar clock gating approach is applicable to other energy recovery clocked flip-flops. Fig. 15(b) and (c) show the SDER and DCCER with clock gating, respectively.

Process variations (threshold voltage variations) can result in delay variations of flip-flops. We have compared the delay sensitivity to threshold voltage variation between square-wave and energy recovery clocked flip-flops as shown in the last column of Table III. The maximum delay variation is measured across the slow-slow (SS) and fast-fast (FF) process corners. Our results show that the proposed energy recovery clocked flip-flops not only remain functional across process corners, but also they show comparable or slightly less delay sensitivity to process variation compared to square-wave clocked flip-flops.

V. ENERGY RECOVERY CLOCK GATING

We target further reducing the clock power in idle periods by the application of the clock gating technique to the energy recovery clock. Clock gating is a well known idea that is applied to square wave clock systems to reduce power in idle states [10].
and clock gated flip-flops. It is observed that the clock gating does not introduce any power overhead. This is because of the use of small transistors in the NOR gates and also reduction in the short circuit power dissipated on the logic gates connected to the sinusoidal clock (the NOR gate shows less short circuit power than the inverter gate due to larger stack of transistors).

Table V shows results for the power consumed during the sleep mode for 50% data switching activity. Power savings of more than 1000 times are obtained during the idle state when compared to the power consumed without clock gating. The power savings increase with increase in the data switching activity.

Table VI shows delay comparisons between the original flip-flops and the flip-flops with clock gating. The results show that the clock gating addition has no impact on setup and hold time of the flip-flops. The delay overhead is caused by increase in the clock to output (clk-Q) delay. The overhead in the data to output (D-Q) delay is less than 6.3%.

VI. ENERGY RECOVERY CLOCKED PIPELINED MULTIPLIER

To demonstrate the feasibility and effectiveness of the proposed energy recovery clocking scheme and flip-flops, a pipelined array multiplier has been designed using the proposed clocking scheme. The multiplier is a 64 x 64-bit array multiplier, pipelined in 8 stages with the SCCER flip-flops as pipeline flip-flops. The multiplier was pipelined into 8 stages, with the inputs and outputs sampled, which required 9 rows of flip-flops for pipelining. The rows of flip-flops were spaced evenly across the multiplier, which was broken up into diagonal sections, so that horizontal and vertical paths across the multiplier were equally divided. The design has a total of 607 flip-flops. The clock inputs of all the flip-flops are connected together through an H-tree type of clock across an area of 2 mm x 1.2 mm. Wide metal 5 and 4 layers are used for the clock tree to reduce the resistance of the clock tree which is the limiting factor in terms of maximum clock frequency for distributing an energy recovery clock. The RC distributed model of the clock tree was extracted to make sure that the sinusoidal clock signal propagates properly through the clock network with minimal amplitude degradation at the final nodes of the clock tree at a target clock frequency of 200 MHz. The logic part of the design is composed of AND and full-adder gates. The design was custom laid-out in the TSMC 0.25-μm CMOS process. A similar multiplier has been designed using transmission gate flip-flops and square-wave clock. The clock tree in this multiplier was also H-tree; however, buffers were inserted to properly propagate the square-wave clock through the clock network.

We also integrated an on-chip ring oscillator for generating the square-wave clock. The oscillator is a voltage controlled oscillator as shown in Fig. 17, providing the flexibility of changing and adjusting the clock frequency. This voltage controlled oscillator is based on current-starved inverters [9]. According to the simulations, changing the adjust voltage (Vadj) from 0 to 5 V, the oscillating frequency varied from dc to 1.2 GHz. This oscillator provides a square-wave clock with 50% duty cycle which is directly used for the square-wave multiplier. The generated clock
is also sent to a clock divider (divide-by-8) and sent off-chip. By off-chip monitoring of the divide-by-8 clock, the high frequency clock of the on-chip oscillator can be adjusted.

The reference pulse (REF) required for the resonant energy recovery clock generator [see Fig. 11(a)], is also generated on-chip by a pulse generator as shown in Fig. 18. The pulse generator generates short pulses at rising edges of the square-wave clock. The pulse width is adjusted by adjusting the delay of the delay element using the adjust voltage (Vadj_pulse). The delay element is also based on current-starved inverters [9].

The buffers and driver of the resonant energy recovery clock generator [see Figs. 11(a) and 19] are also integrated on chip; however, the inductor is connected off-chip. The oscillator and pulse generator are devoted a separate power supply to minimize the effect of supply noise from the logic part on the delay (frequency) of the oscillator and the delay (pulse width) of the pulse generator. The supply of the buffers of the resonant clock generator is separate to easily measure the power overhead associated with the generation of the energy recovery clock. Moreover, in each multiplier, the power lines of flip-flops, logic, and clock buffers (in the case of square-wave) were separated and connected to separate pads to easily measure each component of the power.

The inputs to the multipliers are generated by a 21-bit linear feedback shift register (LFSR) integrated on chip. The LFSR provides a pseudo-random pattern for testing the multipliers. The LFSR was chosen based on the ability to be loaded with all 1’s and quickly go into a cycle of patterns which exhibit a roughly similar number of 0’s and 1’s to the inputs. In this way, the inputs to the multipliers are fairly random and are not biased to either 0’s or 1’s. The outputs of the LFSR drive groups of three or four signals for each 64-bit input.

VII. TEST AND MEASUREMENT RESULTS

The two multipliers along with the LFSR, ring oscillator, pulse generator, and the energy recovery clock driver were integrated in a test chip and fabricated in TSMC 0.25-μm CMOS process. Fig. 19 shows the die photo of the chip. A special input/output (I/O) pad was designed for connecting the off-chip inductor to the clock tree of the energy recovery clocked multiplier. In order to minimize the length of bonding wire and associated parasitics to the clock tree of the energy recovery clocked multiplier, it was selected to be ceramic, LCC52. This package is easy to test and also provides small cavity size that helps to reduce the length of bonding wire and associated parasitics. It is important to minimize these parasitics because they limit the maximum resonant frequency of the energy recovery clock generator. In order to further minimize the parasitics, a printed circuit board (PCB) was designed for mounting the package and connecting it to the test instruments. Off-chip decoupling capacitors were added to power supplies to stabilize the supply voltages.

The maximum resonant frequency of 160 MHz was achieved by using no off-chip inductor (L = 0, clock pin is tied directly to Vdd/2). This means that the operating frequency was limited by parasitics associated with packaging and bonding wires. This also implies that for further increase in frequency, an on-chip integration of the inductor needs to be considered. With an on-chip inductor, we could achieve smaller inductances and therefore higher frequencies; however, due to poorer quality of on-chip inductances the energy efficiency would not be better than off-chip inductance. Nonetheless, the main goal here is to compare the power dissipation of the two multipliers at the same frequency. Fig. 20 shows typical measured waveforms of the generated energy recovery and square wave clock signals.

Fig. 21 shows the power breakdown of the multipliers obtained by measurements at the clock frequency of 160 MHz. In one mode [see Fig. 21(a)], the LFSR is reset and inputs to the multipliers do not change. The power measured in this mode corresponds to zero data switching activity. In this case [see Fig. 21(a)], the logic power is negligible. In another mode, the power is measured when the LFSR runs and generates pseudo-random patterns [see Fig. 21(b)]. The logic power is the same.
between the two multipliers because of the same design and data pattern. The energy recovery clocking scheme reduces the clock tree power by more than 70% compared to the square-wave clocking. The measured clock tree power of the energy-recovery clocked multiplier includes the power associated with the buffers of its clock tree. The power saving on flip-flops varies between 68% and 39% depending on the data switching activity. The saving at lower data switching activities is more because of the conditional capturing property of the SCCER flip-flop. Compared to the square-wave clocked multiplier, the energy-recovery clocked multiplier shows overall power savings of 25%–69% depending on data switching activities. The results demonstrate the effectiveness of the proposed energy recovery clocking scheme for low-power applications.

**VIII. CONCLUSION**

We proposed four novel energy recovery clocked flip-flops that enable energy recovery from the clock network, resulting in significant total energy savings compared to the square-wave clocking. The proposed flip-flops operate with a single-phase sinusoidal clock, which can be generated with high efficiency. We implemented 1024 proposed energy recovery clocked flip-flops through an H-tree clock network driven by a resonant clock-generator, generating a sinusoidal clock. Simulation results show a power reduction of 90% on the clock-tree and total power savings of up to 83% as compared to the same implementation using conventional square-wave clocking scheme and flip-flops. We applied clock gating to energy recovery clocked flip-flops. Clock gating in energy recovery clocked flip-flops result in significant power savings during the idle state of the flip-flops without any considerable overhead compared to the original flip-flops. We fabricated and tested an energy recovery clocked pipelined multiplier with an integrated resonant clock-generator, generating a sinusoidal clock. Results show a power reduction of 70% on the clock-tree and total power savings of 25%–69% as compared to the same multiplier using conventional square-wave clocking scheme and corresponding flip-flops. The results demonstrate the feasibility and effectiveness of the energy recovery clocking scheme in reducing total power consumption.

**REFERENCES**


Hamid Mahmoodi (S’00–M’06) received the B.S. degree in electrical engineering and the M.S. degree in electrical and computer engineering from Iran University of Science and Technology, Tehran, Iran, in 1998 and 2000, respectively, and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, in 2005.

He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, School of Engineering, San Francisco State University, San Francisco, CA. His research interests include low-power, robust, and high-performance circuit design for nano-scale technologies. He has many publications in journals and conferences and several patents pending.

Prof. Mahmoodi was a recipient of the 2006 IEEE Circuits and Systems Society VLSI Transactions Best Paper Award and the Best Paper Award of the 2004 International Conference on Computer Design. He is a technical program committee member of IEEE Custom Integrated Circuits Conference and International Symposium on Quality Electronics Design.

Matthew Cooke received the B.S. and M.S. degrees in electrical engineering from Purdue University, West Lafayette, IN, in 2002 and 2004, respectively.

Between 1999 and 2002, he participated in a formal co-op with IBM Microelectronics Division working in several test and design groups. In 2004, he joined AMD, Austin, TX, where he is currently a Circuit Design Engineer. He has two pending U.S. patents. His research interests include low-power, variation-tolerant, and area-optimized circuits.

Kaushik Roy (S’90–M’90–SM’90–F’02) received the B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana-Champaign, in 1990.

He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, where he worked on FPGA architecture development and low-power circuit design. He joined the Department of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, in 1993, where he is currently a Professor and holds the Roscoe H. George Chair in Electrical and Computer Engineering. His research interests include VLSI design/CAD for nano-scale Silicon and non-Silicon technologies, low-power electronics for portable computing and wireless communications, VLSI testing and verification, and reconfigurable computing. He has published more than 400 papers in refereed journals and conferences, holds 8 patents, and is coauthor of two books on low power CMOS VLSI design.

Dr. Roy was a recipient of the National Science Foundation Career Development Award in 1995, the IBM Faculty Partnership Award, the ATT/Lucent Foundation Award, the 2005 SRC Technical Excellence Award, the SRC Inventors Award, the Best Paper Awards from the 1997 International Test Conference, the IEEE 2000 International Symposium on Quality of IC Design, the 2003 IEEE Latin American Test Workshop, the 2003 IEEE Nano, the 2004 IEEE International Conference on Computer Design, the 2006 IEEE/ACM International Symposium on Low Power Electronics and Design, the 2005 IEEE Circuits and System Society Outstanding Young Author Award (Chris Kim), and the 2006 IEEE Transactions on VLSI Systems Best Paper Award. He is a Purdue University Faculty Scholar, the Chief Technical Advisor of Zenasis Inc., and Research Visionary Board Member of Motorola Labs (2002). He has been on the editorial board of IEEE Design and Test, IEEE Transactions on Circuits and Systems—I: Regular Papers, and IEEE Transactions on Very Large Scale Integration (VLSI) Systems. He was Guest Editor for a Special Issue on Low-Power VLSI in the IEEE Design and Test (1994), the IEEE Transactions on Very Large Scale Integration (VLSI) Systems (June 2000), and the IEE Proceedings—Computers and Digital Techniques (July 2002).

Vishy Tirumalashetty received the B.S. degree in electrical engineering from JNT University, Hyderabad, India, in 2005, and the M.S. degree in electrical engineering from San Francisco State University, San Francisco, CA, in 2007.

He was a Research Assistant and a Graduate Teaching Assistant with San Francisco State University. He has interned with the Industrial Assessment Center, a Department of Energy sponsored program, from 2005 to 2007. He is currently an Energy Engineer with Itron Inc., Oakland, CA.