A Low-Power SRAM Using Bit-Line Charge-Recycling

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Abstract—Low-power SRAM design is crucial since it takes a large fraction of total power and die area in high-performance processors. Reducing voltage swing of the bit-line is an effective way to save the power dissipation in write cycles. Voltage swing reduction of bit-lines is, however, limited due to possible write-failures. We propose a new low-power SRAM using bit-line Charge Recycling (CR-SRAM) for the write operation. In the proposed write scheme, differential voltage swing of a bit-line is obtained by recycled charge from its adjacent bit-line capacitance, instead of the power line. Applying such a charge recycling technique to the bit-line significantly reduces write power. A test chip with 32 Kbits (256 rows x 128 columns) is fabricated and measured in 0.13 μm CMOS to demonstrate operation of the proposed SRAM. Measurement results show 88% reduction in total power during write cycles compared to the conventional SRAM (CON-SRAM) at V_{DD} = 1.5 V and f = 100 MHz.

Index Terms—Charge-recycling, low power, process variation, SRAM, write margin, write power.

I. INTRODUCTION

CONSIDERABLE attention has been paid to the design of low-power and high-performance SRAMs as they are critical components in both handheld devices and high-performance processors. Read-cycle power consumption is kept low by limiting the swing of the bit-lines, but write-cycle power consumption remains quite large due to the full swing nature of the bit-lines during the write operation. As systems become more complex, SRAMs tend to have larger number of bits per word. In this type of SRAM, the active power is dissipated mainly by charging and discharging of the highly capacitive bit-lines.

Reducing voltage swing on the bit-lines is an effective way to reduce the power dissipation in write cycle. Recently, a low-power SRAM using a sense amplifying cell (SAC-SRAM) has been reported that reduces write power by reducing the voltage swing on bit-lines [1]. In this scheme, however, it is difficult to further reduce the write power since reducing voltage swing of bit-lines is limited by possible write failures under process variations. For stable write operation in SAC-SRAM, the amplitude of voltage swing of the bit-line should be greater than a marginal value to be able to invert the state of the internal nodes of the SRAM cell in write operation. A low-power SRAM using hierarchical bit-line and local sense-amplifiers (HBLSA-SRAM) has been reported to reduce write power consumption in bit-lines [2]. However, HBLSA-SRAM needs local sense-amplifiers in each SRAM sub-arrays and results in additional area overhead. In addition, SRAM design using this technique is complex because it requires optimization of SRAM sub-array size for proper power and memory area.

In this paper, a new write scheme is proposed for low-power SRAM which uses both low voltage swing and charge-recycling (CR) [3], [4] on bit-line. In the proposed write scheme, low voltage swing of each bit-line is obtained by the recycled charge from the adjacent bit-line capacitance, instead of the
power line. In order to improve the data retention capability of unselected SRAM cells during write cycle, the power supply lines of memory cells in a column are connected to each other and separated from the other column’s power lines. By separately applying the power supply lines of one column from other column’s supply power line, we improved the data retention capability for unselected SRAM cells during write cycle. We have also investigated CR-SRAM write stability under process variations. Experimental results show that it is possible to successfully write using the proposed write scheme without any write-failure by limiting the number of charge-recycling bit-line pairs. A prototype 32 Kbits (256 rows x 128 columns) CR-SRAM is implemented in IBM 130 nm CMOS technology and it exhibits write power dissipation of 192 µW with 1.5 V supply at 100 MHz. A 32 Kbits CON-SRAM array (256 rows x 128 columns) without charge-recycling was also implemented to compare the SRAM write power. Experimental results show that the proposed write scheme can reduce total power by 88% during write cycles compared to that of conventional SRAM. To summarize, this paper makes the following contributions.

- We propose a new low-power SRAM based on a bit-line charge-recycling method. To the best of our knowledge, this is the first time that CR concept has been directly applied to the bit-line to reduce dynamic write power associated with bit-line swing in SRAMs.
- By isolating the selected SRAM cells from power supply lines during write operation, we could successively apply the charge-recycling method to bit-lines and achieve a low-power SRAM. Measurement results show that the proposed SRAM achieves a total power reduction of 88% during write cycles compared to the conventional SRAM.

The rest of the paper is organized as follows. In Section II, the write scheme using CR is proposed. In Section III, we present the power comparison of CON-SRAM and CR-SRAM, and...
present write immunity under process variation. In Section IV, we present the measurement results. Finally, conclusions are drawn in Section V.

II. Charge-Reycling Architecture

Active power in a conventional full-swing write scheme is dissipated mainly by high charging and discharging currents in bit-lines. Reducing voltage swing on the bit-line is an effective way to reduce power dissipation in write cycles. Low voltage swing bit-line in write cycles has been reported in [1], [5], [6]. In these schemes, however, it is difficult to further reduce the write power because the probability of write-error greatly increases as the voltage swing is reduced. In order to further reduce the active power in write cycles, we propose a new write scheme using CR method in which the previously used charge on a bit-line is reused on the adjacent bit-line for creating a low voltage swing.

The rest of the section is organized as follows. First, we explain the concept of SRAM write scheme using CR method to reduce active power of bit-lines in write cycle. Second, we will explain the power control circuitry which is introduced to improve the data retention capability during write operation. Third, we will discuss the SRAM mode change between read and write cycles in the proposed scheme. Finally, we will describe the implementation of CR-SRAM based on the proposed write scheme.

A. Concept of SRAM Writing Using Bit-Line Charge-Reycling

Fig. 1(a) shows a simplified circuit diagram to illustrate the concept of CR-SRAM. A bit-line pair is composed of a bit-line (BL) and a complementary bit-line (BLB). In Fig. 1(a), we assumed that the number of CR bit-line pairs, N, is 2. The simplified write circuit using CR is composed of two bit-line pairs, two exchangers and five switches connected in series which are controlled by EV and EQ signals. DIN1 and DIN2 in Fig. 1(a) represent input data to be written to the cell and determine the switch connections between a bit-line pair and the neighboring bit-line pairs. Each exchanger has four switches (two S switches and two P switches). The exchanger is shown in Fig. 1(b) in more detail. All switches in exchanger are implemented using transmission-gates. If DIN is high, switch P’s are connected and switch S’s are disconnected, while if DIN is low, switch P’s are disconnected and switch S’s are connected. It can be noted that the switches P and S in exchanger determine whether the bit-line and complementary bit-line will be directly or cross-connected to the neighboring bit-line pair depending on input data.

The SRAM write operation in the proposed scheme is performed in the equalization and the evaluation modes. In equalization mode, two bit-lines in a bit-line pair are pre-charged to a common voltage. This common voltage is established by consecutive charge-recycling write operations. In evaluation mode, two bit-lines in a bit-line pair have different voltages. In order to explain the concept of charge-recycling, the equivalent switch connections along with bit-line voltage levels for equalization and evaluation modes are displayed in Fig. 2. Fig. 2(a) shows the switch connections during equalization mode for EV = “0”, EQ = “1”, and input pattern of two-bit data (DIN1DIN2) to be written is “01.” In Fig. 2(a), we assumed that the common voltages (3/4VDD and 1/4VDD) [3], [4] are established by consecutive charge-recycling write operations. When the SRAM operation changes from read to write cycle, these common voltages are initially given by the reference generation circuit, and this point will be discussed in more detail in Section II-C. When

![Fig. 3. Voltage waveforms illustrating concept of charge-recycling on bit-lines with N = 2 in CR-SRAM.](image-url)
SRAM is in equalization mode, all connections between bit-line pairs, which are predetermined by input data, are disconnected and two bit-lines in each bit-line pair are connected by an EQ signal. The two bit-lines in the bit-line pair with different voltages share their charges and their voltage becomes the average of the two values. If we assume that the number of CR bit-line pair is \( N \), all bit-lines have the same capacitances, and \( i = 1, 2, \ldots, N \), the voltage in the \( i \)th bit-line pair becomes \([2 \cdot N - 2 \cdot i + 1]/(2 \cdot N)\) \( \times V_{DD} \) [3], [4]. When the SRAM is in evaluation mode, two bit-lines in each bit-line pair are disconnected and all bit-lines are connected to bit-lines in the neighboring bit-line pair by an EV. A bit-line and its neighboring bit-line are connected by predetermined input data. Fig. 2(b) and Fig. 2(c) show the switch connections during evaluation mode for \( EV = \text{“1”} \), \( EQ = \text{“0”} \), and input data patterns \((DIN_1, DIN_2)\) to be written are \text{“01”} and \text{“10”}, respectively. When the input data is high, the bit-line is connected to the neighboring bit-line pair with higher voltage and the complementary bit-line is connected to the neighboring bit-line with lower voltage. They share their charges and their voltage becomes the average of the two values. Thus, the common voltage \( 1/2 \cdot V_{DD} \) in Fig. 2(b) is the averaged voltage value of \( V_{BL1} (3/4 \cdot V_{DD}) \) and \( V_{BL2} (1/4 \cdot V_{DD}) \) in Fig. 2(a). At this time, two bit-lines in a bit-line pair have different voltages by connecting the neighboring bit-lines. As a result, the \( i \)th bit-line pair has a voltage difference \( \Delta V \) of \((1/N) \cdot V_{DD} \) [3], [4]. If input data is written as high, the voltage of the bit-line becomes \((1/N) \cdot V_{DD} \) higher than that of the complementary bit-line. On the contrary, if input data is low, the voltage of bit-line becomes \((1/N) \cdot V_{DD} \) lower than that of the complementary bit-line. Using the \((1/N) \cdot V_{DD} \) voltage difference between bit-line pair, we can write data into SRAM cell. It can be noted from Fig. 2(c) that the bit-line BL1, which is in the left bit-line pair and must be connected to the neighboring bit-line pair with the higher voltage, is connected to \( V_{DD} \). On the contrary, the bit-line BL2 in Fig. 2(c), which is in the right bit-line pair and must be connected to the neighboring bit-line pair with lower voltage, is connected to ground.

Fig. 3 shows voltage waveforms when two-bit input data \((DIN_1, DIN_2)\) changes from \text{“01”} to \text{“10”} \( V_{Q1} \) and \( V_{QB1} \) in Fig. 3 represent the internal node voltages in the SRAM cell. Through the charge sharing between bit-lines in the same bit-line pairs and in the different bit-line pairs during equalization and evaluation, respectively, the charge used in the left bit-line is recycled in the right bit-line pair in the next clock cycle, as shown in Fig. 3. In this scheme, the charge of bit-line can be recycled again and again by rolling down to the lower adjacent bit-line pair in every cycle, until this charge reaches ground. If the number of CR bit-line pair is \( N \), the bit-line charge in the left bit-line pair is recycled \( N \) times through \( N \) bit-line pairs from \( V_{DD} \) to ground. When a group has \( N \) bit-line pairs and bit-line capacitance is \( C_{BL} \), the \( N \) bit-line pairs consume the power of \((1/N) \cdot C_{BL} \cdot V_{DD}^2 \) per clock cycle instead of \( N \cdot C_{BL} \cdot V_{DD}^2 \). The power saving ratio of the

![Diagram](image)

**TABLE I**

<table>
<thead>
<tr>
<th>WE</th>
<th>COL[n]</th>
<th>V_{DDM}[n]</th>
<th>V_{SSM}[n]</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>( V_{DD} )</td>
<td>( V_{SB} )</td>
<td>Retention</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>( V_{DD} )</td>
<td>0</td>
<td>Read</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>( V_{DD} )</td>
<td>( V_{SB} )</td>
<td>Retention</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Hi-Z</td>
<td>Hi-Z</td>
<td>Write</td>
</tr>
</tbody>
</table>
bit-lines in the CR-SRAM becomes $1/N^2$ [3]. As $N$ increases, the power saving in the CR-SRAM drastically increases.

**B. Power Control Circuit for Charge-Recycling**

In order to increase power saving and ensure a write using CR, the charge loss due to bit-line leakage current should be minimized. Because the bit-line leakage current reduces the voltage swing between bit-line pair during write operation and hence, causes the degradation of write stability. The bit-line leakage current including SRAM cell leakage current can be simply reduced by increasing the source-line voltage from $V_{SS}$ to $V_{SB}$ due to the increased reverse body bias of access transistors [7], [8]. In the proposed scheme, we adopted the source-biasing scheme (SB-SRAM) [7], [8] in which the source-line, connected to the source terminals of the driver MOSFETs, is controlled, so that it is zero or has a positive bias voltage $V_{SB}$ according to SRAM operational mode.

To be able to write a data into SRAM cell using low-voltage swing on bit-lines, the SRAM cell should be isolated from power sources ($V_{DD}$ and $V_{SS}$) during CR while the word-line is activated [9]. The isolation of the word-line activated SRAM cells from power sources (floating) during a write cycle, however, decreases the data retention stability particularly for the SRAM cells of unselected columns [9]. The word-line activated SRAM cells become largely unstable when the supply voltages of SRAM cells are in floating states, and the data in these SRAM cells are easily destroyed. In order to improve the data retention stability of the unaccessed SRAM cells during a write operation, we make the SRAM cells to be floating only in the selected columns. By introducing the column-based power-line control [9], we can improve the data retention capability for the memory cells which are not selected to be written. We will discuss about the data retention capability during write operation in more detail in Section III-C. Fig. 4(a) illustrates the key structure of the technique. The power lines ($V_{DD}$ and $V_{SS}$) of memory cells in a column are connected to each other and separated from the other columns. The $V_{DDM}[n]$ and $V_{SSM}[n]$ are connected to $V_{DD}$ and $V_{SB}$ (or $V_{SS}$) by power switches of $SN[n]$, $SP1[n]$, and $SP2[n]$. These power switches are controlled by the write enable signal WE and column selection signal $COL[n]$, and it is turned off when the memory cell in the column is accessed for writing, and $V_{DDM}[n]/V_{SSM}[n]$ change to a floating state. The isolation of SRAM cell from power lines also results in significant leakage reduction on idle cells.

Fig. 4(b) and Table I show the timing diagram and truth table of control circuit in write/read cycles based on proposed write scheme. The control signals $V_{UP}[n]$ and $V_{DN}[n]$ are synchronized with the nth column selection signal $COL[n]$, and the power switches ($SN[n]$, $SP1[n]$, and $SP2[n]$) are turned off when $COL[n]$ becomes high in write-cycle (WE = “1”). After $COL[n]$ become low, both $V_{UP}[n]$ and $V_{DN}[n]$ go back to low, $V_{DDM}[n]$ and $V_{SSM}[n]$ become $V_{DD}$ and $V_{SB}$, and small swing data is amplified to $(V_{DD} - V_{SB})$ swing inside a cell. The cycle time can be divided into three parts depending on whether write enable signal WE and column selection signal $COL[n]$ are high or low. When $COL[n]$ is low, the SRAM maintains the data retention mode irrespective to the status of WE since the virtual $V_{SS}$ and $V_{DD}$ line voltages ($V_{SSM}[n]$, $V_{DDM}[n]$) become $V_{SB}$ and $V_{DD}$, respectively, and the cell stores the data at a reduced voltage swing of $(V_{DD} - V_{SB})$. When $COL[n]$ and WE are high, both $V_{SSM}[n]$ and $V_{DDM}[n]$ are in floating states (Hi-Z) and SRAM is in write mode. Note that the column selection signal $COL[n]$ should switch to “0” after the word-line is turned off to ensure successful write to a cell. When $COL[n]$ and WE is high and low, respectively, $V_{SSM}[n]/V_{DDM}[n]$ become $V_{SS}/V_{DD}$, and SRAM is in the read mode.

**C. Mode Change Between Read and Write Cycles**

There are several differences between conventional (COND- SRAM) and the proposed SRAM (CR-SRAM). In the proposed
SRAM, bit-lines have different voltage levels during write cycle determined by the charge-recycling operation. This fact requires a special design consideration to transition between read and write cycles. In the read cycle, all bit-lines are pre-charged to \( V_{DD} \). When the cycle changes from read to write, bit-line voltages need to be preset to their write voltage levels that would normally be obtained after several consecutive charge recycling write operations. We address this issue by generating the set of voltage levels needed to initialize bit-lines upon transition from read to write. Fig. 5(a) shows the pre-charge configuration to write when \( EV = 0 \), \( EQ = 1 \), \( PW = 1 \), \( DIN_1 = 0 \), \( DIN_2 = 1 \), and \( N = 2 \). When the operation mode changes from read to write, the initial node voltage of \( V_{H1}/V_{L1} \) and \( V_{H2}/V_{L2} \) are preset to \( V_{REF1} \) and \( V_{REF2} \) respectively by switching \( PW = 1 \). The \( V_{REF1} \) and \( V_{REF2} \) are given by \((2 \cdot N - 2 \cdot i + 1) \times V_{DD})/(2 \cdot N)\), when \( N \) is the number of charge-recycling bit-line pair, and \( i = 1, 2, \ldots , N \). When \( N = 2 \) and \( V_{DD} = 1.8 \) V at 180 nm node technology, the values of \( V_{REF1} \) and \( V_{REF2} \) are 1.35 V and 0.45 V, respectively. Fig. 5(b) shows the reference generation circuit for write pre-charge when mode changes from read to write. The PW signal is activated only once when mode is changed from read to write. If the PW is switching to an off-state, all the power-lines of reference generation circuit are cut-off state. Since these initial start-up reference voltages are required only upon transition from read to write cycle, the power overhead of the start-up circuit including reference voltage sources is negligible.

### D. Implementation of CR-SRAM

Fig. 6 shows the CR-SRAM structure with \( N = 2 \) and 4:1 column selection MUX (number of column decoder output = 4). The CR-SRAM is composed of a column/row driver, interface signal generator, power control circuit, and M-grouped blocks. M-grouped blocks in Fig. 6 are sub-arrays and each grouped block has a column driver and \((N_X \times \text{number of column decoder output})\) bit-line pairs. Each column driver has \( N \) and \((N + 1)\) switches which are controlled by \( EQ \) and \( EV \) signals, respectively. When the input data is high, the bit-line and complementary bit-lines are connected to the neighboring bit-lines with higher and lower voltage, respectively. The bit-line, which is in the left bit-line pair in a group, is connected to \( V_{DD} \). The complementary bit-line, which is in the right bit-line pair, is connected to ground. On the contrary, when the input data is low, the bit-line and complementary bit-line are connected to the neighboring bit-lines with lower voltage and higher voltage, respectively.

### III. Simulation Results and Comparisons

In order to verify the effectiveness of proposed SRAM in scaled technologies [10], we will evaluate the power consumptions and SRAM stability using predictive technology models (PTM) [11] assuming the memory array size of 256 rows \( \times \) 256 columns and column decoder size of 4. In Section III-A, we will evaluate the SRAM power dissipations with read/write operations, technology nodes, and frequencies. In Section III-B, we will evaluate the write stability for process variations. The data retention capability during write operation will be investigated in Section III-C. Finally, in Section III-D, we will investigate the read/hold SNM and write margins.
A. Writing Power Comparison of CR-SRAM

The power dissipation of the proposed SRAM is simulated using a 0.18 μm predictive technology model [11]. The NMOS/PMOS threshold voltages of 400 mV/–420 mV with a 1.8 V supply voltage ($V_{DD}$) and a 0.4 V source line voltage ($V_{SB}$) were used in simulation. Fig. 7 shows a simulated waveforms when read cycle = 50% and write cycle = 50% in 4-stacked bit-line pairs ($N = 4$) at 100 MHz. When $WE$ switches to high, SRAM switches to the write cycle and the initial start-up signal $PW$ is activated to preset the voltages of the bit-lines. Then, the voltages of the bit-lines are maintained by charge-recycling operation. Fig. 7 also shows the waveforms when SRAM mode changes from write to read cycle. When the mode changes from read to write, the bit-lines are pre-charged to $V_{DD}$ and SRAM begins to read the stored data.

Fig. 8(a) shows the power comparison of CR-SRAM and CON-SRAM for several write/read (W/R) cycle patterns. W/R’s in Fig. 8(a) represents the ratio of numbers of write to read cycles during 10 cycles. For example, 80/20 represents 8 read and 2 write cycles during 10 cycles. In each scenario, the number of mode changes from read to write (or write to read) is once during 10 cycles, except 50/50. The number of mode changes of 50/50 is five during 10 cycles. The total power includes leakage power of SRAM array, row driver power, power of control circuit for charge-recycling, and column driver power. The column driver power includes power dissipation due to charging/discharging of bit-line (write power), power dissipations in the circuits for read/write, pre-charge to read and pre-set to write. The power dissipation in row driver includes the dissipated power in row-decoder, and word-line buffers. The power dissipation in control circuit includes the dissipated power in interface circuits generating control signals such as WE, SAE, EV, EQ, and PW. In this comparison, we assumed that the bit-line of a CON-SRAM has full voltage swing of $V_{DD}$. The leakage power is negligibly small and the most power in CON-SRAM is dissipated in column driver by dynamic power due to full-swing.

By using the CR method, the power dissipation of CR-SRAM is reduced to 7.7% that of CON-SRAM (92.3% power reduction) during write cycles ($W/R = 100/0$). Fig. 8(b) shows the comparison of power consumption under write cycle with number of bit-line pair $N$ in a group of SRAM. As $N$ increases, the total power dissipation of CR-SRAM decreases to 27.4% ($N = 2$), 7.7% ($N = 4$), 6% ($N = 6$) and 4.8% ($N = 12$) compared to CON-SRAM.

We have investigated the impact of technology scaling on the total power savings of proposed scheme in 256 rows × 256 columns array. Fig. 9 shows the comparisons of CR-SRAM with CON-SRAM in total power consumption for different technology nodes. The power supply voltages used in this study are 1.8 V, 1.6 V, 1.4 V, and 1.2 V for 180 nm, 130 nm, 100 nm and 70 nm, respectively. As the transistor size is more scaled down, the leakage power of SRAM becomes more important. For 70 nm technology node, the leakage component of CON-SRAM is 58% of the total power consumption and the proposed scheme reduces the total power by 94% compared to the conventional scheme.

Fig. 10 shows the power comparison for different clock frequencies in the 70 nm technology node, where leakage power
is also a significant portion of the total power. Results are obtained for the consecutive writing mode (W/R = 100/0). As the clock frequency increases from 10 MHz to 1 GHz, the dominant power changes from leakage power to write power. As compared to CON-SRAM, the power dissipation in CR-SRAM is reduced to 7.5%, 6.6%, and 6.5% at 10 MHz, 100 MHz and 1 GHz, respectively. The leakage reduction due to source biasing is also significant. From the results of Fig. 10, it is confirmed that the CR-SRAM can more effectively reduce the write power in higher operation frequencies where the dynamic power becomes a larger fraction of the total power.

**B. Write Immunity Under Process Variations**

Die-to-die and within-die variations in process parameters result in mismatch in the strength of different transistors in an SRAM cell, resulting in write failures [12], [13]. In the proposed write scheme, the power supply lines are floating during the time the word-line is high. Floating power supply lines (V_D and V_SS) in the memory cell assist the write operation because the floating power supply lines disable the driver nMOS and load pMOS of the cell [9]. In order to estimate the write immunity under process variations, we evaluate the maximum allowed mismatch in threshold voltages of SRAM cell transistors in the worst case direction (ΔV_TH) for the write operation. Fig. 11(a) shows the 6T-SRAM cell and the threshold voltage assignments in an SRAM cell when threshold voltage mismatch is worst case direction. Fig. 11(b) shows the maximum allowed worst case mismatch in threshold voltages (ΔV margin) for different number of bit-line pairs N. In the simulation, we assumed f = 100 MHz, T = 25 °C and V_DDR = 1.8 V, 1.6 V, 1.4 V, and 1.2 V in 180 nm, 130 nm, 100 nm, and 70 nm, respectively. As N increases, the acceptable range of ΔV_TH decreases because the voltage differential between bit-lines in a bit-line pair decreases at the rate of (1/N) x V_DDR. Smaller voltage differential between bit-lines in a bit-line pair reduces
the tolerance to threshold voltage variation in the write operation. If $N$ is 10 in 180 nm technology, the allowed maximum threshold voltage mismatch is about 71 mV which is still larger than $3\sigma_{V_{TH}}$ of threshold voltage variation [14]. In this estimation, the $\sigma_{V_{TH}}$ (threshold voltage variation) is borrowed from [14]. In this study, we define $N_{\text{MAX}}$ as the maximum number of $N$ for which the $\Delta V_{TH}$ margin is higher than the value of $3\sigma_{V_{TH}}$ for a given technology node. Fig. 11(c) shows $N_{\text{MAX}}$ for various technology nodes, and the values of $N_{\text{MAX}}$ are given by 11, 8, 7, and 5 at 180 nm, 130 nm, 100 nm, and 70 nm technology node, respectively. At 70 nm, the allowed $N$ is 5 and enough to save the dynamic power on bit-lines.

With the technology scaling, the random intra-die variation is expected to increase [14]. This makes the SRAM cells more vulnerable to failure. We have investigated the impact of technology scaling on the write failure. Fig. 12(a) shows Monte Carlo simulation of write failure with process variation in threshold voltage for different $N$ values. As $N$ increases, the number of write failure increases for a given process variation. Fig. 12(b) shows the total number of write failures with variation of threshold voltage for different technology nodes. The numbers of write failure increase with technology scaling due to the increase of threshold mismatch [14].

C. Data Retention Capability of Unselected Cells During Write Operation

We investigated the data retention capability for the unselected SRAM cells during write operation. In order to improve the data retention stability of the unaccessed SRAM cells during write operation, we make the SRAM cells to be floating only in the selected columns. The floating state of power line for the unselected SRAM cells has a negative impact on the data retention capability because it weakens the strength of nodes storing “1” or “0” due to isolation from power sources.
Fig. 13(a) shows SRAM cells when WL1 and COL[1] are selected. When WL3 and COL[1] are selected, the C1 and C9 cells are accessed to write. Since COL[1] is selected, the power lines of cell C5 and C13 are in floating state while the word-line is in off-state. In order to investigate the data retention capability of SRAM cells, we evaluated the maximum threshold voltage mismatch in the worst direction for the retention condition. Fig. 13(b) shows allowed threshold voltage mismatch for data retention of C5. As the transistor feature size is scaled down, the allowed threshold voltage mismatches in the worst direction decreases due to the higher leakage current of transistor during write operation. It is confirmed from Fig. 13(b) that data retention capability for an unaccessed cell C5 is high enough to hold the stored memory data during write cycles since allowed threshold voltage mismatch for data retention is higher than 165 mV at 70 nm technology, which is 1.83 times of $3\sigma_{V_{TH}}$, if $3\sigma_{V_{TH}}$ is assumed to be 90 mV [14].

**D. Read/Hold SNM, and Write Margin**

In this paper, the static noise margin (SNM) of the proposed scheme is compared with those of SB-SRAM and CON-SRAM. The static noise margin (SNM) is defined by Seevinck [15] as the minimum DC noise voltage necessary to change the state of a cell and can be estimated graphically as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve [15]. Fig. 14(a) and Fig. 14(b) show the results for read and hold SNM, respectively. The read and hold SNMs of CR-SRAM are degraded by 38% and 7% compared to CON-SRAM respectively. Because the supply voltage is degraded due to the voltage drop at power switches (SP1[n], SP2[n], and SN[n]) in Fig. 4(a)), the read- or hold-SNM are degraded due to reduced supply voltage level. Note that the read-SNM of a well-known SB-SRAM is also degraded by 34% compared to CON-SRAM due to the series connected nMOS switches. By incorporating the proposed scheme with the column-based dynamically switching of supply voltage level during read operation, it can be expected to improve the read-SNM [16].

We also investigated the write margin. The write margin is defined as the minimum bit-line voltage required to flip the state of the SRAM cell [17]. To write a cell, one of the bit-lines needs to be discharged close to the ground in order to flip the cell state. The ease with which a cell can be written depends on how close the bit-line needs to be driven to the ground. Therefore, the required low-level of bit-line voltage during write operation is an indicator of process variation. By evaluating the write operation with the different low-level of voltage swing in bit-line at a given speed, we can obtain write margin. Fig. 15(a) shows the minimum bit-line voltage to ensure writing a “0” (write margin). For comparison, we also included the write margin of power-line floating write technique (PF-SRAM) [9]. For all technology nodes, CR-SRAM has the largest write margin among other SRAM techniques. Fig. 15(b) shows the improvements of write margin. The write margins of SB-SRAM, FP-SRAM and CR-SRAM are improved by 12%, 20%, and 40% compared to that of CON-SRAM, respectively.
The large improvement of CR-SRAM in write margin can be interpreted as follows. The driver nMOS and load pMOS transistors of SRAM cell become inactive by floating supply lines ($V_{DD}$, $V_{SS}$), and this makes it easy to invert the SRAM node voltage during write operation [5], [9].

IV. MEASUREMENT RESULTS

A 32 Kbits (256 rows × 128 columns) SRAM test chip with the proposed writing scheme (CR-SRAM) was fabricated in a 0.13-$\mu$m IBM CMOS technology. The microphotograph of the test chip and layout showing the organization are shown in Fig. 16. The layout is consisted of row driver, column driver, SRAM array, and interface circuits. A conventional 32 Kbits SRAM (CON-SRAM) array (256 rows × 128 columns) without charge-recycling, i.e., full-swing writing was also implemented to compare the SRAM write power. The fabricated memory was measured at room temperature at different power supply voltages. In order to measure the powers of write and array leakage in CR-SRAM and CON-SRAM, power pins are assigned separately. Table II tabulates the measured test chip. The measured write powers are 162 $\mu$W (CR-SRAM) and 990 $\mu$W (CON-SRAM) at 100 MHz clock, respectively. The core area of the test chip including CON-SRAM is 0.765 mm$^2$ (0.90 mm × 0.85 mm). In HSPICE simulation, the maximum clock speed is 1.20 GHz.

The array leakage power of CR-SRAM is measured at $V_{DD} = 1.5$ V and 25 $^\circ$C while sweeping the source-bias voltage ($V_{SB}$) from ground to 1.5 V (Fig. 17). Leakage power savings becomes moderate for $V_{SB}$ above 0.4 V since the reduction in cell leakage levels off and junction leakage becomes a significant portion [18]. The measured leakage power of the 32 Kbits CR-SRAM at $V_{SB}$ of 0.4 V was 23.4 $\mu$W. This is only 5% compared to the array leakage without source-biasing SRAM.

We also measured the SRAM writing power separately from column driver. Fig. 18 shows the measured writing power of a CR-SRAM for various clock frequencies. The write power is more saved as the clock frequency increases since the power dissipation by charging and discharging of bit-lines becomes more dominant compared to the leakage power. When the clock frequency approaches 100 MHz, the total writing power saving is increased up to 87.1% for the conventional full-swing scheme.

Fig. 19 compares the measured total power dissipation of CR-SRAM with that of CON-SRAM. The power consumptions in each part of the SRAM are measured at 100 MHz under the write mode with a 1.5 V supply voltage ($V_{DD}$) and a 0.4 V source line voltage ($V_{SB}$). By applying the proposed CR technique, the total power dissipation in a CR-SRAM is reduced to 12% compared to CON-SRAM.

Fig. 20 shows the measured readout waveforms from data output buffer at 1.5 V $V_{DD}$ and 50 MHz clock frequency. The input data pattern is written in the SRAM chip during write cycles, and the output data pattern is loaded during read cycles.
V. CONCLUSION

This paper presents a low-power charge-recycling SRAM for battery-operated portable applications. By applying the charge recycling technique to the bit-lines, it is possible to effectively reduce the SRAM write power associated with charging and discharging of the highly capacitive bit-lines. The CR-SRAM with 32 Kbits array is implemented in IBM 130 nm CMOS technology and measurement results show 88% reduction in total power dissipation during write cycles compared to the conventional SRAM at $V_{DD} = 1.5$ V and $f = 100$ MHz. The proposed
CR-SRAM architecture is a promising candidate for embedded memory of battery operated portable applications.

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