ABSTRACT
Temperature and power are interrelated. With increase in temperature, power dissipation increases and vice versa. This paper analyzes the interdependency of power dissipation and temperature and also presents simulation results obtained by deriving the final power and temperature for nano-scale SRAM circuits with any environmental condition. Given the strong temperature dependence of BTI aging effects, accurate temperature estimation is an important step in determining the impact of aging effects on SRAM. As an example, the thermal estimation for a conventional SRAM and a power gated SRAM are performed to show the comparative impact of BTI aging effects on both the circuits.

I. INTRODUCTION
Many research papers have been discussed on junction temperature and how the maximum junction temperature is estimated [1], [2], and [4]. Dissipated power of any microchip is closely related to and is affected by the microchip’s temperature. For example, the dissipation of dynamic and leakage power increases the temperature of the microchip, which in turn increases the leakage power dissipation. The power and temperature interdependence is increasing in nano-scale due to increased leakage levels and the exponential dependence of leakage power on temperature. Moreover, in SRAM circuits, the total power consumption is dominated by leakage power as the majority of the SRAM cells are in idle state and dissipating only leakage power. So, it is essential for any power estimation methodology to include temperature in its estimates [1]. It has already been mentioned by many researchers that the junction temperature is a function of the ambient temperature; the junction to case, and case to ambient thermal resistances; and the power dissipation [2], [4] and [5]. The power consumption of high performance microchips increases with increase in temperature, due to increased leakage at higher temperature. To make sure the microchip operates in a normal safe way, we have to prevent it from gaining excessive heat. Even though, cooling materials such as thermal grease and heat sinks might help in removing the heat from the microchip that is always not the case.

Extreme temperature may lead to overheating and burning of the microchip instantly resulting in thermal runaway. As a result, the microchip may sustain irreversible damage. To better understand our research approach, we use a thermal estimation simulation framework to obtain steady-state power and temperature results. In this work, as an example, we estimated the junction temperature ($T_J$) of a six transistor (6T) static random access memory (SRAM) cell and a power-gated (7T) SRAM cell in the 32nm predictive CMOS technology [3] for different number of memory cells. A BTI aging model [7] is also used for estimating the aging effect on 6T and power-gated (7T) SRAM. To account for the threshold voltage ($V_t$ or $V_{th}$) variations, we took three different process corners into consideration which are the Low $V_t$, Nominal $V_t$, and High $V_t$ inter-die process corners. The temperature of the microchip varies due to the work load and environment experienced (ambient temperature). To account for the changes in the ambient temperature, we considered two different temperature levels: the low room temperature (25°C) and the worse case ambient temperature (50°C) for determining the Static Noise Margin (SNM) results.

The rest of the paper is organized as follows: Section II gives a brief description of the thermal estimation method that we used in our research. The circuit simulation to obtain the power is done in HSPICE and eventually a script language is used for estimating the final junction temperature and power. We highlight the main factors and variables that were important to be considered. Section III provides an overview of the BTI aging model used for $V_t$ shift estimation. Section IV is a case study
which is split into two different case studies giving detail descriptions about SRAM. The former being the conventional SRAM (6T) and the latter being a power gated SRAM. Section V shows the SNM results which are obtained by using the BTI model to find out the aging effect on SNM of 6T SRAM and the power gated SRAM when considering an array of billion transistor cells. After the aging effect is applied, we show how SNM impacts both the 6T and 7T SRAM. The important results for consideration are reported in both section IV and V. Finally, Section VI concludes the paper. At the end references are provided.

II. THERMAL ESTIMATION METHOD

Thermal estimation is a method used to calculate the junction temperature by considering the interdependence of power and temperature. Fig. 1 shows the algorithm model used for estimating the final junction temperature and power in an electrothermal analysis tool [4].

Initially, we assume values for initial junction temperature \( T_{\text{J,initial}} \), ambient temperature \( T_{\text{amb}} \), number of memory cells and junction-to-ambient thermal resistance \( R_{JA} \). In this research, we considered \( R_{JA} \) as 1°C/W for a chip scale package [6]. We start with the assumed value for the initial junction temperature and then find the standby (leakage) power of one memory cell \( (P) \) from HSPICE simulation by keeping the supply voltage \( \text{(Vdd)} \) at 0.9V. Since, in a large SRAM, the total chip power is dominated by leakage power and also the dynamic power which is not temperature dependent, we only consider leakage power in our analysis. Once we get the leakage power of one cell, the total chip power is estimated as the product of total number of memory cells and the power of one cell \( (P) \). We then estimate the junction temperature using the following equation:

\[
T_J = T_{\text{amb}} + \text{Memory_size} \times P \times R_{JA}
\]  

After this, the algorithm checks the difference between the initial junction temperature \( (T_{\text{J,initial}}) \) and the new estimated junction temperature \( (T_J) \) to see if the difference is less than 0.1%. If the temperature difference is more than 0.1%, the \( T_{\text{J,initial}} \) is updated with the new estimated \( T_J \) and the above process (power estimation at new temperature followed by temperature estimation) repeats. If the temperature difference is less than 0.1%, then we take the final junction temperature and power as the estimated chip junction temperature and power. In each iteration of the algorithm, we also check if the temperature is converging by comparing the estimated junction temperature with 200°C. If the estimated junction temperature is below 200°C, then it will concede as the next \( T_J \) which in turn will be used for the next iteration; otherwise, it is acknowledged as a thermal runaway. The thermal runaway limit is taken at 200°C because it is an upper limit on the temperature that a junction can achieve before it starts malfunctioning. We perform the junction temperature and power estimation at the ideal room temperature \( (T_{\text{amb}} = 25^\circ \text{C}) \) and worse case ambient temperature \( (T_{\text{amb}} = 50^\circ \text{C}) \).

III. BTI ESTIMATION

A model for Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI) was recently developed by Predictive Technology Model (PTM) group [3, 7]. We used this beta version of the model to estimate the changes in threshold voltage \( (V_t \text{ or } V_{th}) \) over time. The model demonstrates the dependence of NBTI on process and design parameters for particular technology used. In our case, the aging model is calibrated for 32nm using High K metal gate model. The aging mainly depends on the operation mode of the transistor, i.e. static or...
dynamic. For a particular transistor, with the stress and recovery timing as shown in the Fig 2:

\[ \Delta V_{th} = \sqrt{K_v^2 \cdot \left(t - t_0\right)^2 + \Delta V_{th1}^2 + \Delta \delta_v} \]

**Phase 2:** Recovery, \( t = (t_2, t_3) \)

\[ \Delta V_{th} = (\Delta V_{th1} - \Delta \delta_v) \cdot \left[1 - \sqrt{\eta (t - t_0)/T}\right] \exp\left[\frac{E_{ox}}{kT}\right] \exp\left[-\frac{V_{th}}{V_{th} - V_{th}}\right] \]

Where,

\[ E_{ox} = \frac{V_{gs} - V_{th}}{T_{ox}} \]

\[ \Delta V_{th} = K_v \cdot \beta^{0.25} \cdot T^{0.25} \cdot \left[\frac{1 - (1 - \eta (t - t_0)/T)^n}{1 - (1 - \eta (1 - \beta))\eta^n} \right]^{0.5} + \Delta \delta_v \]

The strong temperature dependence of the BTI is reflected in \( K_v \) (i.e. \( \exp(-E_a/kT) \) term, where \( T \) is the temperature in Kelvin). For long term degradation and multiple cycle predictions, the following equations describe the \( V_t \) change after \( n \) cycles of stress and recovery, where \( \beta \) is the stress duty cycle and \( T \) is the clock period.

**IV. SRAM CASE STUDIES**

**A. Conventional SRAM**

The conventional Static Random Access Memory is a six transistor circuit as shown in Fig. 3. Each bit of an SRAM is stored on four transistors (two pull-up PMOS and two pull-down NMOS) that form two cross coupled inverters. There are two NMOS access transistors to access the SRAM cell during read and write cycles. A memory bit has two stable states which are denoted as 0 and 1.
corner chips experience much higher junction temperature due to dissipating more leakage power. Leakage power is more for low \( V_t \) transistors compared to high \( V_t \) transistors. Larger memory arrays experience higher temperature, which is simply because of dissipating more power.

The implication of higher junction temperature for the low \( V_t \) SRAM chip is that they will age faster as the BTI gain effects are exponentially temperature dependent. We will quantify this impact in terms of SNM degradation in section V. Fig. 5 shows the results obtained for the power per memory cell (watts) vs. memory size (number of bits) for three different process corners: Low, Nominal and High \( V_t \) and for two ambient temperatures: room temperature (25°C) and worse case ambient temperature (50°C).

### B. Power Gated SRAM

Power gating is a very effective leakage reduction and low power design technique [8]. The power gated SRAM is the conventional SRAM having an additional transistor connected to it known as a sleep transistor (SL) as shown in Fig. 6. Power gating is crucial for the context of SRAM designs because it is mostly used for reducing standby leakage power consumption. Generally, power gating is applied to larger blocks (single or multiple rows/columns), which are controlled by sleep control (SL) signals derived from memory address decoder. In addition to turning off the sleep transistor (M7), a fixed DC voltage is also applied to the virtual ground node (node SS), referred to as source biasing voltage [9]. This DC voltage ensures a fixed reduce voltage supply for the cell in sleep mode to ensure a minimum SNM and at the same reduces the leakage power. We have set the source bias voltage at an optimal voltage of 0.5V. The goal is to turn off as many cells as possible to reduce leakage power. Most of the SRAM cells in a large SRAM array will be in sleep (power gated) mode. Hence, we can estimate the total chip power by estimating the leakage power of one SRAM cell in sleep mode and multiplying it by the total number of cells.

![Power Gated SRAM](image)

The power consumption vs. memory size for the power gated SRAM at three different process corners: Low, Nominal and High \( V_t \) at room (25°C) and worse case temperature (50°C) is depicted in Fig. 7. As expected, the low \( V_t \) SRAM at the low
room temperature (25°C) has the least power consumption. The reported power results are at the estimated junction temperatures.

For one billion cell design, the power gated SRAM shows a minimum of 9.26% power reduction (at 25°C ambient temperature and in High Vt corner) and a maximum of 76.4% power reduction (at 50°C ambient temperature and in Nominal Vt corner) compared to the conventional 6T SRAM. Reduced power consumption results in reduced junction temperature for the power gated SRAM.

Fig. 8 shows the estimated junction temperatures for the power gated SRAM, which shows colder junction temperatures than the conventional 6T SRAM. The junction temperatures are 8.74°C colder for 25°C ambient temperature and in High Vt corner and 72.53°C colder at 50°C ambient temperature and in Nominal Vt corner. The colder junction temperature for power gated SRAM will result in less aging effect. Results of improved aging of the power gated SRAM will be shown in the next section.

V. SNM RESULTS

SRAM cell stability is measured by Static Noise Margin (SNM). We will estimate the SNM for each design (6T and 7T) under different ambient temperatures. Moreover, we estimate the SNM degradation for each design and each ambient temperature over a period of 2 years. The above estimation will be done at the estimated junction temperature for each design using the temperature estimation algorithm discussed. We set the memory size to one billion cells for each design. The estimated Tj for the conventional 6T SRAM are 60.5°C and 122.54°C for room and 50°C ambient conditions, respectively (Table 1).

For the room ambient temperature, the cell is at colder temperature of 60.5°C and there is a drop in SNM by 4.08% from 0.1282V to 0.1230V in two years. For the 50°C ambient condition, the cell experiences a higher temperature of 122.53°C, and there is higher SNM drop of 8.21% from 0.1082V to 0.0994V within a period of two years. These results show that the cell at the colder ambient condition shows more SNM and due to colder operating temperature experiences less aging. Notice that the estimated power and junction temperature are based on standby power estimations, however, the SNM measurements are the read mode SNM, because the read mode shows less SNM than the hold (standby) mode for 6T SRAM cell.

<table>
<thead>
<tr>
<th>Ambient Temperature (°C)</th>
<th>Estimated Junction Temp Tj (°C)</th>
<th>Read SNM -- fresh (V)</th>
<th>Read SNM -- after 2 years (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 (cold)</td>
<td>60.5</td>
<td>0.1282</td>
<td>0.1230 (-4.08%)</td>
</tr>
<tr>
<td>50 (hot)</td>
<td>122.5</td>
<td>0.1082</td>
<td>0.0994 (-8.21%)</td>
</tr>
</tbody>
</table>

Table 1: Junction temperature and SNM aging results of 6T SRAM at two ambient temperatures ($R_{ja} = 1°C/W$)
The power gated SRAM can be in two modes: active mode (read operation) and sleep mode (hold mode). The power and junction temperature are estimated based on the sleep mode leakage power consumption since majority of the cells are in sleep mode. The SNM is measured in both the active (read) mode and the sleep (hold) mode, since either mode can potentially be a worst case mode for SNM. For the 7T power gated SRAM, the estimated junction temperatures are 25.01°C and 50.01°C for the room (cold) and hot (50°C) ambient conditions. Under cold ambient, the SNM of the cell in the active mode reduces by 2.38% in two year life-time due to BTI aging. This reduction is 3.7% in the sleep mode. Under hot ambient, the SNM of the cell ages faster due to higher junction temperature (2.71% SNM drop in read mode SNM and 4.43% sleep mode SNM drop in two years lifetime).

Table 2: SNM results for the 7T SRAM at two ambient temperatures ($R_{ja} = 1°C/W$)

<table>
<thead>
<tr>
<th>Ambient temperature (°C)</th>
<th>25 (cold)</th>
<th>50 (hot)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Estimated Junction Temp $T_J$ (°C)</td>
<td>25.01</td>
<td>50.01</td>
</tr>
<tr>
<td>Read SNM -- fresh (V)</td>
<td>0.1123</td>
<td>0.1004</td>
</tr>
<tr>
<td>Read SNM -- after 2 years (V)</td>
<td>0.1096</td>
<td>0.0977</td>
</tr>
<tr>
<td>Sleep (Hold) SNM – fresh (V)</td>
<td>0.1179</td>
<td>0.1153</td>
</tr>
<tr>
<td>Sleep (Hold) SNM – after 2 years (V)</td>
<td>0.1136</td>
<td>0.1102</td>
</tr>
</tbody>
</table>

Comparing the results in Tables 1 and 2 clearly shows that the designs that operate at higher temperatures (due to dissipating more power) will age faster. This is due to the strong temperature dependence of the BTI aging effects. It is also observed that the power gating reduces the power consumption of the design and hence the operating junction temperature, resulting in less SNM aging over lifetime. Under the room ambient condition and compared to the conventional 6T SRAM, the power gated SRAM reduces the read SNM aging from 4.08% to 2.38%. This is attributed to less leakage power and hence colder junction temperature of the power gated design.

VI. CONCLUSION

We proposed a methodology to estimate junction temperature of SRAM design for the purpose of accurate estimation of the BTI aging effects. We analyzed the junction temperatures for 6T SRAM and 7T power gated SRAM cell in 32nm CMOS technology. For the estimated junction temperatures, we also applied the BTI aging model for estimating SNM degradation over a 2-year lifetime. Our results clearly show that due to the sensitivity of BTI aging to temperature, accurate estimation of the SNM aging requires accurate junction temperature estimation. In our case study of the SRAM design, we observed that the power gated SRAM experiences colder junction temperatures compared to the conventional 6T SRAM due to less power consumption. Due to colder junction temperatures, the power gated SRAM also experiences less SNM aging compared to the 6T SRAM cell.

REFERENCES