

## LAB #4: BJT CHARACTERIZATION

Updated: May 5, 2003

### Objective:

To characterize a *bipolar junction transistor* (BJT), both statically and dynamically. To compare PSpice simulations with experimental observations.

### Components:

1 × 2N2222 *npn* BJT, 1 × NTE112 (or equivalent) Small-Signal Schottky Diode; capacitors: 1 × 0.1 μF and 1 × 10 μF; resistors: 1 × 100 Ω, 1 × 1.0 kΩ, 2 × 10 kΩ, 2 × 100 kΩ, 1 × 330 kΩ (all 5%, ¼ W).

### Instrumentation:

A bench power supply, a triangle signal generator, a pulse generator, a digital multi-meter, and a dual-trace oscilloscope with low input capacitance X10 probes.

## PART I – THEORETICAL BACKGROUND

Even though today's digital electronics is dominated by CMOS technology, there are still great many electronic systems in operation that were implemented in the bipolar technologies (TTL and ECL) that preceded the takeover by CMOS. Consequently, the servicing and upgrading of these systems requires the knowledge of bipolar logic families. Moreover, nowadays many ICs are fabricated in the so-called *BiCMOS* technology, which combines the advantages of both bipolar and CMOS technologies to achieve performance levels that could not be achieved by either one of the two technologies alone. For the above reasons, it pays to study the bipolar junction transistor (BJT) in sufficient detail.

When it comes to switching applications, BJTs *differ* from FETs in two important respects:

- A BJT requires a certain amount of *base current* to go on. By contrast, a FET exhibits virtually infinite input resistance, indicating that inter-stage loading and fanout are more critical in BJT circuits.
- BJT conduction is established by *minority carriers*, which need to be *injected* into the base region to turn the BJT on, and to be *removed* from the base region to turn the BJT off – both of which take time to be accomplished. By contrast, conduction in FETs is established by majority carriers only, which exhibit no charge-storage effects – just like ordinary resistors. Consequently, the switching characteristics of BJTs are more complex than those of FETs. Mercifully, Spice simulation is of great help in the study of bipolar switching circuits.

We also make the following additional comparisons:

- Beside minority-charge storage effects, a BJT exhibits also stray capacitances, namely the *junction capacitances*  $C_{je}$  and  $C_{jc}$  between base and emitter and between base and collector, respectively. These are similar to the capacitances  $C_{gs}$  and  $C_{gd}$  between gate and source and between gate and drain of a MOSFET. However, while  $C_{je}$  and  $C_{jc}$  are *junction* capacitances,  $C_{gs}$  and  $C_{gd}$  are *overlap* capacitances.
- As we know, a MOSFET exhibits also the junction capacitances  $C_{sb}$  and  $C_{db}$ , and the overlap capacitance  $C_{gb}$ ; however, these capacitances do not have their counterparts in BJTs.
- Another difference is that the small-signal transconductance  $g_m$  of a BJT is generally much higher than that of a FET. This is due to the *exponential  $i$ - $v$*  characteristic of the BJT, which is generally much steeper than the *quadratic* characteristic of a FET. However, in switching applications this difference is usually of less concern than in analog applications.

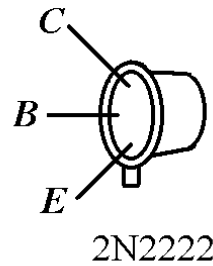
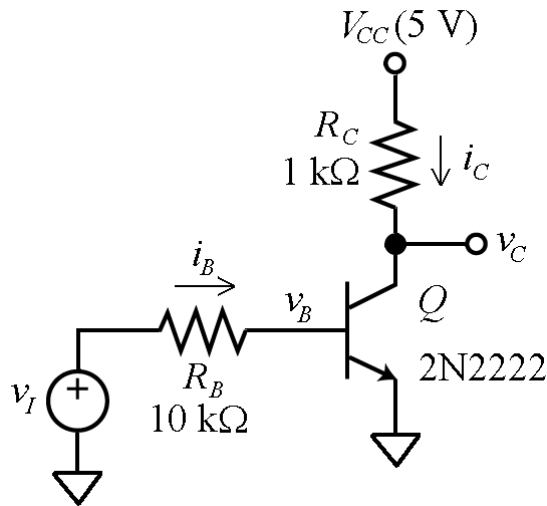


Fig. 1 – Basic BJT inverter, and the 2N2222 BJT..

### PSpice Simulations:

In the following we shall use PSpice to display both the *static* and *dynamic characteristics* of the simple BJT inverter of Fig. 1. The circuit is based on the popular 2N2222 *npn* BJT, whose model is available in PSpice’s library. This model is based on the information provided in the manufacturer’s data sheets, which report *typical* data. In this lab we shall characterize a particular 2N2222A sample and develop our own PSpice model for it. Then, we shall compare computer simulations and experimental observations. You are also encouraged to compare your measured data against those reported in the data sheets, which can readily be downloaded from the Web (for instance, by visiting <http://www.google.com> and searching for 2N2222A or variants thereof.) You can simulate the circuits below on your own. To this end, go to <http://online.sfsu.edu/~sfranco/CoursesAndLabs/Labs/453Labs.html>, and once there, click on **PSpice Examples** and then follow the instructions contained in the **Readme** file.

### Static BJT Characteristics:

Figure 2 shows the PSpice circuit used to visualize the static characteristics of the inverter for the case in which  $v_I$  is swept from 0 V to 2 V. Figure 3 shows, top to bottom, the *base current*  $i_B$ , the *collector current*  $i_C$ , the *base voltage*  $v_B$ , and the *collector voltage*  $v_C$ . On the  $v_C$  curve, at the bottom, we identify two important points: the *edge-of-conduction* (EOC) and the *edge-of-saturation* (EOS), and we make the following considerations:

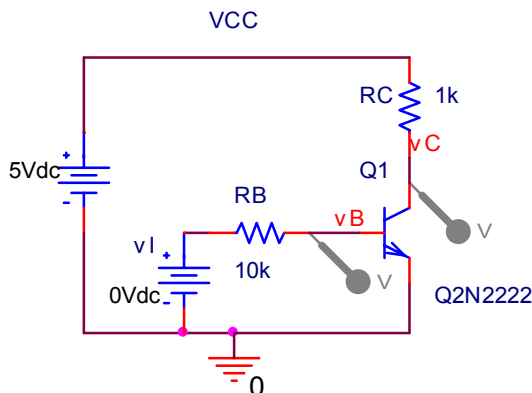


Fig. 2 - PSpice circuit to display the voltage and current transfer characteristics of the BJT inverter.

- To the left of the EOC, the BJT is in *cut off* (CO). The voltage and current transmitted by  $R_B$  to the base are insufficient to turn the BJT convincingly on, so  $i_B \cong 0$ ,  $i_C \cong 0$ , and  $v_C \cong V_{CC} = 5 \text{ V}$ .
- Between the EOC and the EOS, the BJT operates in the *forward-active* (FA) region and gives

$$i_C = \beta_F i_B \quad (1)$$

where  $\beta_F$  is the FA *current gain*. In this region,  $i_C$  is related to the base-emitter voltage drop  $v_{BE}$  as

$$i_C = I_s e^{v_{BE}/V_T} \quad (2)$$

where  $I_s$  is a scaling factor called the *collector saturation current*, and  $V_T$  is a scaling factor called the *thermal voltage* ( $V_T \cong 26 \text{ mV}$  at 300 K). For low-power BJTs,  $I_s$  is typically on the order of femtoamperes ( $1 \text{ fA} = 10^{-15} \text{ A}$ ).

Turning Eq. (2) around, we find  $v_{BE} = V_T \ln(i_C/I_s)$ . Since  $i_C$  appears in the argument of the logarithm,  $v_{BE}$  will change very little as the operating point is swept from the EOC to the EOS. Consequently, within the FA region we can approximate

$$v_{BE} \cong V_{BE(\text{on})} \quad (3)$$

Low-power silicon BJTs typically exhibit  $V_{BE(\text{on})} \cong 0.7 \text{ V}$ . Within the FA region we also have  $v_C = V_{CC} - R_C i_C = V_{CC} - R_C \beta_F i_B \cong V_{CC} - R_C \beta_F (v_I - V_{BE(\text{on})})/R_B$ , indicating that the slope of the  $v_C$  curve is

$$a = -\beta_F \frac{R_C}{R_B} \quad (4)$$

In the PSpice example given,  $a \cong -166 \times 1/10 = -16.6 \text{ V/V}$ .

- Once the EOS is reached,  $v_{CE}$  stabilizes at the approximately constant value  $v_{CE} = V_{CE(\text{sat})} \cong 0.1 \text{ V}$ . Consequently,  $i_C$  saturates at

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \quad (5)$$

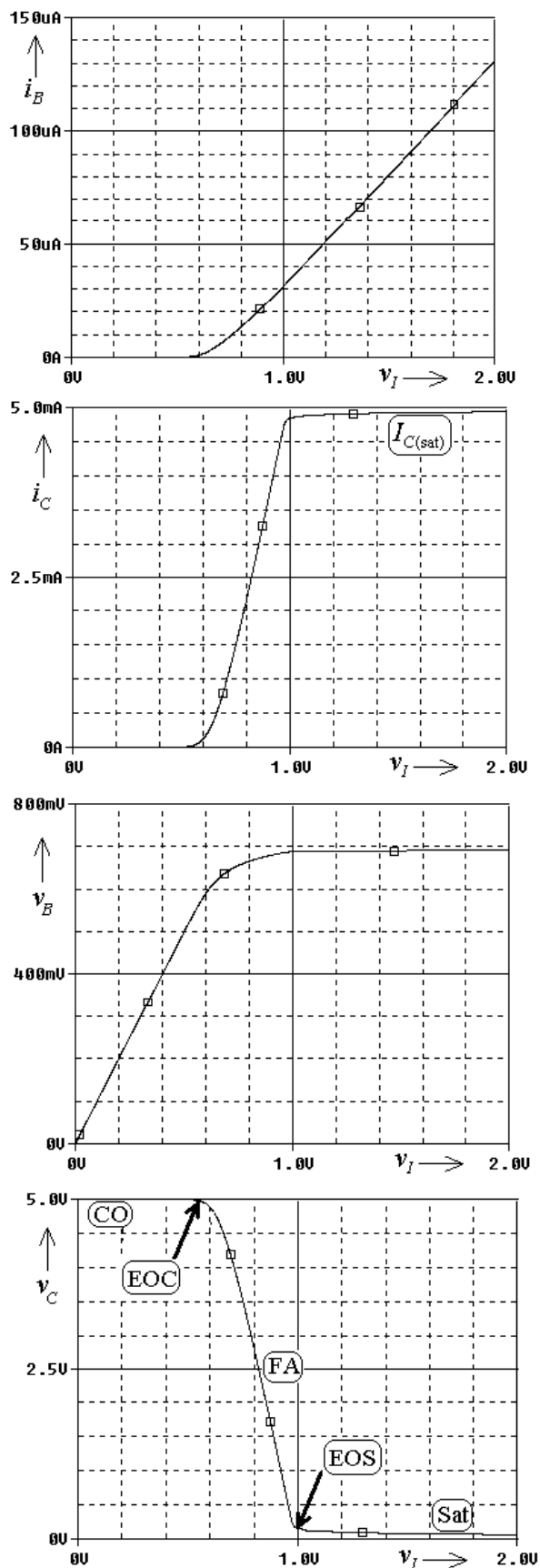
or  $I_{C(\text{sat})} \cong (5 - 0.1)/1 = 4.9 \text{ mA}$  in the example given. Hence, the name *saturation* for the region to the right of the EOS. In this region,  $i_B$  keeps increasing with  $v_I$ , but  $i_C$  remains constant at  $I_{C(\text{sat})}$ . The ratio  $i_C/i_B$ , which in saturation is aptly denoted as  $\beta_{\text{sat}}$ , is  $\beta_{\text{sat}} = I_{C(\text{sat})}/i_B$  and it *decreases* past the EOS, indicating that

$$\beta_{\text{sat}} \leq \beta_F \quad (6)$$

In the PSpice example given,  $\beta_{\text{sat}}$  ranges from  $\beta_{\text{sat}} = \beta_F \cong 166$  right at the EOS, to  $\beta_{\text{sat}} \cong (4.9 \text{ mA})/(130 \mu\text{A}) \cong 38$  at the rightmost point of the graph, corresponding to  $v_I = 2 \text{ V}$ . Clearly, *the deeper* the BJT is in saturation, *the lower* the value of  $\beta_{\text{sat}}$ .

If in Fig. 1 we interchange the emitter (E) and collector (C) terminals with each other (see Fig. 7b below), then the BJT is said to operate in the *reverse mode*. The counterpart of the forward-active region is now the *reverse-active* (RA) region, where Eq. (1) becomes

$$i_E = \beta_R i_B \quad (7)$$



**Fig. 3** – Plots of the basic BJT inverter's voltages and currents as functions of  $v_I$ .

While  $\beta_F$  is typically on the order of  $10^2$  or higher,  $\beta_R$  is much lower, typically on the order of 10 to 0.01.

When a BJT is in *saturation*, both its *B-E* and *B-C* junctions are *forward biased*, so the device can be regarded as operating *simultaneously* in FA and RA! Theory predicts the following expression:

$$V_{CE(sat)} = V_T \ln \frac{1 + (1 + \beta_{sat}) / \beta_R}{1 - \beta_{sat} / \beta_F} \quad (8)$$

Note that while  $\beta_F$  and  $\beta_R$  are intrinsic BJT parameters, the value of  $\beta_{sat}$  depends on the operating conditions established, or forced, by the user. For this reason,  $\beta_{sat}$  is often denoted also as  $\beta_{forced}$ .

### Dynamic BJT Characteristics:

The switching behavior of a BJT is far more complex than that of a MOSFET because of minority charge-storage effects within its base region. BJT dynamics are governed by *charge-control equations*, which for the *npn* BJT take on the form

$$i_B = \frac{Q_F}{\tau_{BF}} + \frac{Q_R}{\tau_{BR}} + \frac{d}{dt}(Q_F + Q_R + Q_{je} + Q_{jc}) \quad (9a)$$

$$i_C = \frac{Q_F}{\tau_F} - Q_R \left( \frac{1}{\tau_R} + \frac{1}{\tau_{BR}} \right) - \frac{d}{dt}(Q_R + Q_{jc}) \quad (9b)$$

$$i_E = -\frac{Q_R}{\tau_R} + Q_F \left( \frac{1}{\tau_F} + \frac{1}{\tau_{BF}} \right) + \frac{d}{dt}(Q_F + Q_{je}) \quad (9c)$$

where

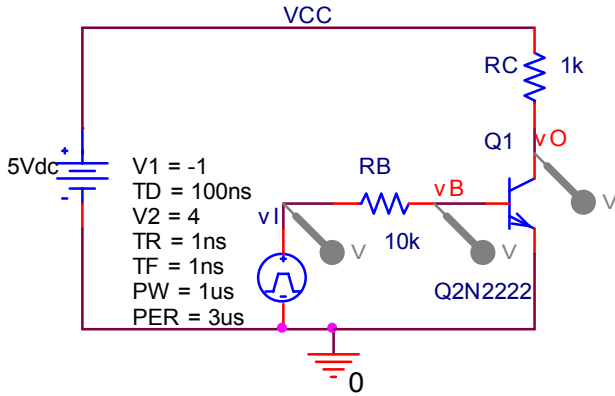
- $Q_F$  is the *FA-mode excess minority-carrier base charge*
- $Q_R$  is the *RA-mode excess minority-carrier base charge*
- $Q_{je}$  is the charge stored in the *space-charge layer* of the *B-E* junction
- $Q_{jc}$  is the charge stored in the *space-charge layer* of the *B-C* junction
- $\tau_F$  is the *mean forward transit time* of minority carriers in the base region
- $\tau_{BF}$  is the *FA-mode mean lifetime* of minority carriers in the base region
- $\tau_R$  is the *mean reverse transit time* of minority carriers in the base region
- $\tau_{BR}$  is the *RA-mode mean lifetime* of minority carriers in the base region

To gain a better feel for the roles of the different charge components, we use the PSpice circuit example of Fig. 4 to display all relevant waveforms of the simple inverter of Fig. 1 in response to a pulse  $v_I$  that we have chosen to alternate between  $V_L = -1$  V to  $V_H = 4$  V. The various waveforms are depicted in Fig. 5. Following the inception of the input pulse at  $t = t_0$ , we observe the following events:

- From  $t_0$  to  $t_1$  the BJT is brought from *CO* to the *EOC*. During this time interval, called the *delay time*

$$t_D = t_1 - t_0 \quad (10)$$

the charges  $Q_F$  and  $Q_R$  are still zero, so Eq. (9) reduces to



**Fig. 4** - PSpice circuit to display the dynamic characteristics of the basic BJT inverter.

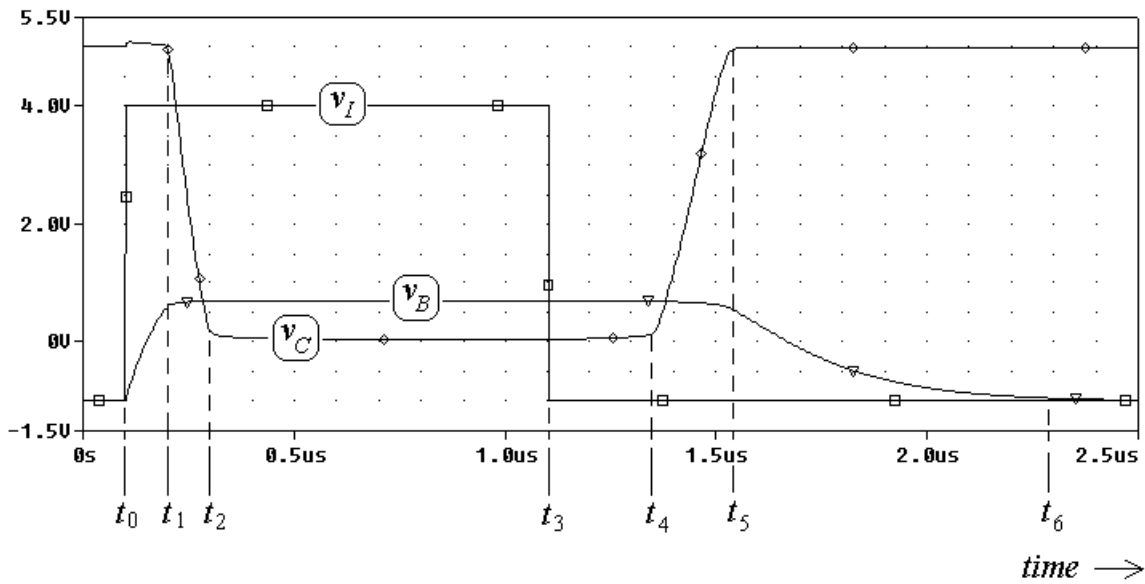
$$i_B = \frac{d}{dt}(Q_{je} + Q_{jc}) \quad (11a)$$

$$i_C = -\frac{d}{dt}(Q_{jc}) \quad (11b)$$

Equation (11a) states that  $i_B$  merely goes into charging up the space-charge layers of the  $B-E$  and  $B-C$  junctions. Associated with these space-charge layers are the  $B-E$  and  $B-C$  junction capacitances

$$C_{je} = \frac{C_{je0}}{(1 - v_{BE}/\phi_e)^{m_e}} \quad (12a)$$

$$C_{jc} = \frac{C_{jc0}}{(1 - v_{BC}/\phi_c)^{m_c}} \quad (12b)$$



**Fig. 5** – Plot of all relevant waveforms for the basic BJT inverter.

where

- $C_{je0}$  and  $C_{jc0}$  are the *zero-bias* ( $v_{BE} = v_{BC} = 0$ ) values of these capacitances
- $\phi_e$  and  $\phi_c$  are the *built-in potentials* of the corresponding junctions
- $m_e$  and  $m_c$  are the *grading coefficients* of the corresponding junctions

In our example,  $C_{je}$  is charged from  $v_{BE}(t_0) = -1$  V to  $v_{BE}(t_1) \cong 0.7$  V, and  $C_{jc}$  is charged from  $v_{BC}(t_0) = -6$  V to  $v_{BC}(t_1) \cong -4.3$  V. It is interesting to note that the portion of  $i_B$  flowing through  $C_{jc}$  exits the collector to flow into  $R_C$ , causing a small bump in  $v_C$  above  $V_{CC}$ . This is confirmed by Eq. (11b).

- From  $t_1$  to  $t_2$ , the BJT is brought from the *EOC*, through the *FA region*, to the *EOS*. During this time interval, called the *fall time*

$$t_F = t_2 - t_1 \quad (13)$$

we are witnessing the buildup of  $Q_F$  ( $Q_R$  is still zero), so Eq. (9) reduces to

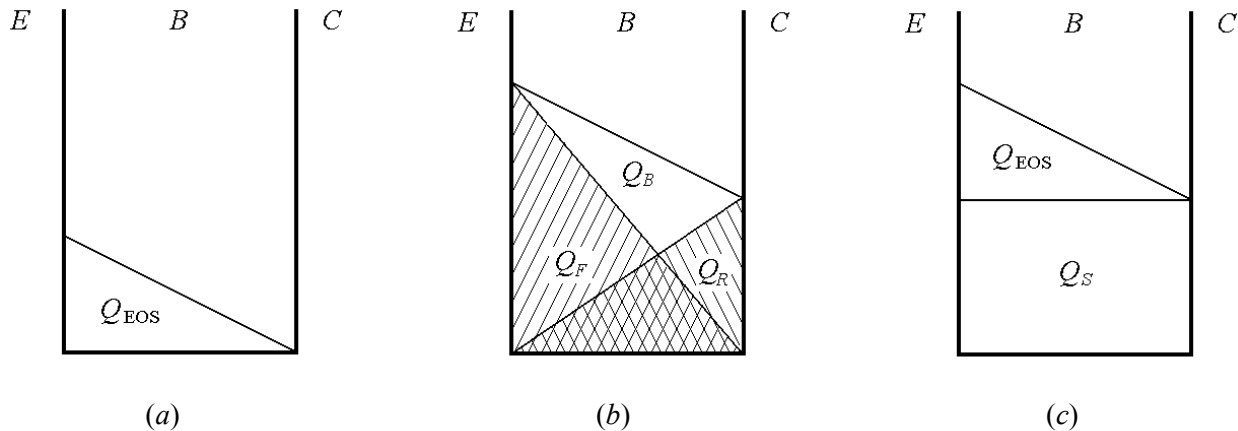
$$i_B = \frac{Q_F}{\tau_{BF}} + \frac{d}{dt}(Q_F + Q_{je} + Q_{jc}) \quad (14a)$$

$$i_C = \frac{Q_F}{\tau_F} - \frac{dQ_{jc}}{dt} \quad (14b)$$

In our example, there is negligible charge transfer to  $C_{je}$  because  $v_{BE}$  remains approximately constant at  $V_{BE(on)} \cong 0.7$  V;  $C_{jc}$  is charged from  $v_{BC}(t_1) \cong -4.3$  V to  $v_{BC}(t_2) \cong +0.6$  V; and the rest of  $i_B$  goes into building up as well as maintaining  $Q_F$ . As  $Q_F$  builds up, so does  $i_C$ , by Eq. (14b). This causes  $v_C$  to swing from 5 V to approximately 0.1 V.

- At time  $t_2$ , the BJT is at the *EOS*, and the excess minority charge accumulated thus far in the base is  $Q_{EOS} = \tau_F I_{C(EOS)} = \tau_F I_{C(sat)}$ , with  $I_{C(sat)}$  given in Eq. (5). This charge is depicted in Fig. 6a. The amount of base current necessary to bring the BJT to the EOS is

$$I_{B(EOS)} = \frac{I_{C(EOS)}}{\beta_F} \quad (15)$$



**Fig. 6** – Excess minority charge in the base region: (a) at the edge of saturation (EOS), and (b), (c) in deep saturation.

In the given example we have  $I_{B(\text{EOS})} \cong 30 \mu\text{A}$ .

- After  $t_2$ , the BJT enters *deep saturation*. Since now also the *B-C* junction is forward biased, we witness also the buildup of  $Q_R$ , beside  $Q_F$  already there, so the total base charge is  $Q_B = Q_F + Q_R$ , see Fig. 6b. As depicted in Fig. 6c, we can also express this charge as

$$Q_B = Q_{\text{EOS}} + Q_S \quad (16)$$

where  $Q_{\text{EOS}} = \tau_F I_{C(\text{EOS})} = \tau_{BF} I_{B(\text{EOS})}$  is the previously defined charge right at the EOS, and  $Q_S$  represents the *additional charge* resulting from operation in deep saturation. Aptly called the *overdrive base charge*,  $Q_S$  builds up according to the equation

$$i_{BS} = \frac{Q_S}{\tau_S} + \frac{dQ_S}{dt} \quad (17)$$

where

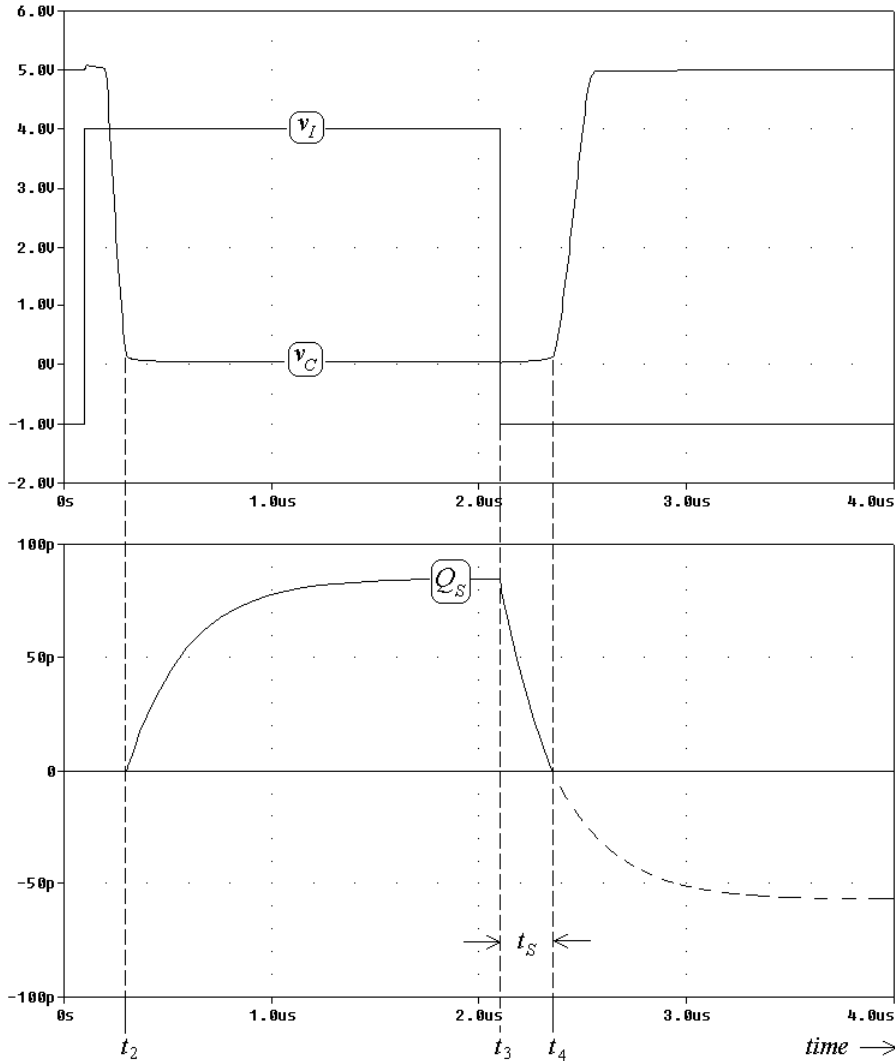


Fig. 7 – Illustrating the buildup as well as the removal of the overdrive base charge  $Q_S$ .

$$i_{BS} = i_B - I_{B(EOS)} \quad (18)$$

is called the *base current overdrive*. In the given example,  $i_{BS} \cong 330 - 30 = 300 \mu\text{A}$ . The time constant  $\tau_S$ , called the *saturation time constant*, is a weighted sum of  $\tau_{BF}$  and  $\tau_{BR}$ , owing to the fact that the BJT is now simultaneously in FA and RA,

$$\tau_S = \frac{(\beta_R + 1)\tau_{BF} + \beta_F\tau_{BR}}{\beta_F + \beta_R + 1} \quad (19)$$

In the given example,  $\tau_S \cong 285 \text{ ns}$ . At the end of the buildup, the overdrive base charge attains the steady-state value  $Q_S = \tau_S i_{BS}$ . In the given example,  $Q_S \cong 85 \text{ pC}$ . The buildup of  $Q_S$  is depicted in the expanded view of Fig. 7.

- At  $t_3$ , the input pulse is removed, but the BJT *continues to remain on!* In fact, it remains saturated until all of the charge  $Q_S$  stored in its base is completely removed! This removal is accomplished by the base current now flowing *out* of the base terminal. Charge removal is still governed by Eq. (17), except that now  $i_{BS}$  is negative. In the given example,  $i_{BS} \cong -170 - 30 = -200 \mu\text{A}$ , and the mathematical projection of the steady-state excess charge is now  $Q_S = \tau_S i_{BS} \cong -57 \text{ pC}$ . The removal of  $Q_S$  is completed at  $t_4$ , and the time interval

$$t_S = t_4 - t_3 \quad (20a)$$

aptly called the *storage time*, is readily found as

$$t_S = \tau_S \ln \frac{I_{BF} - I_{BR}}{I_{B(EOS)} - I_{BR}} \quad (20b)$$

where  $I_{BF} = (V_H - V_{BE(\text{on})})/R_B$ ,  $I_{BR} = (V_L - V_{BE(\text{on})})/R_B$ , and  $I_{B(EOS)}$  is given by Eq. (15). In the given example we have  $I_{BF} \cong 330 \mu\text{A}$ ,  $I_{BR} \cong -170 \mu\text{A}$ , and  $I_{B(EOS)} \cong 30 \mu\text{A}$ .

- From  $t_4$  to  $t_5$ , the BJT is brought from the *EOS*, through the *FA region*, back to the *EOC*. This is similar to the event from  $t_1$  to  $t_2$ , but in reverse. This transition is still governed by Eq. (12), but with  $i_B$  now negative. Defining the *rise time*

$$t_R = t_5 - t_4 \quad (21)$$

we observe that our example gives  $t_R \gg t_F$ , owing to the fact that  $i_B$  has much smaller magnitude during  $t_R$  than during  $t_F$ .

- From  $t_5$  to  $t_6$ , the BJT is brought *back* from the *EOC* to the initial *CO* condition. This is similar to the event from  $t_0$  to  $t_1$ , but in reverse. This event is still governed by Eq. (10), but with  $i_B$  now negative. Defining the *recovery time*

$$t_{RR} = t_6 - t_5 \quad (22)$$

we observe that  $t_{RR} \gg t_D$ .

## PART II – EXPERIMENTAL PART

Henceforth, steps shall be identified by letters as follows: **C** for calculations, **M** for measurements, and **S** for Spice simulations. As usual, all data must be expressed in the form  $X \pm \Delta X$ .

Mark one of the 2N2222A BJTs available in your kit (the other is a spare).

### Static Characteristics:

**MC1:** We use the circuit of Fig. 8a for *static FA parameter* measurements (for the pin configuration of the 2N2222 BJT, refer to Fig. 1). Assemble the circuit with power off, keeping leads short and connecting a 0.1- $\mu$ F bypass capacitor between the 5-V and the ground bus in close proximity to the BJT. Next, apply power, and measure  $I_B$ ,  $I_C$ , and  $V_{BE}$ . Finally, calculate  $\beta_F = I_C/I_B$  and  $I_s = I_C / e^{V_{BE}/(26 \text{ mV})}$

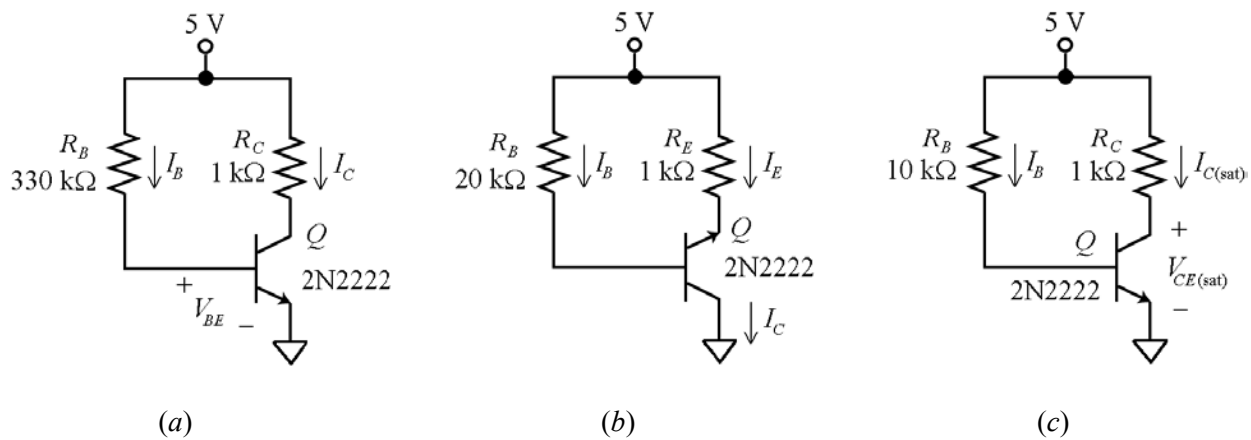
**Reminder:** To measure  $V_{BE}$ , configure the multi-meter as a *DC Voltmeter*, and connect it in *parallel* between *B* and *E*. To measure  $I_B$ , configure the multi-meter as a *DC Ammeter*, break the circuit at *B*, and insert the ammeter in *series* between  $R_B$  and *B*. To measure  $I_C$ , break the circuit at *C*, and insert the ammeter in *series* between  $R_C$  and *C*. Recall that a multi-meter exhibits *low* input resistance when configured as an *ammeter*, and *high* input resistance when configured as a *voltmeter*. As you switch the instrument back and forth between the two modes, avoid creating inadvertent low-resistance connections that might damage both your instrument and your circuit! This may occur if you try to perform a *voltage* measurement with the instrument still configured for *ammeter* operation! As a good work habit, always configure your instrument with its terminals disconnected from the circuit, and then connect it in *series* for *ammeter* measurements, in *parallel* for *voltmeter* measurements. If you are careless and end up damaging the BJT under consideration, you'll have to repeat all measurements on another BJT sample!

**MC2:** We use the circuit of Fig. 8b for *static RA parameter* measurements. Assemble the circuit with power off, following the precautions of Step MC1 (for  $R_B$ , use  $2 \times 10 \text{ k}\Omega$  in series). Next, apply power, measure  $I_B$  and  $I_E$ , calculate  $\beta_R = I_E/I_B$ , and give as many reasons as you can think of why  $\beta_R \ll \beta_F$ .

**MC3:** We use the circuit of Fig. 8c for *saturation parameter* measurements. After assembling your circuit with the usual precautions, measure  $I_B$ ,  $I_{C(\text{sat})}$ , and  $V_{CE(\text{sat})}$ , and calculate  $\beta_{\text{sat}} = I_{C(\text{sat})}/I_B$ . Finally, use Eq. (8) to calculate  $V_{CE(\text{sat})}$ , compare with the measured value, and account for any differences.

**C4:** Predict  $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ , and  $V_{IH}$  for the basic inverter of Fig. 1 if  $Q_1$  is the *particular* BJT sample that you have just characterized.

**SC5:** Use PSpice to plot the VTC of the inverter of Fig. 1 if  $Q_1$  is the *particular* BJT sample that you have just characterized. Then, find  $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ , and  $V_{IH}$  graphically, compare with those predicted in Step C4, and account for any differences.



**Fig. 8** – Test circuits for static measurements in the (a) *forward-active* (FA), (b) *reverse-active* RA, and (c) *saturation* regions.

**Remark:** For a realistic simulation of your particular BJT sample, you need to override the BJT parameters assumed by PSpice, which are typical, and impose those found experimentally. To this end, click the 2N2222 BJT in your PSpice schematic to select it, and then click **Edit** → **PSpice Model** to change its parameter values to those found experimentally. In our simplified characterization, we specify only the values of  $I_s$ ,  $\beta_F$ , and  $\beta_R$ , so the model statement becomes

```
.model Q2N2222 NPN( IS=* Bf=* Br=* )
```

where the asterisks indicate the values found experimentally, such as: (  $I_s=2.5\text{ fA}$   $Bf=150$   $BR=5$  )

**MC6:** Assemble the circuit of Fig. 1 with the BJT sample you have just characterized, and use similar techniques to those of Step MC3 of Lab #2 to display its VTC on the oscilloscope. Then, find  $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ , and  $V_{IH}$  graphically, compare with those of Step SC5, and account for any discrepancies.

### Dynamic BJT Characteristics:

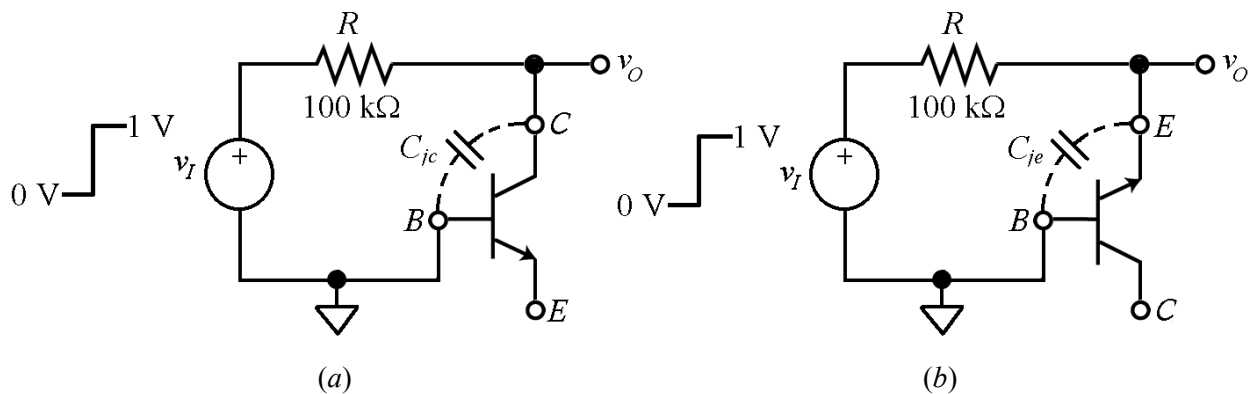
For the dynamic characterization of our device we need to find  $C_{jc}$ ,  $C_{je}$ ,  $\tau_F$ , and  $\tau_R$ . The complete characterization of  $C_{jc}$  and  $C_{je}$  requires a trio of parameters for each, namely, the zero-bias capacitances  $C_{jc0}$  and  $C_{je0}$ , the built-in potentials  $\phi_c$  and  $\phi_e$ , and the grading coefficients  $m_c$  and  $m_e$ . For the purposes of this lab we shall limit ourselves to finding only the zero-bias capacitances. Then in the course of our PSpice simulations, we shall use the potentials and grading coefficients given in the 2N2222 model already available in PSpice's library.

### Finding $C_{jc0}$ and $C_{je0}$ :

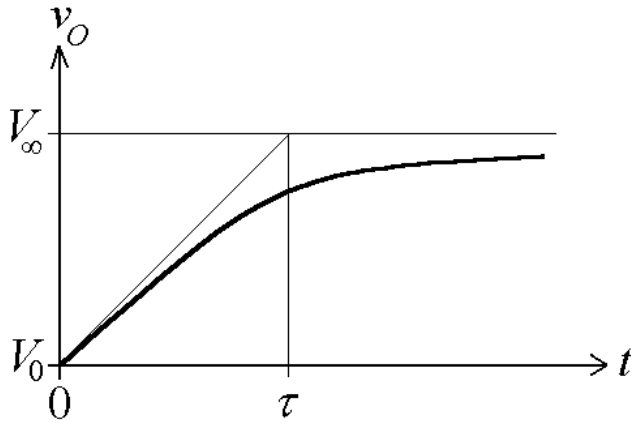
We use the test circuits of Fig. 9 to find the zero-bias capacitances  $C_{jc0}$  and  $C_{je0}$ . In either case we make the junction capacitance  $C_j$  form an RC circuit. Applying an input voltage step as depicted in Fig. 10, results in a *pseudo-exponential* output transient (recall that junction capacitances vary with voltage and are thus nonlinear!). However, the slope of the response *right at the origin* is  $V_{\infty}/(RC_{j0})$ , where  $V_{\infty}$  is the *steady-state* value of  $v_o$ . Consequently, we can find  $C_{j0}$  indirectly via a simple *slope measurement* on the oscilloscope. Note that the polarity of the input step has been chosen so as to keep the corresponding junction at all times *reverse biased* in order to evidence only its capacitive behavior.

**MC7:** Turning first to  $C_{jc0}$  (Fig. 9a). proceed as follows:

- While monitoring  $v_i$  with Ch. 1 of the oscilloscope, adjust the waveform generator so that  $v_i$  is a 50-kHz square wave alternating between 0 V and 1 V. This ensures that the B-C junction is never



**Fig. 9** – Test circuits to measure (a)  $C_{jc0}$  and (b)  $C_{je0}$ .



**Fig. 10** – Illustrating the graphical determination of the zero-bias junction capacitance  $C_{j0}$ .

forward-biased, causing it to act as a mere capacitance  $C_{jc}$  between  $C$  and  $B$  (note that  $E$  is left unconnected!).

- With Ch. 1 of the oscilloscope triggered on the leading edge of  $v_i$ , observe  $v_o$  with Ch. 2. The result is a transient whose *tangent* at  $V_0$  ( $= 0$  V) intercepts the steady-state value  $V_\infty$  ( $= 1$  V) at  $\tau = R(C_{jc0} + C_{\text{stray}})$ , where  $C_{jc0}$  is the value of  $C_{jc}$  at  $v_{BC} = 0$ , and  $C_{\text{stray}}$  is the stray capacitance of the probe and wires. Use graphical techniques to find  $\tau$ .

**Remark:** For optimal visualization of  $v_o$ , you may wish to change the frequency of  $v_i$  from the initial suggested value of 50 kHz. Also, make sure you first compress the horizontal scale of the oscilloscope to visualize the steady-state value  $V_\infty$ , and then you suitably expand it until slope is in the vicinity of  $45^\circ$ , which provides about the best condition for slope measurements.

- Disconnect  $B$  from ground, and find the *new* value  $\tau_0$  of the intercept. Clearly,  $\tau_0 = RC_{\text{stray}}$ .
- Pull  $R$  out of the circuit, measure it with the ohmmeter, and calculate  $C_{jc0} = (\tau - \tau_0)/R$ .

**Warning:** For this and the following measurements, it is critical that you use a low input-capacitance probe, such as a X10 probe (make sure to check that you probe is properly compensated, as discussed in Appendix 2!). Also, keep all leads as short as possible to minimize the effect of parasitics.

**MC8:** Repeat Step MC7, but with  $C$  and  $E$  *interchanged* with each other to find  $C_{je0}$  (see Fig. 9b.) Compare the value of  $C_{je0}$  with that of  $C_{jc0}$ , and try justifying the difference.

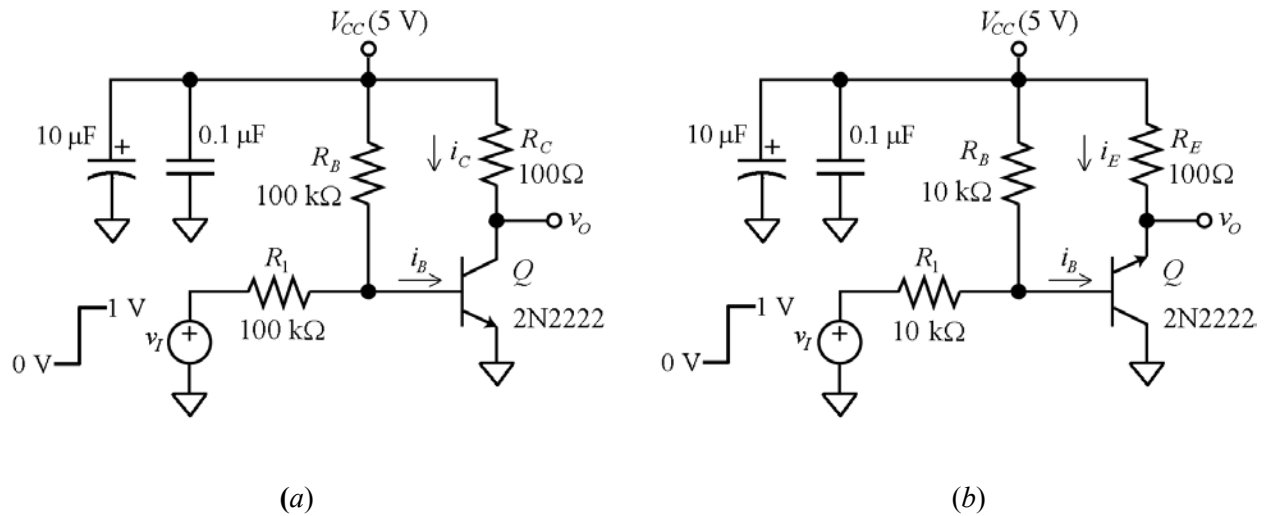
### Finding $\tau_F$ and $\tau_R$ :

We use the test circuits of Fig. 11 to find  $\tau_{BF}$  and  $\tau_{BR}$ . Then, using the results of our static characterization, we calculate  $\tau_F = \tau_{BF}/\beta_F$ , and  $\tau = \tau_{BR}/\beta_R$ .

Turning first to the circuit of Fig. 11a, we note that  $R_B$  biases the BJT in the FA region, and the small-valued resistance  $R_C$  senses the collector current  $i_C$ . Applying an input voltage step via  $R_1$  will force the BJT to switch between two different operating points *both* within the *FA region*. The setup is designed to ensure negligibly small variations in  $v_{BE}$  and  $v_{BC}$  so that the effects of  $C_{je}$  and  $C_{jc}$  can be ignored. Consequently, Eq. (14) simplifies further as

$$i_B = \frac{Q_F}{\tau_{BF}} + \frac{dQ_F}{dt} \quad (23a)$$

$$i_C = \frac{Q_F}{\tau_F} \quad (23b)$$



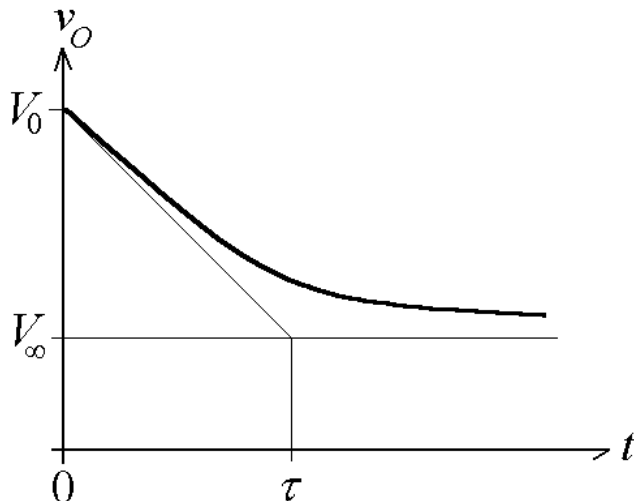
**Fig. 11** – Test circuits to find  $\tau_{BF}$  and  $\tau_{BR}$ .

The solution to Eq. (23a) is an *exponential transient* in  $Q_F$  governed by the *time constant*  $\tau_{BF}$ . But, by Eq. (23b),  $i_C$  is proportional to  $Q_F$ , indicating an exponential transient also in  $i_C$  and with the same time constant  $\tau_{BF}$ . To be able to observe this transient with the oscilloscope, we send  $i_C$  through  $R_C$  to develop the voltage transient  $v_O$ , on which we then find  $\tau_{BF}$  graphically (see Fig. 12). The procedure is similar to that of Step MC7, except that now  $v_O$  is in the vicinity of 5 V. To be able to observe the transient with sufficient resolution, you must thus use the oscilloscope in the *AC mode* and adjust it for a suitable vertical sensitivity.

Similar considerations hold for the setup of Fig. 11b, in which we operate the BJT in the RA region to find  $\tau_{BR}$ . In this case the expressions of Eq. (9) reduce to

$$i_B = \frac{Q_R}{\tau_{BR}} + \frac{dQ_R}{dt} \quad (24a)$$

$$i_E = \frac{Q_R}{\tau_R} \quad (24b)$$



**Fig. 12** – Illustrating the graphical determination of  $\tau_{BF}$  and  $\tau_{BR}$ .

(The disappearance of the negative sign in Eq. (24b) is due to the reversal of direction of  $i_E$ .) The solution to Eq. (24a) is an *exponential transient* in  $Q_R$  governed by the *time constant*  $\tau_{BR}$ , which we find graphically by again observing  $v_O$ .

**MC9:** With power off, assemble the circuit of Fig. 11a. Apply power, and while monitoring  $v_I$  with Ch. 1 of the oscilloscope (DC mode), adjust the pulse generator so that  $v_I$  is a 100-kHz square wave alternating between 0 V and 1 V. With Ch. 1 of the oscilloscope triggered on the leading edge of  $v_I$ , observe  $v_O$  with Ch. 2 (AC mode), and use the graphical technique of Fig. 12 to find  $\tau_{BF}$ . (For optimal visualization of  $v_O$ , you may wish to change the frequency of  $v_I$  from the initial suggested value of 100 kHz).

**Warning:** For this measurement to succeed, it is critical that you use short leads and bypass the supply with a 0.1- $\mu$ F and a 10- $\mu$ F capacitor connected in parallel and mounted in close proximity to the BJT. The 10- $\mu$ F capacitor is a polarized type, so make sure to connect the “-” side to ground and the “+” side to the supply! The polarized capacitor works well at low frequencies, the other at high frequencies, so together they provide good filtering over the entire frequency range of interest.

**MC10:** Repeat step MC9, but for the circuit of Fig. 11b. Find  $\tau_{BR}$  graphically, and then calculate  $\tau_R = \tau_{BR}/\beta_R$  using the value of  $\beta_R$  found in Step MC2. Compare  $\tau_R$  and  $\tau_F$ , and try justifying the big difference.

**C11:** Using the data gathered so far, find  $\tau_S$  via Eq. (19). Then, use Eq. (20b) to predict  $t_S$  for the inverter of Fig. 1 if  $Q_1$  is the *particular* BJT sample that you have just characterized, and  $v_I$  is a pulse alternating between  $V_L = -1$  V to  $V_H = 4$  V, in the manner of Fig. 5.

**SC12:** Use PSpice to plot the transient response of the inverter of Fig. 1 if  $Q_1$  is the *particular* BJT sample that you have just characterized and  $v_I$  is a pulse alternating between  $V_L = -1$  V to  $V_H = 4$  V, in the manner of Fig. 5. Then, find  $t_1$  through  $t_6$ , as well as the storage time  $t_S$ . Compare with the value of  $t_S$  predicted in Step C11, and justify any differences.

**Remark:** For a realistic simulation, you again need to override the BJT parameters assumed by PSpice, which are typical, and impose those found experimentally. Thus, in addition to the values of  $I_S$ ,  $\beta_F$ , and  $\beta_R$  already considered, we need to specify those of  $C_{jc0}$ ,  $C_{je0}$ ,  $\tau_F$ , and  $\tau_R$ . Your complete model statement for  $Q_1$  will thus look like:

```
.model Q2N2222 NPN(Is=* Bf=* Br=* Cjc=* Cje=* Tf=* Tr=*)
```

where the asterisks again indicate experimental values, such as: ( . . . CJE=10pF TF=0.5ns . . . ). You also need to provide the values of  $\phi_c$ ,  $\phi_e$ ,  $m_c$ , and  $m_e$ . As mentioned, for these parameters we use the values specified in the 2M2222 model available in PSpice’s library. These are:

```
(Mjc=0.3416 Vjc=0.75 Mje=0.377 Vje=0.75)
```

**M13:** With power off, assemble the inverter of Fig. 1, using the BJT sample that you have just characterized. (Keep leads short, and bypass the supply with a 0.1- $\mu$ F and a 10- $\mu$ F capacitor mounted in parallel in close proximity to the BJT.) Next, using Ch 1 of the oscilloscope to monitor the pulse generator, adjust it so that  $v_I$  is a 200-kHz square wave alternating between  $V_L = -1$  V to  $V_H = 4$  V, in the manner of Fig. 5. Finally, apply power, observe  $v_O$  with Ch. 2 of the oscilloscope (DC mode), and measure  $t_1$  through  $t_6$ . (For optimal visualization of  $v_O$ , you may wish to change the frequency of  $v_I$  from its initial suggested value of 200 kHz). Compare the storage time  $t_S$  with the value found in step SC12, and justify any differences.

**M14:** For the inverter of step M13, investigate how  $t_D$ ,  $t_F$ ,  $t_S$ ,  $t_R$ , and  $t_{RR}$  are effected by:

- Lowering  $V_L$  to  $-3$  V while keeping  $V_H = 4$  V
- Letting  $V_L = 0$  V and  $V_H = 5$  V
- Reducing the *width* of the  $v_I$  pulse, with  $V_L = 0$  V and  $V_H = 5$  V, until its falling edge ( $t_3$ ) coincides with the instant in which the BJT reaches the EOS ( $t_2$ ).

In each of the above cases, justify qualitatively any changes in terms of charge-control analysis.

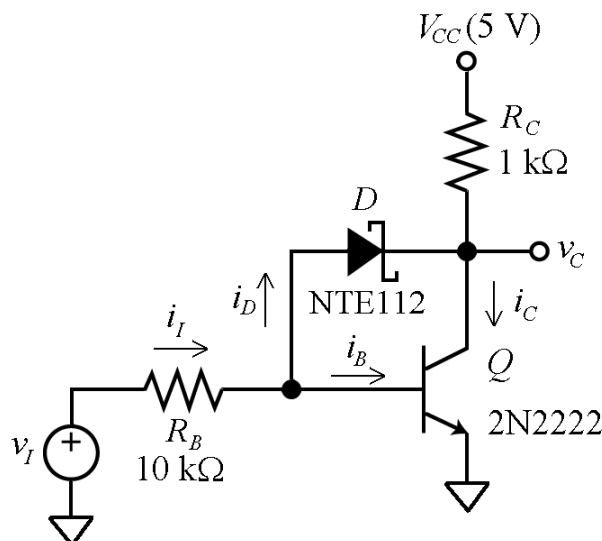
### Schottky Clamp:

It is apparent that the storage time  $t_S$  plays a dominant role in propagation delay of a BJT inverter. Mercifully, this time can be eliminated altogether by using a *Schottky-barrier diode* (SBD) clamp, as depicted in Fig. 13. A key feature of an SBD is a forward voltage drop *a few tenths of a volt less* than that of a silicon *pn* junction, typically  $V_{D(\text{on})} \cong 0.4$  V. Placing an SBD in parallel with the *B-C* junction, which typically needs  $V_{BC(\text{on})} \cong 0.7$  V to be convincingly forward biased, will prevent any convincing buildup of  $Q_R$  when we try to saturate the BJT: the overdrive base current  $i_{BS}$  is simply diverted through the SBD into the collector. Moreover, since the latter is clamped at  $V_{CE} = V_{BE(\text{on})} - V_{D(\text{on})} \cong 0.7 - 0.4 = 0.3$  V, that is, at  $V_{CE} > V_{CE(\text{sat})} \cong 0.1$  V, the BJT is prevented from going past the EOS, where there would be a buildup of  $Q_S$ . In the absence  $Q_S$ , there are no storage effects and we thus have  $t_S = 0$ .

An SBD is fabricated by forming a contact between a *metal* such as aluminum and a *lightly doped n-type semiconductor*. Since in both materials conduction takes place by majority carriers (electrons), an SBD exhibits *no charge storage effects*, another key feature of SBDs. However, like a conventional *pn* diode, an SBD exhibits a junction capacitance  $C_j$ , which in the arrangement of Fig. 13 is in parallel with  $C_{jc}$ . This results in a slight increase in  $t_D$ ,  $t_F$ ,  $t_R$ , and  $t_{RR}$  – a price well worth paying for the complete elimination of  $t_S$ !

**M15:** With power off, assemble the circuit of Fig. 13, but with the left terminal of  $R_B$  initially connected  $V_{CC}$  (that is, make  $v_I = 5$  V). Apply power, and with the DC ammeter inserted in *series*, measure the currents  $i_I$ ,  $i_B$ ,  $i_D$ , and  $i_C$ . Next, with the DC voltmeter connected in *parallel*, measure the voltage drops  $V_{BE}$ ,  $V_D$ , and  $V_{CE}$ . From the value  $V_{CE}$ , as well as the value of the ratio  $i_C/i_B$ , what do you conclude about the region of operation of the BJT?

**C16:** Using the values of  $I_D$  and  $V_D$  of Step M15, calculate the SBD's saturation current as



**Fig. 13** – Using a Schottky barrier diode to prevent a BJT from saturating.

$$I_s = I_D / e^{V_D / (26 \text{ mV})} \quad (25)$$

**M17:** Repeat Step M13, but with the SBD in place. Compare the various delays with and without the SBD, and comment on your results, especially  $t_s$ .

**MC18:** Following a procedure analogous to that of Step MC7, find the SBD's junction capacitance  $C_{j0}$ .

**S19:** Simulate the inverter of Step M17 via PSpice, compare the various delays of your simulations with those observed experimentally in Step M17, and account for any differences.

**Remark:** For a realistic simulation, you need to specify a model for the SBD, which in our simplified characterization takes on the form

```
.model D      D( IS=*  CJO=* )
```

where the asterisks indicate the values found experimentally, such as: (  $I_S=200\text{pA}$   $C_{J0}=2\text{pF}$  )

**MS20:** How does the presence of the SBD affect the noise margins of your inverter? Investigate by displaying its VTC both on the oscilloscope and via PSpice. Compare, and comment.