SFSU - ENGR 453 – DIGITAL IC DESIGN LAB

# LAB #2: CHARACTERIZATION OF CMOS GATES

Updated Feb. 25, 2005.

## Objective:

To characterize different types of CMOS gates (Inverters, NAND and NOR gates, and Transmission gates). To compare PSpice simulations with experimental observations.

## Components:

1 × CD4007UB MOSFET Array, 2 × 0.1 μF capacitors, and resistors: 1 × 100 Ω, 1 × 10 kΩ (5%, ¼ W).

## Instrumentation:

A bench power supply, a triangular-wave generator, a pulse generator, a digital multi-meter, and a dual-trace oscilloscope with X10 probes.

## PART I – THEORETICAL BACKGROUND

The *threshold voltage* of an *n*MOSFET is

$$V_{tn} = V_{tn0} + \gamma_n \left( \sqrt{2|\phi_p| + V_{SB}} - \sqrt{2|\phi_p|} \right) \qquad (1)$$

where $V_{tn0}$ is the threshold voltage with $V_{SB} = 0$, $\gamma_n$ is the *body-effect coefficient*, and $\phi_p \cong -0.3$ V. For an *n*MOSFET we must always have $V_{SB} \geq 0$ V, this being the reason why in ICs the body of *n*MOSFETs is always tied to the *most negative voltage* (MNV). An *enhancement n*MOSFET has $V_{tn0} > 0$, so rising $V_{SB}$ above 0 V will make $V_{tn}$ even *more positive*.

For $v_{GS} \leq V_{tn}$, the *n*MOSFET is in cutoff. For $v_{GS} \geq V_{tn}$, the *n*MOSFET is on, and it operates either in the *saturation* region (also called *active* region) , or in the *triode* region (also improperly called the *linear* region), depending on the range of values of $v_{DS}$. Specifically, for $v_{DS} \geq v_{GS} - V_{tn}$ the device operates in *saturation*, where we have

$$i_{D(\text{Sat})} = \frac{k_n}{2} (v_{GS} - V_{tn})^2 \times (1 + \lambda_n v_{DS}) \qquad (2)$$

while for $v_{DS} \leq v_{GS} - V_{tn}$ it operates in the *triode* region, where we have

$$i_{D(\Omega)} = k_n[(v_{GS} - V_{tn})\, v_{DS} - \frac{1}{2} v_{DS}^2\, ] \times (1 + \lambda_n v_{DS}) \qquad (3)$$

In the above equations, $k_n$ is the *device transconductance parameter*, and $\lambda_n$ is the *channel-length modulation parameter.* In DC calculations it is customary to assume $\lambda_n = 0$ for simplicity. We also have

$$k_n = k'_n \frac{W_n}{L_n} \qquad (4)$$

where $k'_n$ is the *process transconductance parameter*, and $W_n$ and $L_n$ are the channel *width* and *length*.

 

In *saturation* an *n*MOSFET exhibits *current-source* behavior, while near the origin of its $i_D$-$v_{DS}$ characteristic it exhibits *resistive* behavior. In fact, ignoring $v_{DS}^2$ as well as $\lambda_n v_{DS}$ near the origin, we obtain $i_{D(\Omega)} \cong k_n(v_{GS} - V_{tn})v_{DS}$, indicating an *approximately linear* dependence of $i_D$ upon $v_{DS}$. The reciprocal of the slope of the $i_D$-$v_{DS}$ curve is the *channel resistance* near the origin,

$$r_{DSn} = \frac{1}{k_n(v_{GS} - V_{tn})} \tag{5}$$

This expression indicates *voltage-controlled resistance* behavior, with $v_{GS}$ being the control voltage. Note that $r_{DSn}$ depends also on the body bias via $V_{tn}$. Moreover, the larger the value of $k_n$, the smaller $r_{DSn}$.

Dual considerations hold for *p*MOSFETs, provided we *reverse voltage polarities* and *current directions*. Thus, the *threshold voltage* of a *p*MOSFET is

$$V_{tp} = V_{tp0} - \gamma_p \left( \sqrt{2\phi_n + V_{BS}} - \sqrt{2\phi_n} \right) \tag{6}$$

where $V_{tp0}$ is the threshold voltage for $V_{BS} = 0$, $\gamma_p$ is the *body-effect coefficient*, and $\phi_{fp} \cong -0.3$ V. For a *p*MOSFET we must always have $V_{BS} \geq 0$ V, this being the reason why in ICs the body of *p*MOSFETs is always tied to the *most positive voltage* (MPV). An *enhancement p*MOSFET has $V_{tp0} < 0$, so rising $V_{BS}$ above 0 V will make $V_{tp}$ even *more negative*.

For $v_{SG} \leq |V_{tp}|$, the *p*MOSFET is in cutoff. For $v_{SG} > |V_{tp}|$, the *p*MOSFET is on, and it operates either in the *saturation* region (also called *active* region) , or in the *triode* region (also called *linear* region), depending on the range of values of $v_{SD}$. Specifically, for $v_{SD} \geq v_{SG} - |V_{tp}|$, the device operates in *saturation*, where we have

$$i_{D(\mathrm{PO})} = \frac{k_p}{2}(v_{SG} - |V_{tp}|)^2 \times (1 + \lambda_p v_{SD}) \tag{7}$$

while for $v_{SD} \leq v_{GS} - |V_{tn}|$ it operates in the *triode* region, where we have

$$i_{D(\Omega)} = k_p[(v_{SG} - |V_{tp}|)\, v_{SD} - \frac{1}{2} v_{SD}^2\,] \times (1 + \lambda_p v_{SD}) \tag{8}$$

In the above equations, $k_p$ is the *device transconductance parameter*, *and* $\lambda_p$ is the *channel-length modulation parameter.* In DC calculations it is customary to assume $\lambda_p = 0$ for simplicity. We also have

$$k_p = k'_p \frac{W_p}{L_p} \tag{9}$$

where $k'_p$ is the *process transconductance parameter*, and $W_p$ and $L_p$ are the channel *width* and *length*.

In *saturation,* a *p*MOSFET exhibits *current-source* behavior, while near the origin of its $i_D$-$v_{SD}$ characteristic it exhibits *resistive* behavior. In fact, ignoring $v_{SD}^2$ as well as $\lambda_n v_{SD}$ near the origin, we obtain $i_{D(\Omega)} \cong k_p(v_{SG} - |V_{tp}|)v_{SD}$, indicating an approximately linear dependence of $i_D$ upon $v_{SD}$. The reciprocal of the slope of the $i_D$-$v_{SD}$ curve is the *channel resistance* near the origin,

$$r_{SDp} = \frac{1}{k_p(v_{SG} - |V_{tp}|)} \quad (10)$$

This expression indicates *voltage-controlled resistance* behavior, with $v_{SG}$ being the control signal. Note that $r_{SDp}$ depends also on the body bias via $V_{tp}$. Moreover, the larger the value of $k_p$, the smaller $r_{SDp}$.

## VTCs and Noise Margins:

The most basic logic circuit is the *inverter*. To build a complex digital system we need more sophisticated logic circuits such a NAND and NOR gates, flip-flops, encoders/decoders, registers, and memories. However, when it comes to the *study of electrical properties*, the basic inverter, in spite of its simplicity, is fairly representative of most logic circuits, so we find it appropriate to investigate it in proper detail.

As a signal produced by a *transmitting gate* travels down a wire, it picks up various forms of noise, so by the time it reaches a *receiving gate* it may be appreciably contaminated. The question arises as to *how much noise* can be tolerated at the receiving end and still allow for the signal to be interpreted correctly there. A logic family's ability to function correctly in noisy environments is measured via its *noise margins*.

As shown in Fig. 1($a$), an inverter is powered between $V_S$ (typically 5 V) and ground. Circuit behavior is best visualized via the *voltage transfer curve* (VTC), representing the plot of $v_O$ versus $v_I$. Figure 1($b$) shows the idealized VTC. For $v_I < 0.5V_S$ the circuit gives $v_O = V_S$ (= $V_{OH}$), and for $v_I > 0.5V_S$ it gives $v_O = 0$ V (= $V_{OL}$). The VTC of a practical inverter will generally depart from this idealized shape, and will look more like that of Fig. 1($c$). Here we observe that as long as $v_I$ is *sufficiently low* (near 0V), the inverter gives $v_O = V_{OH}$ (note that $V_{OH}$ is not necessarily $V_S$); as long as $v_I$ is *sufficiently high* (near $V_S$), the inverter gives $v_O = V_{OL}$ note that $V_{OL}$ is not necessarily 0 V).

The departure of a practical VTC from the ideal is specified in terms of the *noise margins*, defined as

$$NM_L = V_{IL} - V_{OL} \quad (11a)$$

$$NM_H = V_{OH} - V_{IH} \quad (11b)$$

where $V_{IL}$ and $V_{IH}$ are the values of $v_I$ corresponding to the points of the VTC where *slope* is –1 V/V. Physically, the noise margins represent the *maximum amount of noise* that can be tolerated on a line going

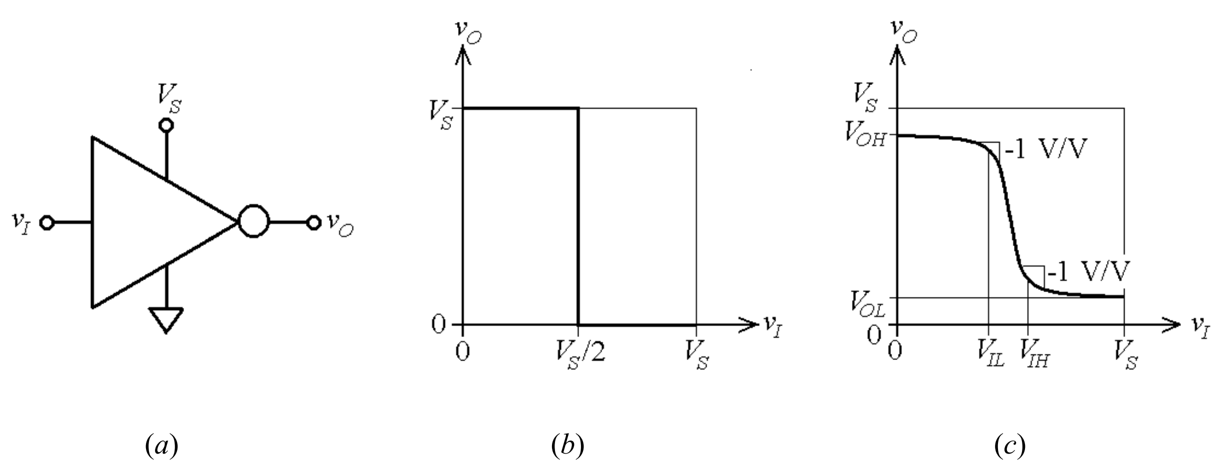


**Fig. 1** – ($a$) Logic inverter. ($b$) Idealized VTC, and ($c$) practical VTC.

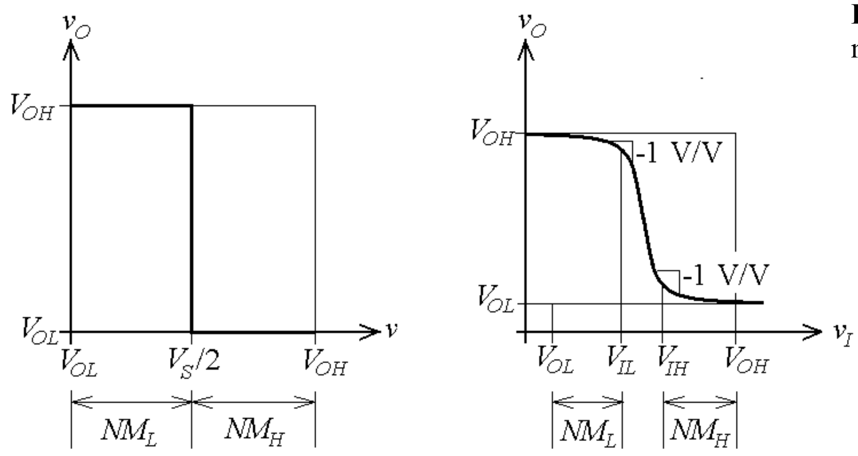


**Fig. 2** – Visualizing the noise margins

from the output of a transmitting gate to the input of a receiving gate. As illustrated further in Fig. 2, any noise in excess of this margin will be amplified by the receiving gate by *more than unity*, potentially leading to erroneous circuit behavior. Clearly, the higher the noise margins, the better. For the idealized VTC of Fig. 1(*b*) we have $NM_L = NM_H = 0.5V_S$ (= 2.5 V for $V_S$ = 5 V).

VTCs are readily visualized with a dual-trace oscilloscope operated in the *x-y* mode, or via PSpice using a DC Sweep. Figure 3 shows a PSpice circuit to display both the *voltage transfer curve* (VTC) and the *current transfer curve* (ITC) of a CMOS inverter consisting of two homebrew MOSFETs, called respectively 453nMOSFET and 453pMOSFET. Both devices were created by renaming and suitably editing the *PSpice Models* of two MOSFETs available in the PSpice Library. This has been done first by clicking the device to select it, then by clicking **Edit** → **PSpice Model** to change the values of its parameters. Following are the model statements for the two devices:

```
.model 453nMOSFET     NMOS(W=4u L=1u kp=50u Vto=1 lambda=0.01)

.model 453pMOSFET     PMOS(W=8u L=1u kp=20u Vto=-1.5 lambda=0.02)
```

The two curves are shown in Fig. 4.

As depicted in the VTC display at the top, the input sweep carries the two MOSFETs, denoted respectively as $M_p$ and $M_n$, thorough the regions shown (CO indicates the *cutoff* region, Ω the *ohmic*

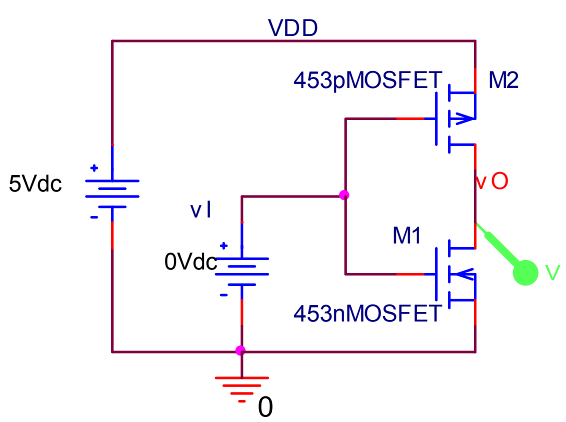


**Fig. 3** – PSpice circuit to display the VTC and ITC of a CMOS inverter.

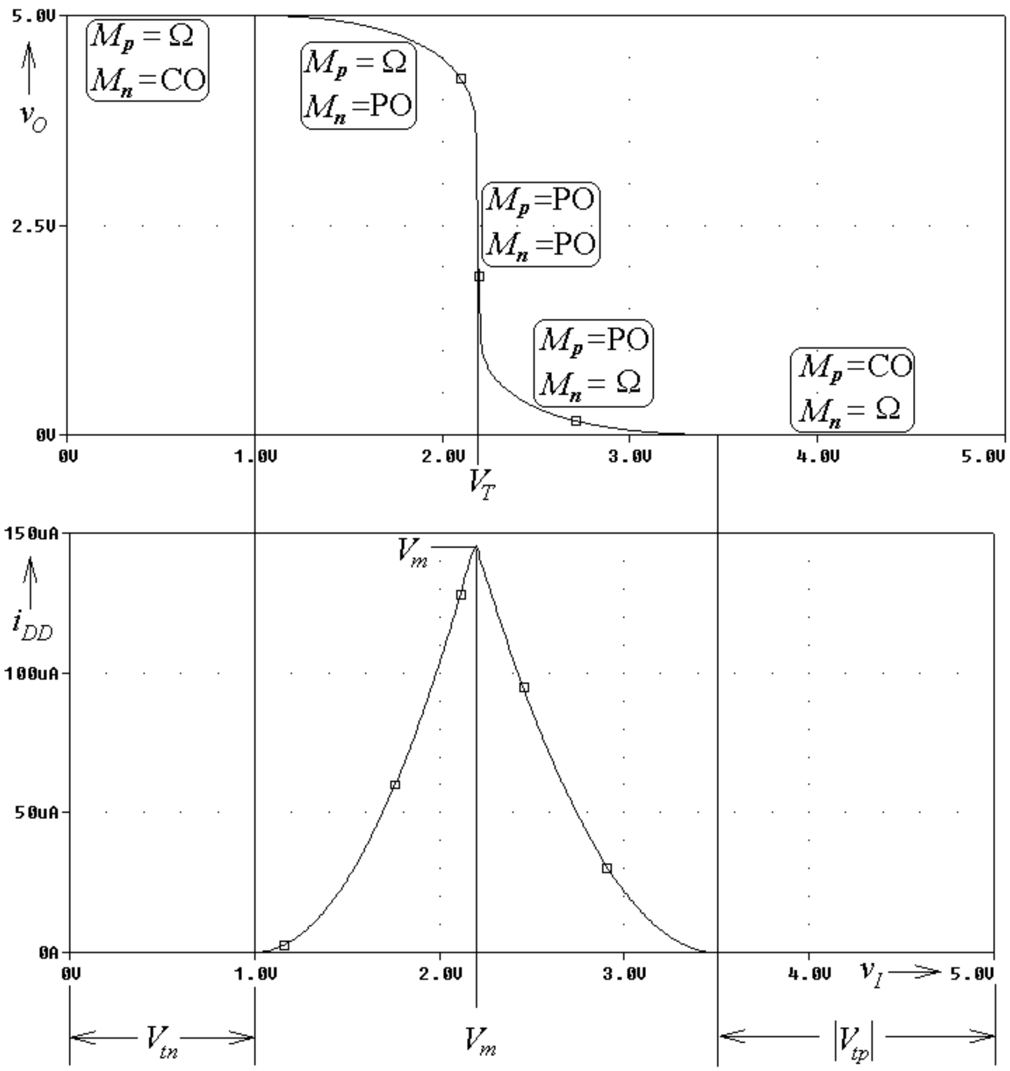


**Fig. 4 -** Voltage (top) and current (bottom) transfer curves for the CMOS inverter of Fig. 3.

region, and PO the *pinch-off* region). One can use simple graphical techniques to identify the points where slope is –1 V/V and thus find $V_{IL}$ and $V_{IH}$. Then, one calculates the noise margins via Eq. (11).

The central portion of the VTC, where both MOSFETs are in PO and *slope* is the *steepest*, is of great interest in *analog applications*. The slope $a = dv_O/dv_I$ there represents *voltage gain*. The value of $v_I$ around which this region is centered shall be called the *trip voltage* $V_T$. We observe that because of differences in the parameters of the *n*MOSFETs and *p*MOSFETs, the trip voltage $V_T$ is not necessarily halfway between 0 V and $V_{DD}$, that is, in general we have $V_T \neq \frac{1}{2}V_{DD}$.

Also shown in Fig. 4, bottom, is the plot of the current $i_{DD}$ drawn by the inverter from its supply $V_{DD}$ as a function of $v_I$. This current is zero both for $v_I \leq V_{tn}$, where the *n*MOSFET is in CO, and for $v_I \geq (V_{DD} - |V_{tp}|)$, where the *p*MOSFET is in CO. However, for $V_{tn} \leq v_I \leq (V_{DD} - |V_{tp}|)$, both MOSFETs conduct, and the current exhibits a bell-shaped profile. Its maximum shall be denoted as $I_m$, and the value of $v_I$ at which it occurs shall be denoted as $V_m$. Near this point *both* FETs are operating in PO. In general $V_m$ and $V_T$ are not necessarily identical, though very close.

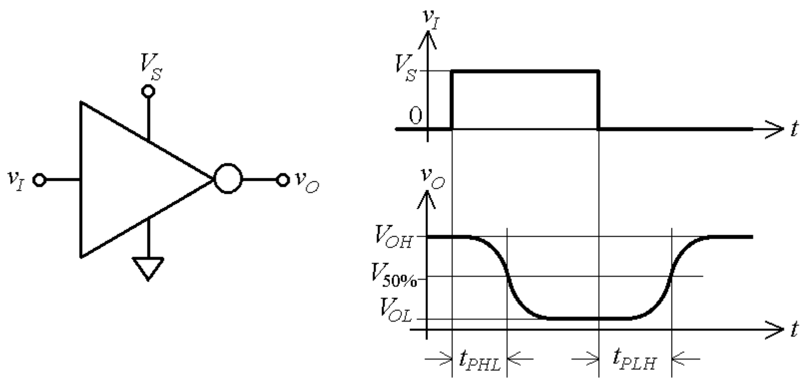


**Fig. 5** – Illustrating the propagation delays.

You can simulate the above inverter on your own by downloading its appropriate files from the Web. To this end, go to http://online.sfsu.edu/~sfranco/CoursesAndLabs/Labs/301Labs.html, and once there, click on **PSpice Examples**. Then, follow the instructions contained in the **Readme** file.

**Propagation Delays:**

An inverter's response to a sharp-edged input pulse is not instantaneous, as the circuit takes a certain amount of time to swing its output from one level to the other (see Fig. 5). The speed of response is characterized in terms of the *propagation delays* $t_{PLH}$ and $t_{PHL}$. The amount of time, following the *leading* edge $v_I$, that it takes for $v_O$ to swing from $V_{OH}$ down to the transition's *midpoint*, defined as

$$V_{50\%} = \frac{V_{OL} + V_{OH}}{2} \tag{12}$$

is denoted as $t_{PHH}$. Likewise, the amount of time, following the *trailing* edge of $v_I$ , that it takes for $v_O$ to swing from $V_{OL}$ up to $V_{50\%}$ is denoted as $t_{PLH}$. The two delays are not necessarily identical, so their average

$$t_P = \frac{t_{PLH} + t_{PHL}}{2} \tag{13}$$

is aptly called the *average propagation delay*. In CMOS gates, the nonzero propagation delays stem from the parasitic capacitances internal to the MOSFETs that need to be charged/discharged in order to allow for the output to switch from one state to the other.

## PART II – EXPERIMENTAL PART

The purpose of this laboratory is to characterize a variety of gates implemented with the transistors of the CD4007UB MOSFET Array that you have characterized in Lab #1. For convenience, the pin diagram of this IC is repeated in Fig. 6. Beware that all wiring tips and experimental precautions stressed in Lab #1 still hold! If you damage the particular CD4007 sample you are working with, you'll need to characterize a new sample in order to ensure consistency between measurements and simulations. Transistors belonging to the *same* IC sample are indeed matched to a good degree, but no matching can be expected between *different* IC samples.

Henceforth, steps shall be identified by letters as follows: **C** for calculations, **M** for

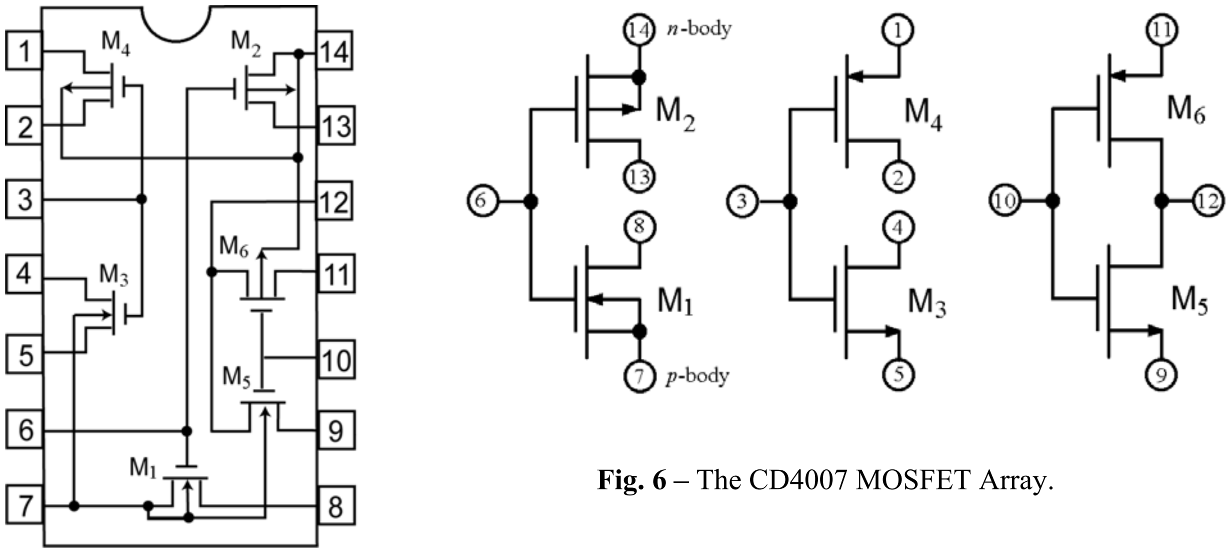


**Fig. 6** – The CD4007 MOSFET Array.

measurements, **P** for pre-lab preparations, and **S** for Spice simulations. As usual, all data must be expressed in the form $X \pm \Delta X$.

## Basic CMOS Inverter

**PC1:** Using the *n*MOSFET and *p*MOSFET values of $V_{t0}$ and $k$ determined in Lab #1, predict the *noise margins* of the CMOS inverter of Fig. 7*a*, as well as the *trip voltage* $V_T$.

***Hint:*** (*a*) To find $V_{IL}$, impose $i_{Dn(\mathrm{PO})} = i_{Dp(\Omega)}$ (use $\lambda_n = \lambda_p = 0$ for simplicity; also, note that $v_{GSn} = v_I$; $v_{SGp} = V_{DD} - v_I$, and $v_{SDp} = V_{DD} - v_O$). Next, differentiate both sides with respect to $v_I$, impose $dv_O/dv_I = -1$, and calculate at $v_I = V_{IL}$.

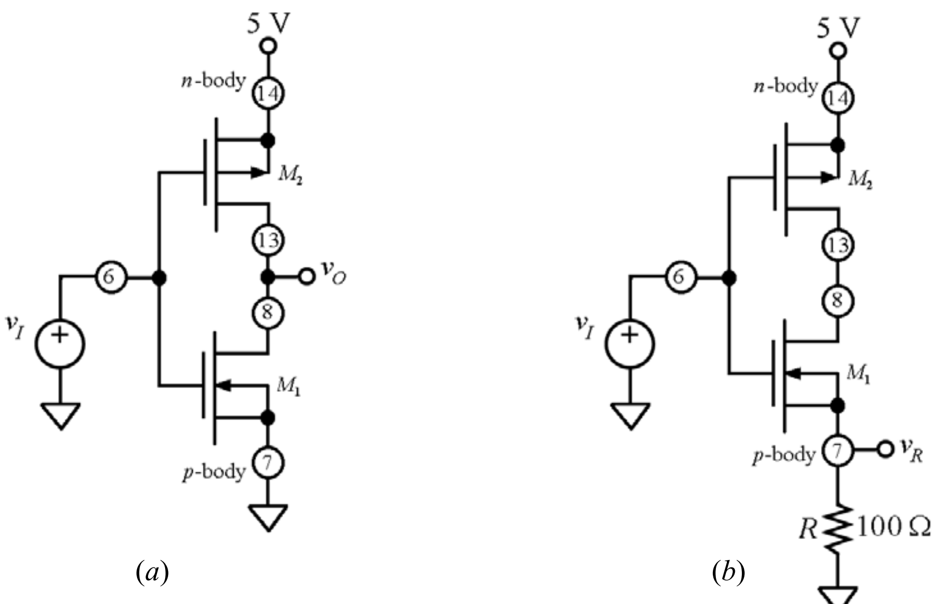


**Fig. 7** – (*a*) CMOS inverter: (*b*) Using *R* to sense the inverter's current.

($b$) To find $V_{IH}$, impose $i_{Dn(\Omega)} = i_{Dp(PO)}$ (again use $\lambda_n = \lambda_p = 0$, along with $v_{GSn} = v_I$, $v_{DSn} = v_O$, and $v_{SGp} = V_{DD}$ - $v_I$). Next differentiate both sides with respect to $v_I$, impose $dv_O/dv_I$, = –1, and calculate at $v_I = V_{IH}$.

($c$) To find $V_T$, impose $i_{Dn(PO)} = i_{Dp(PO)}$ (use $\lambda_n = \lambda_p = 0$ for simplicity, and note that $v_{GSn} = v_I$ and $v_{SGp} = V_{DD}$ - $v_I$,). Then, let $v_I \rightarrow V_T$, and solve for $V_T$.

**PS2:** Plot the VTC of the inverter of Step PC1 using PSpice, find $V_{IL}$, $V_{IH}$, $V_{OL}$, $V_{OH}$, and $V_T$ graphically, graphically, compute the noise margins, compare with predicted values, and justify any discrepancies.

**MC3:** Observe the VTC of the inverter of Step PC1 experimentally with the oscilloscope, determine $V_{IL}$, $V_{IH}$, $V_{OL}$, $V_{OH}$, and $V_T$ graphically, compute the noise margins, compare with those of Step PS2, and justify any discrepancies.

***Reminder***: To observe the VTC *experimentally*, first adjust the signal generator so that $v_I$ is a *triangular wave* of about 100 Hz and alternating between $V_{SS}$ (0 V) and $V_{DD}$ (5 V); adjust it while monitoring it with the oscilloscope. Next, switch the oscilloscope to the *x-y mode*, with $v_I$ as the *x* axis (Ch. 1, 1 V/div, DC), and $v_O$ as the *y* axis (Ch. 2, 1 V/div, DC). Before connecting the scope to your circuit, adjust the offsets of the two channels so that the origin of the *x-y* display (dot) is at the lower left corner of the screen. Also, keep the beam intensity suitably low to avoid burning out the phosphor on the CRT.

**PC4:** Using the *n*MOSFET and *p*MOSFET values of $V_{t0}$ and $k$ determined in Lab #1, predict the values of $V_m$ and $I_m$ for the inverter of Fig. 7*a*. (Recall that $I_m$ is the maximum value of $i_{DD}$, and $V_m$ is the value of $v_I$ at which this maximum occurs.)

***Hint:*** To find $V_m$, impose $i_{Dn(PO)} = i_{Dp(PO)}$ (use $\lambda_n = \lambda_p = 0$ for simplicity, and note that $v_{GSn} = v_I$ and $v_{SGp} = V_{DD} - v_I$,). Then, let $v_I \rightarrow V_m$, and solve for $V_m$; next, find $I_m$ by calculating $i_{Dn(PO)}$ at $v_{GSn} = V_m$.

**PS5:** Use PSpice to plot $i_{DD}$ versus $v_I$ for the inverter of Step PC4, find $I_m$ and $V_m$ graphically, compare with those of Step PC4, and justify any discrepancies.

**M6:** Observe the plot of $i_{DD}$ versus $v_I$ for the inverter of Step PC4 *experimentally*; find $I_m$ and $V_m$ graphically, compare with those of Step PS5, and justify any discrepancies.

***Hint:*** To be able to observe $i_{DD}$ on the oscilloscope, lift Pin 7 off ground and insert a small (100 Ω) current-sensing resistance in series between Pin 7 and ground, as shown in Fig. 7*b*, and use $v_R$ to drive the *y* axis of your display. Clearly, $i_{DD} = v_R / R$.

## Buffered CMOS Inverter

The VTC of the basic inverter of Fig. 7*a* can be improved considerably by *buffering* it with one or more additional inverters. To retain the logic function of inversion, *two* additional inverters are needed in this case. The resulting circuit, shown in Fig. 8, is aptly called a *buffered inverter* (by contrast, that of Fig. 7*a* is an *unbuffered inverter*).

**MC7:** With power off, assemble the circuit of Fig. 8. Then, apply power, and use the oscilloscope to display the VTC from Pin 6 to Pin 3, then the VTC from Pin 6 to Pin 10, and finally the VTC from Pin 6 to Pin 12. You will observe a progressive increase in the squareness of the VTCs as you move the probe from Pin 3 to Pin 10 to Pin 12. How do you justify this? Finally, find the noise margins of the buffered inverter, compare with those of its unbuffered counterpart, and comment on the significant improvement..

## Propagation Delays:

**MC8:** Adjust the pulse generator for a train of pulses alternating between 0 V and 5 V, and a period of about 1 μs; use Ch. 1, 1 V/div, DC. Apply it to the inverter of Fig. 7*a*, and monitor the output with Ch. 2,

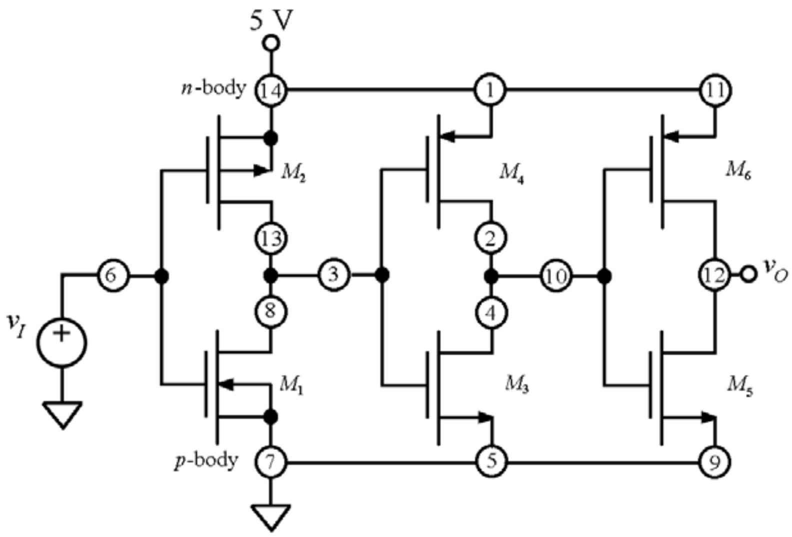


**Fig. 8** - Buffered CMOS inverter:

1 V/div, DC. Adjust the pulse generator frequency until the waveforms look approximately as in Fig. 5, and measure $t_{PLH}$ and $t_{PHL}$. Beware that $t_{PLH}$ and $t_{PHL}$ are not necessarily equal, due to the different current-driving capabilities of the two transistors. Finally, calculate $t_P$.

***Warning:*** Don't forget to take into account the effects of probe loading, as discussed in connection with Step M12 of Lab # 1. For this measurement, it is critical that you use a low-input capacitance probe, such as a X10 probe as discussed in Appendix 2. Also, make sure that your probe is properly compensated, and keep all leads short to reduce the effect of stray capacitances!

**MC9:** Repeat Step MC8, but for the buffered inverter of Fig. 8. Compare with the delays of its unbuffered counterpart, and comment. Clearly, the price for the better noise margins of buffered gates is increased circuit complexity and delay.

## The Power-Delay Product

The *power-delay product* (PDP), defined as the product of the *average power dissipation per gate PDP* and the gate's *average propagation delay* $t_P$, represents a figure of merit of a particular logic family, and allows for comparison among different families. To find this parameter, we operate our three inverters as a *ring counter*, we measure its period of oscillation $T$ as well as the average current $I_{DD}$ it draws from the $V_{DD}$ supply. We then find the average power dissipation per gate $P_D = (1/3)V_{DD} \times I_{DD}$, and the average gate delay as $t_P = T/6$, and finally we take their product $PDP = P_D \times t_P$.

**MC10:** With power off, disconnect the input pulse generator from the circuit of Fig. 8, and connect Pin 6 to Pin 12 to make the circuit work as a *ring counter*. Moreover, insert the digital current meter in *series* between the power supply $V_{DD}$ and the common node formed by Pins 14-1-11. Now turn power on, and measure the *average current* $I_{DD}$ drawn by your ring counter from the $V_{DD}$ supply, as well at the period of oscillation $T$. Finally, compute the *PDP* as indicated above

### NOR and NAND Gates

Figure 9 show the interconnections for NOR and NAND gate operation. If we invert $v_O$ with an additional inverter made up of the remaining transistors $M_5$ and $M_6$, the inverter output will provide the OR and the AND functions, respectively. In anticipation of the measurements you are about to make, keep in mind that:

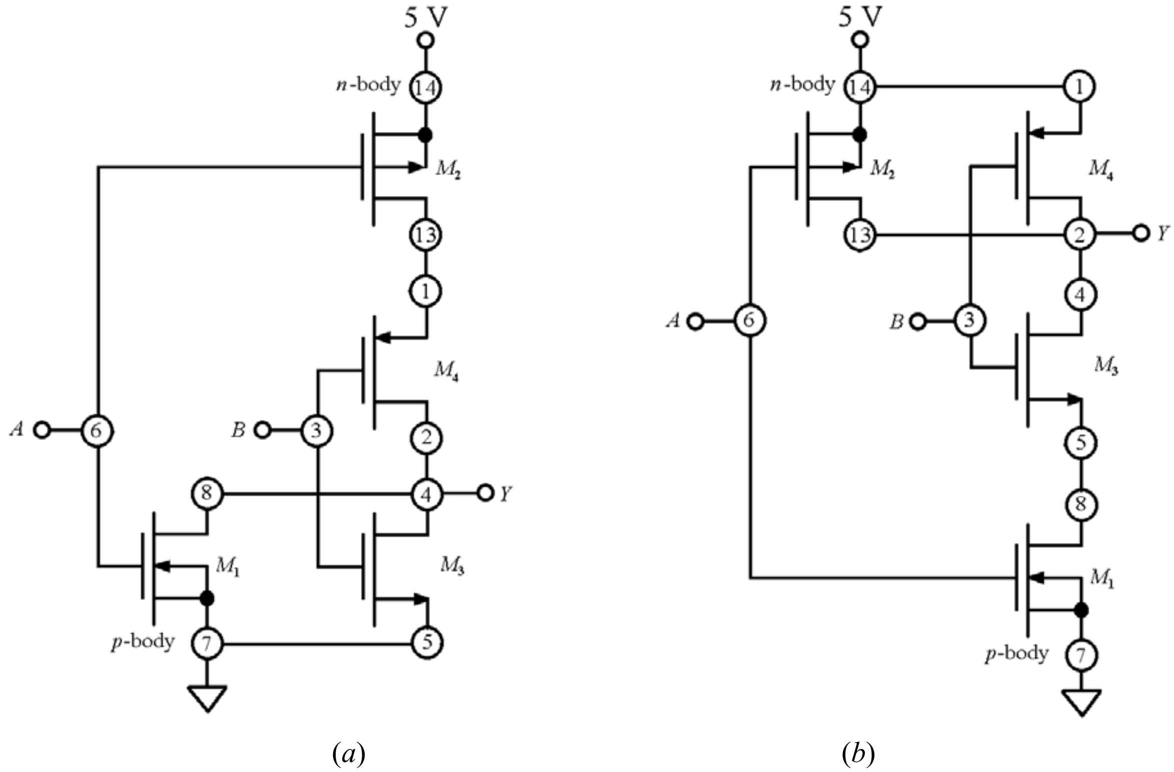


**Fig. 9** – NOR and NAND gates

- Two matched MOSFETS connected in *parallel* act as a single MOSFET with a *channel width twice* as long, effectively *doubling* the device transconductance parameter *k*.
- Two matched MOSFETS connected in *series* act as a single MOSFET with a *channel length twice* as long, effectively *halving* the device transconductance parameter *k*.

**MC11:** With power off, assemble the NOR gate of Fig. 9*a*. Turn power on, and with the inputs tied together to make the gate work as an inverter, observe the VTC with the oscilloscope and find the noise margins as well as the trip voltage. Next, measure the propagation delays (you'll find that one of them is significantly longer than the other; why?). Compare with the unbuffered inverter of Steps MC3 and MC8, and account for all differences.

**MC12:** With power off, configure $M_5$ and $M_6$ (see Fig. 6) as a logic *inverter*, and place it at the output of the NOR gate of Fig. 9*a* to turn it into an OR gate. Then, find the noise margins, trip voltage, and propagation delays of this AND gate. Compare them with those of the NOR gate, and justify all differences.

**MC13:** Repeat Steps MC11 and MC12, but for the NAND gate of Fig. 9*b*.

## Transmission Gates:

Many electronic systems call for an *electronically-controlled switch*, that is, a switch whose state is controlled not manually by a human, but electronically by another circuit. Figure 10 illustrates a typical example. Here, an input source producing an analog signal $v_S$ capable of assuming a continuum of values

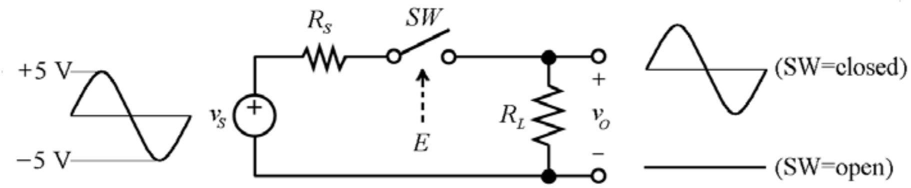


**Fig. 10** – Illustrating the transmission gate concept.

over the range –5 V ≤ $v_S$ ≤ +5V, is connected to a load $R_L$ via a *voltage controlled switch SW*, whose status is controlled by a binary control signal $E$ as follows:

- When $E$ = HIGH, $SW$ = closed, and $v_O = v_I$, indicating that the input is *transmitted* to the output
- When $E$ = LOW, $SW$ = open, and $v_O$ = 0 V, indicating that signal transmission is *inhibited*.

For obvious reasons, an electronically-controlled switch capable of transmitting or inhibiting analog signals is also called an *analog transmission gate*.

A good candidate for the role of electronic switch is an *n*MOSFET ($M_3$ in Fig. 11), where the channel forms the switch $SW$, and $v_{GS3}$ plays the role of the control voltage $E$. As we know, for $v_{GS3}$ = LOW (in practice, for $v_{GS3} < V_{tn}$), $M_3$ is in cutoff and its channel acts as an open switch. However, for $v_{GS3}$ = HIGH (in practice, for $v_{GS3} >> V_{tn}$), $M_3$ will be heavily on. If the voltage $v_{DS3}$ across its channel is sufficiently small, the channel will, according to Eq. (5), act as a small resistance $r_{DSn}$, effectively approximating a closed switch. Clearly, we'd like this resistance to be as small as possible.

Given that the supply voltages in Fig. 11 are $V_{DD}$ = +5V and $V_{SS}$ = –5V, the voltage levels of the

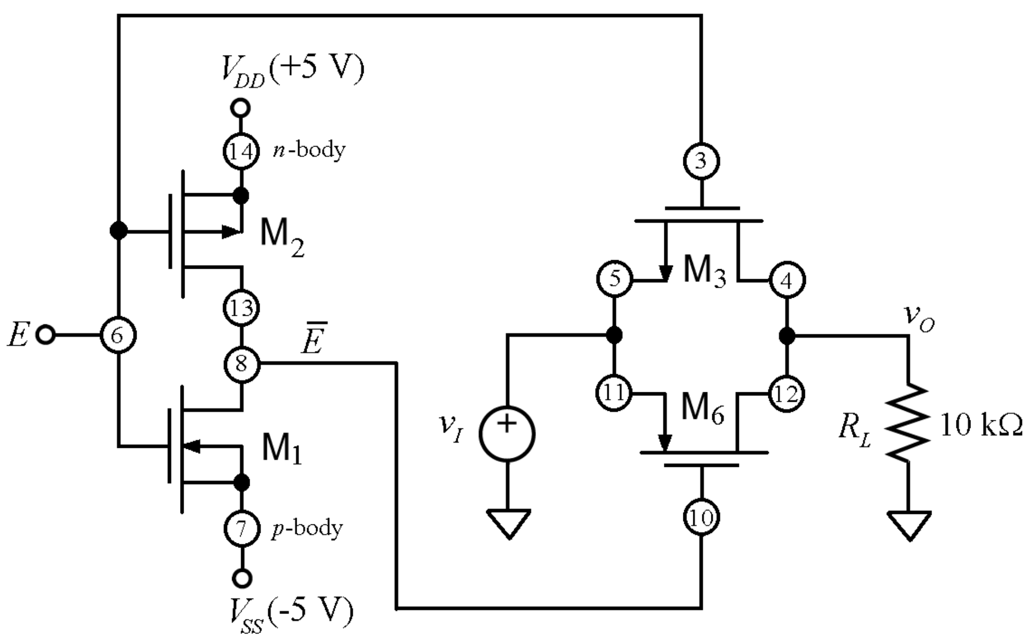


**Fig. 11** – CMOS realization of a transmission gate.

control signal $E$ are likewise HIGH = +5V and LOW = –5 V. Recall that for proper operation, the body of the $n$MOSFETs (Pin 7) must be connected to the MNV (–5V, in our example), indicating that $M_3$ has

$$v_{SB3} = v_I - V_{SS} = v_I + 5 \text{ V} \tag{14}$$

Consequently, $V_{tn3}$ will be a function of $v_I$ itself, as per Eq. (1). Also, for $E$ = HIGH = 5 V, $M_3$ has

$$v_{GS3} = E - v_I = 5 \text{ V} - v_I \tag{15}$$

The channel resistance $r_{DSn}$ of the $n$MOSFET $M_3$ is smallest when $v_I$ is near the *low-end* of its range (–5 V), where $v_{SB3} = 0$ and $v_{GS3} = 10$ V. As $v_I$ is increased from –5 V, $v_{S3}$ increases, and so does $V_{tn3}$, by Eq. (1); at the same time, $v_{GS3}$ decreases. The combined effect is an undesirable increase in $r_{DSn}$, by Eq. (5). In fact, for $v_I$ sufficiently positive to make $v_{GS3} = V_{tn3}$, $M_3$ will turn off, operating as an open switch when in fact it should be closed! Increasing $v_I$ further will simply continue to keep $M_3$ in cutoff. The behavior of $r_{DSn}$ as a function of $v_I$ is depicted in Fig. 12.

The above drawback is overcome by using a $p$MOSFET ($M_6$ in Fig. 11) in *parallel* with the $n$MOSFET, and driving its gate in *anti-phase* with that of the $n$MOSFET. The inversion of the control signal $E$ is accomplished by the inverter made up of $M_1$ and $M_2$. Recall that for proper operation, the body of the $p$MOSFETs (Pin 14) must be connected to the MPV (+5V, in our example), indicating that $M_6$ has

$$v_{BS6} = V_{DD} - v_I = 5 \text{ V} - v_I \tag{16}$$

Moreover, for $E$ = HIGH = +5 V, we have $\overline{E}$ = LOW = –5 V, so

$$v_{SG6} = v_I - \overline{E} = v_I + 5 \text{ V} \tag{17}$$

By dual reasoning, we observe that the channel resistance $r_{SDp}$ of the $p$MOSFET $M_6$ is smallest when $v_I$ is near the *high-end* of its range (+5 V), where $v_{BS6} = 0$ and $v_{SG6} = 10$ V. As $v_I$ is decreased from +5 V, $v_{BS6}$ increases, and so does $|V_{tp6}|$, by Eq. (6); at the same time, $v_{SG6}$ decreases, and the overall effect is an

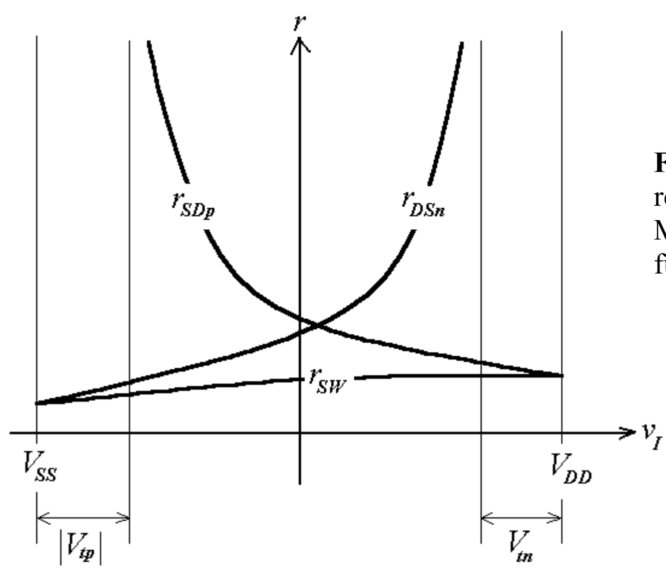


**Fig. 12** – The overall transmission-gate resistance $r_{SW}$, as well as the individual MOSFET resistances $r_{DSn}$ and $r_{SDp}$, as functions of $v_I$.

undesirable increase in $r_{SDp}$, by Eq. (10). In fact, for $v_I$ sufficiently negative to make $v_{SG6} = |V_{tp6}|$, $M_6$ will go in cutoff, operating as an open switch when in fact it should be closed! Decreasing $v_I$ further will simply continue to keep $M_6$ in cutoff. The behavior of $r_{SDp}$ as a function of $v_I$ is also depicted in Fig. 12. The *p*MOSFET will provide low-resistance over the portion of the $v_I$ range over which the *n*MOSFET fails, and vice-versa. Even though the individual FETs provide low channel resistance only over limited ranges of $v_I$, as a *team* they provide *low overall resistance* over the *entire* $v_I$ range!

**PC14:** Using the values of $k$, $V_{t0}$, and $\gamma$ found in Lab #1, calculate the *n*-channel resistance $r_{DSn}$ as well as the *p*-channel resistance $r_{SDp}$ for $v_I = -5$ V, $-4$ V,…, 0 V,…, +4 V, + 5V. Hence, plot $r_{DSn}$, $r_{SDp}$, as well as the overall switch resistance $r_{SW} = r_{DSn}//r_{SDp}$ over the range $-5 \text{ V} \le v_I \le +5\text{V}$. Comment on your findings. ***Hint:*** Use Eqs. (1), (5), (6), (10), and Eqs. (14) through (17).

**M15:** With power (both $V_{DD}$ and $V_{SS}$) off, assemble the transmission gate of Fig. 11. Next, adjust your waveform generator so that $v_I$ is a 1-kHZ sine-wave alternating between −3 V and +3 V (use Ch. 1 of the oscilloscope, 1 V/div, DC). Now, apply power, connect your generator to the transmission gate, and while monitoring its output with the oscilloscope (use Ch. 2, 1 V/div, DC), verify that with $E = +5$ V your circuit yields $v_O \cong v_I$, but with $E = -5$ V it yields $v_O = 0$ V.

***Remark:*** You will observe that $v_O$ is slightly smaller than $v_I$. Explain why, and use the results of step PC12 to justify quantitatively.

**M16:** Disconnect the signal generator and turn power off. Next, disconnect $M_6$ (by lifting either the wire connecting Pin 11 or that connecting Pin 12) to appreciate its effect upon overall circuit behavior. Finally, reapply power, reconnect the signal generator, and with $E = +5$ V, observe $v_O$ as you gradually increase the amplitude of $v_I$ from ±3 V all the way to the full-scale value of ±5 V. Record the output waveform, and justify quantitatively its distortion during the *positive* half-cycle.

**M17:** Lower the signal generator's amplitude back to ±3V, disconnect it from your circuit, and turn power off. Next, reconnect $M_6$ and disconnect $M_3$ (by lifting either the wire connecting Pin 4 or that connecting Pin 5) to appreciate its effect upon overall circuit behavior. Finally, reapply power, reconnect the signal generator, and with $E = +5$ V, observe $v_O$ as you gradually increase the amplitude of $v_I$ from ±3 V all the way to the full-scale value of ±5 V. Record the output waveform, and justify quantitatively its distortion during the *negative* half-cycle. Once finished, remove the signal generator, and turn power off.

**S18:** Using the values of $k$, $V_{t0}$, and $\gamma$ found in Lab #1, simulate the circuits of Steps M13, M14, and M15. Compare with the actual circuits, account for any differences.