

**LAB #1: MOSFET ARRAY CHARACTERIZATION**

Updated Feb. 14, 2005

**Objective:**

To characterize *n*-channel and *p*-channel enhancement MOSFETs, both statically and dynamically. To perform PSpice simulations, and to compare with experimental observations.

**Components:**

1 × CD4007UB MOSFET Array, 2 × 0.1 μF capacitors, 3 × 22 pF capacitors, 1 × 10 kΩ potentiometer, and resistors: 2 × 10 kΩ, and 1 × 1 MΩ, (all 5%, ¼ W).

**Instrumentation:**

A bench power supply, a digital multi-meter, and a dual-trace oscilloscope with X10 probes.

**PART I – THEORETICAL BACKGROUND**

Figure 1 shows the circuit symbols of the *n*-channel enhancement MOSFET (*n*MOSFET) and the *p*-channel enhancement MOSFET (*p*MOSFET), the devices we are going to characterize in this lab. As we know, the *current directions* and *voltage polarities* of one device are *opposite* to those of the other. In fact, the *n*MOSFET and the *p*MOSFET are said to be *complementary* to each other, and when they are fabricated on the same substrate, the resulting technology is referred to as *complementary MOS* (CMOS for short). MOSFETs possess a fourth terminal called the *body* (*B*), which is internally tied to the *substrate*. Though this terminal is not used on purpose, it must be properly biased to prevent unintentional effects.

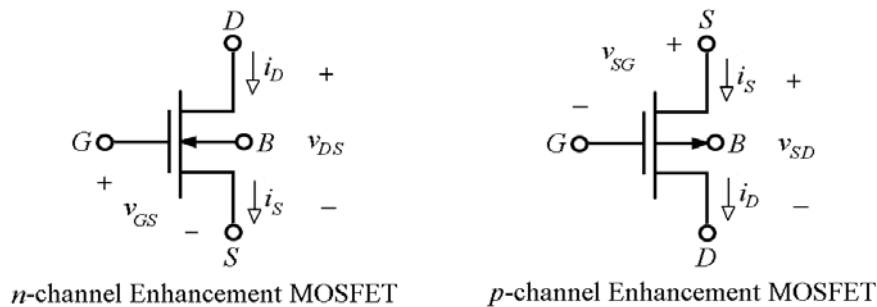
**The *n*MOSFET:**

When an *n*MOSFET is biased in the *pinchoff region*, also called *saturation region* or *active region*, and characterized by the conditions

$$v_{GS} \geq V_{tn} \tag{1a}$$

$$v_{DS} \geq v_{GS} - V_{tn} \tag{1b}$$

its *drain current*  $i_D$  depends on the applied *gate-source* voltage  $v_{GS}$  and the operating *drain-source* voltage  $v_{DS}$  as



**Fig. 1** – Circuit symbols, current directions, and voltage polarities for MOSFETs.

$$i_D = \frac{k_n}{2} (v_{GS} - V_m)^2 (1 + \lambda_n v_{DS}) \quad (2)$$

where

- $k_n$  is a scale factor known as the *device transconductance parameter*, in  $A/V^2$ .
- $V_m$ , known as the *threshold voltage*, is the value of  $v_{GS}$  at which the MOSFET starts conducting.
- $\lambda_n$  is the *channel-length modulation parameter*, in  $V^{-1}$ .

For a low-power  $n$ MOSFET,  $k_n$  is typically in the range of  $10^2 \mu A/V^2$ ,  $V_m$  is in the range of  $10^0 V$ , and  $\lambda_n$  is on the order of  $10^{-2} V^{-1}$ . Note that the extrapolated value of  $i_D$  in the limit  $v_{DS} \rightarrow 0$  is  $i_D = (k_n/2)(v_{GS} - V_m)^2$ .

The *device transconductance parameter*  $k_n$  depends on device geometry as

$$k_n = k'_n \left( \frac{W_n}{L_n} \right) \quad (3)$$

where

- $k'_n$  (also in  $A/V^2$ ) is the *process transconductance parameter*, and  $k'_n = \mu_n C_{ox}$ , where  $\mu_n$  is the *electron mobility* and  $C_{ox}$  is the *gate oxide capacitance per unit area*.
- $W_n$  and  $L_n$  (both in  $\mu m$ ) are the *channel width* and *channel length* of the  $n$ MOSFET

The threshold voltage  $V_m$  depends on the body bias voltage  $V_{SB}$  as

$$V_m = V_{m0} + \gamma_n \left( \sqrt{2|\phi_p| + V_{SB}} - \sqrt{2|\phi_p|} \right) \quad (4)$$

where

- $V_{m0}$  is the threshold voltage in the absence of any body bias ( $V_{SB} = 0$ )
- $\gamma_n$  is the *body-effect coefficient*, typically near  $0.5 V^{1/2}$
- $\phi_p$  is the *equilibrium electrostatic potential* of the  $p$ -type body, typically  $-0.3 V$ .

Recall that in the  $n$ MOSFET the body forms a  $pn$  junction both with the source and the drain regions, with  $B$  acting as the *anode*. To avoid inadvertently turning on either of these junctions, the body of the  $n$ MOSFET must never be biased *more positive* than the source, that is, we must always have  $V_{SB} \geq 0$ , or, equivalently,

$$V_B \leq V_S \quad (5)$$

To satisfy this condition at all times, the body of the  $n$ MOSFET is biased at the *most negative voltage* (MNV) in the circuit.

### The $p$ MOSFET:

Similar considerations hold for the  $p$ MOSFET, provided we *reverse* all *current directions* and *voltage polarities*. Thus, the pinchoff-region conditions of Eq. (1) become, for the  $p$ MOSFET,

$$v_{SG} \geq -V_{tp} \quad (6a)$$

$$v_{SD} \geq v_{SG} + V_{tp} \quad (6b)$$

In this region, Eq. (2) is now rephrased as

$$i_D = \frac{k_p}{2} (v_{SG} + V_{tp})^2 (1 + \lambda_p v_{SD}) \quad (7)$$

where

$$k_p = k'_p \frac{W_p}{L_p} \quad (8)$$

is again the *device transconductance* parameter, in A/V<sup>2</sup>, and  $W_p$  and  $L_p$  (both in  $\mu\text{m}$ ) are the channel *width* and channel *length* of the  $p\text{MOSFET}$ . The quantity  $k'_p = \mu_p C_{ox}$  is again called the *process transconductance parameter*, with  $\mu_p$  being the *hole mobility* and  $C_{ox}$  the *gate oxide capacitance per unit area*. Holes are *less mobile* than electrons, typically  $\mu_p \cong 0.4\mu_n$ . In CMOS technology the value of  $C_{ox}$  is the same for  $n$  and  $p$  channel devices, so we typically have  $k'_p \cong 0.4 k'_n$ .

Equation (4) becomes, for the  $p\text{MOSFET}$ ,

$$V_{tp} = V_{tp0} - \gamma_p (\sqrt{2\phi_n + V_{BS}} - \sqrt{2\phi_n}) \quad (9)$$

where

- $V_{tp0}$  is the threshold voltage in the absence of any body bias ( $V_{BS} = 0$ )
- $\gamma_p$  is the *body-effect coefficient*, typically near  $0.5 \text{ V}^{1/2}$
- $\phi_n$  is the *equilibrium electrostatic potential* of the  $n$ -type body, typically  $+0.3 \text{ V}$ .

Recall that in the  $p\text{MOSFET}$  the body forms an  $np$  junction both with the source and the drain regions, with  $B$  acting as the *cathode*. To avoid inadvertently turning on either of these junctions, the body of the  $n\text{MOSFET}$  must never be biased *more negative* than the source, that is, we must always have  $V_{BS} \geq 0$ , or, equivalently,

$$V_B \geq V_S \quad (10)$$

To satisfy this condition at all times, the body of the  $n\text{MOSFET}$  is biased at the *most positive voltage* (MPV) in the circuit.

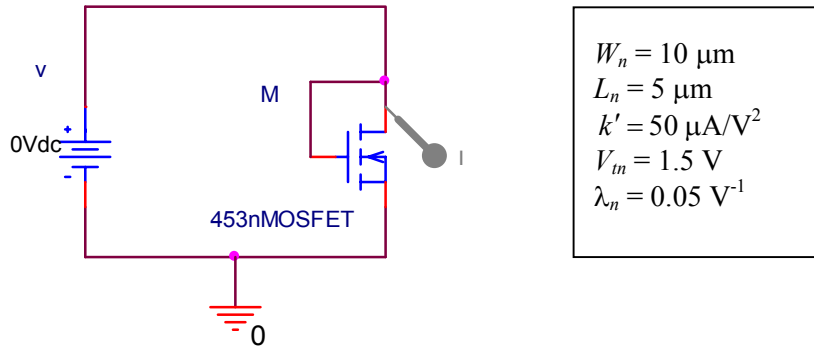
### PSpice Simulations:

MOSFET circuits are readily simulated using PSpice. In the PSpice circuit of Fig. 2 we are using a homebrew  $n\text{MOSFET}$  called 453nFET to display the  $i_D$  versus  $v_{GS}$  characteristic in the so called *diode mode* of operation ( $G$  and  $D$  tied together). This device has been created by renaming and suitably editing the *PSpice Model* of one of the MOSFETs available in the PSpice Library. This has been done first by clicking the device to select it, then by clicking **Edit**  $\rightarrow$  **PSpice Model** to change the values of its parameters. The result is the following model statement:

```
.model 301nMOSFET          NMOS(W=10u L=5u kp=50u Vto=1.5 lambda=0.05)
```

The characteristic, expressed by Eq. (2) and shown in Fig. 3a, is reminiscent of a diode curve – hence, the name.

It is interesting to note that if we plot the  $i$ - $v$  characteristic of a diode-connected MOSFET on a *square-root-versus-linear* system of axes, the resulting curve becomes a *straight line*. Specifically, if we



**Fig. 2** – PSpice circuit to plot the  $i$ - $v$  characteristic of a homebrew  $n$ MOSFET operated in the diode mode ( $G$  and  $D$  tied together, and  $B$  and  $S$  tied together. ).

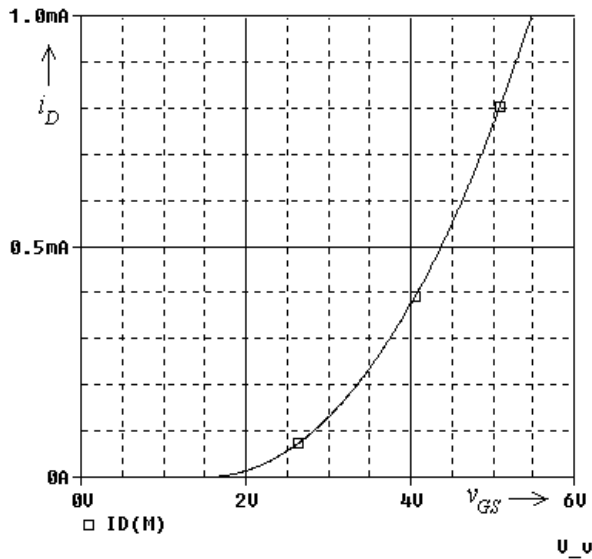
plot Eq. (2) on an  $x$ - $y$  plane with

$$x = v_{GS} = v_{DS} \tag{11a}$$

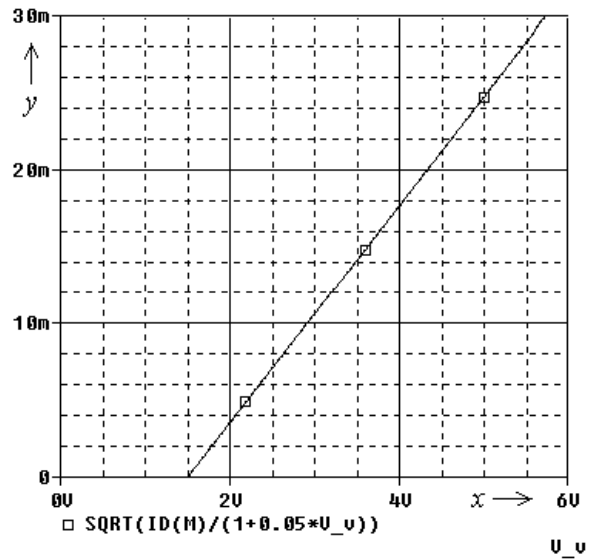
and

$$y = \sqrt{\frac{i_D}{1 + \lambda_n x}} \tag{11b}$$

then the characteristic becomes  $y = \sqrt{k_n/2}(x - V_{tn})$ , that is, a straight line with  $slope = \sqrt{k_n/2}$  and  $x$ -axis *intercept* at  $V_{tn}$ . This is illustrated in Fig. 3b for our homebrew  $n$ MOSFET. We shall find this feature quite convenient from an experimental standpoint.

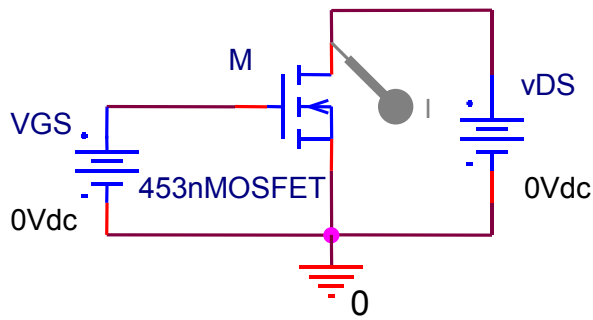


(a)



(b)

**Fig. 3** – The  $i$ - $v$  characteristic of the diode-connected  $n$ MOSFET of Fig. 2.



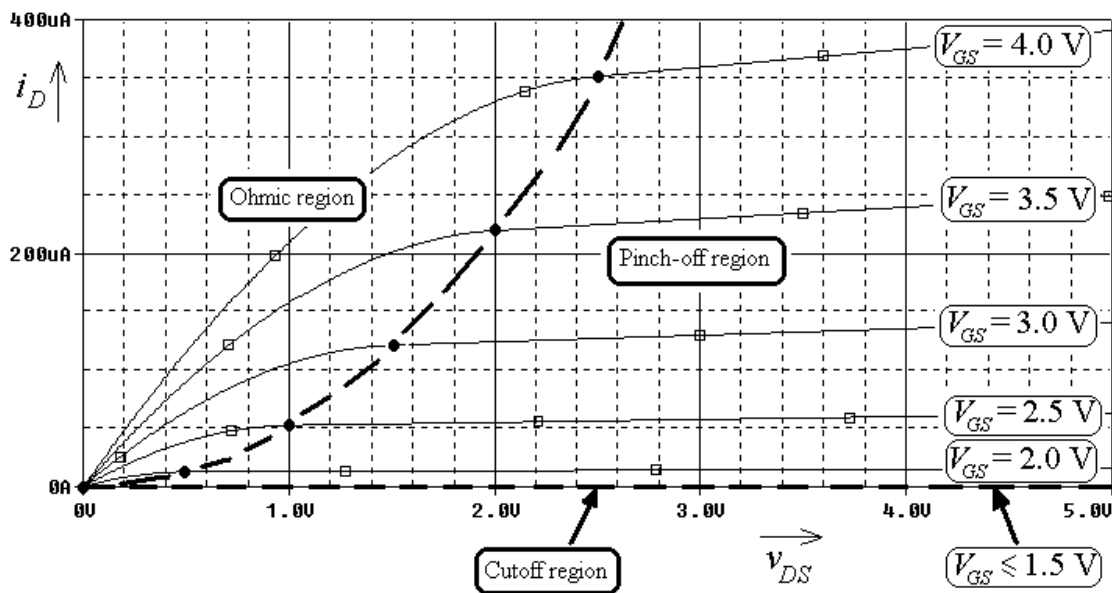
**Fig. 4** - PSpice circuit to plot  $i_D$  versus  $v_{DS}$  for different values of  $V_{GS}$ .

An insightful alternative for illustrating  $n$ MOSFET operation is by plotting  $i_D$  versus  $v_{DS}$  for different values of  $v_{GS}$ . The PSpice circuit of Fig. 4 generates such a plot for incremental steps in  $V_{GS}$  of 0.5 V each. The resulting family of curves, shown in Fig. 5, reveals *three regions* of operation:

- For  $v_{GS} \leq V_m$  ( $= 1.5$  V) we get  $i_D = 0$ , indicating that the  $n$ MOSFET is operating in the **cutoff (CO) region**. In this region both the  $GS$  and  $DS$  ports act as *open circuits*.
- For  $v_{GS} > V_m$ , the  $n$ MOSFET is *on*. The region corresponding to  $v_{DS} > V_{GS} - V_m$  is called the **pinchoff (PO)**, or **saturation**, or **active** region. As we know, in this region Eq. (2) holds, which we repeat here

$$i_D = \frac{k_n}{2} (v_{GS} - V_m)^2 (1 + \lambda_n v_{DS}) \quad \text{for } v_{DS} > V_{GS} - V_m \quad (12)$$

In the PO region, the  $i_D$  versus  $v_{DS}$  curves are almost *horizontal*, indicating *current-source* behavior by the  $DS$  port there. Moreover, if we project the PO curves to the left, they all converge to the *same point* on the  $v_{DS}$  axis. This point is located at  $-1/\lambda_n$  V. Note that when operated in the diode mode,



**Fig. 5** – Illustrating the *three regions* of operation of an  $n$ MOSFET.

the MOSFET has  $v_{DS} = v_{GS}$ , which obviously satisfies  $v_{DS} > V_{GS} - V_m$ , indicating PO operation when the device is on.

- The region corresponding to  $v_{DS} < V_{GS} - V_t$  is called the **ohmic** ( $\Omega$ ), or **triode** region. In this region the channel behaves as a nonlinear resistor, and  $i_D$  takes on the form

$$i_D = k_n \left[ (v_{GS} - V_m) v_{DS} - \frac{v_{DS}^2}{2} \right] (1 + \lambda_n v_{DS}) \quad \text{for } v_{DS} < V_{GS} - V_m \quad (13)$$

For small values of  $v_{DS}$ , we can ignore  $v_{DS}^2/2$  as well as  $\lambda_n v_{DS}$  ( $\lambda_n \ll 1 \text{ V}^{-1}$ ), and approximate

$$i_D \cong \frac{1}{r_{DS}} v_{DS} \quad (14a)$$

where

$$r_D = \frac{1}{k_n (V_{GS} - V_m)} \quad (14b)$$

represents the *channel resistance* in the limit  $v_{DS} \rightarrow 0$ . Such a resistance is controlled by  $V_{GS}$ , indicating *voltage-controlled resistance* behavior near the origin. As shown in Fig. 5, the borderline between the PO and the  $\Omega$  regions is a locus of points forming a *parabola*.

You can simulate the above circuits on your own by downloading their appropriate files from the Web. To this end, go to <http://online.sfsu.edu/~sfranco/CoursesAndLabs/Labs/453Labs.html>, and once there, click on **PSpice Examples**. Then, follow the instructions contained in the **Readme** file.

## PART II – EXPERIMENTAL PART

The purpose of this laboratory is to characterize the CD4007UB MOSFET Array, consisting of three *enhancement nMOSFETs* ( $M_1$ ,  $M_3$ , and  $M_5$ ) and three *enhancement pMOSFETs* ( $M_2$ ,  $M_4$ , and  $M_6$ ) interconnected as in Fig. 6. An important advantage of monolithic fabrication is that devices sharing the same process and geometries tend to exhibit identical characteristics, a feature referred to as *matching*.

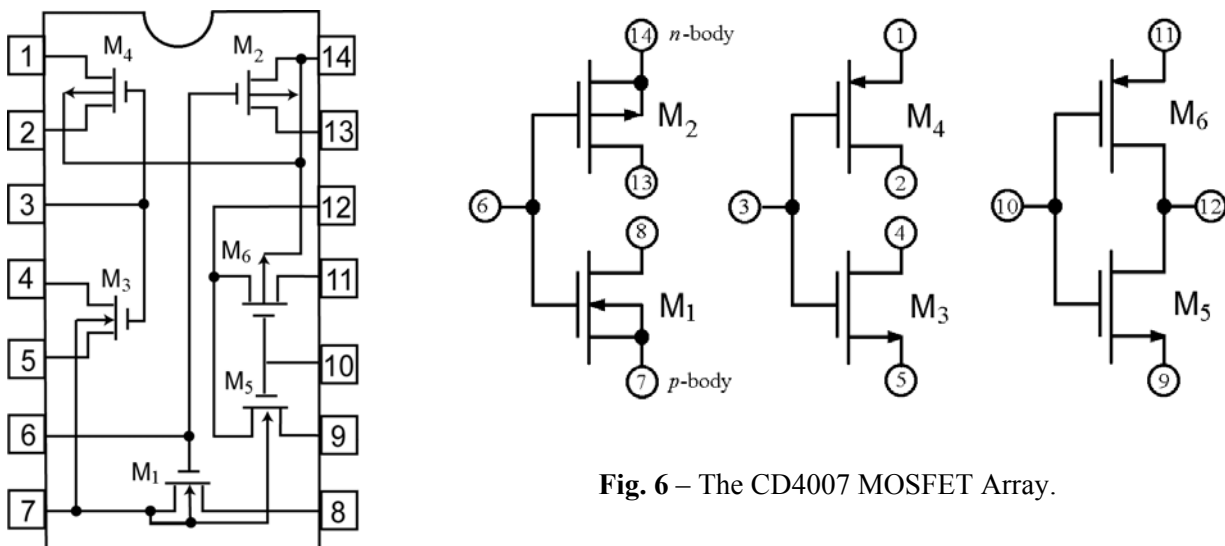


Fig. 6 – The CD4007 MOSFET Array.

In our case we say that  $M_1$ ,  $M_3$ , and  $M_5$  are matched, and, separately, that  $M_2$ ,  $M_4$ , and  $M_6$  are matched.

As mentioned, the body of the three  $n$ MOSFETs (pin 7), which is  $p$ -type, must always be connected to the *most negative voltage* (MNV) in the circuit to avoid inadvertently turning on parasitic junctions. Likewise, the body of the three  $p$ MOSFETs (pin 14), which is  $n$ -type, must always be connected to the *most positive voltage* (MPV) in the circuit. Failure to respect these constraints may invalidate all measurements taken.

The CD4007 is a delicate device. To avoid damaging it, make sure that you always *turn power off* before making any circuit changes, and that before reapplying power, each lab partner checks separately that the circuit has been wired correctly. Also, refer to the Appendix 1 for useful tips on how to wire proto-board circuits. Though the tips are given for an op amp circuit example, similar precautions are generally necessary for any other type of IC.

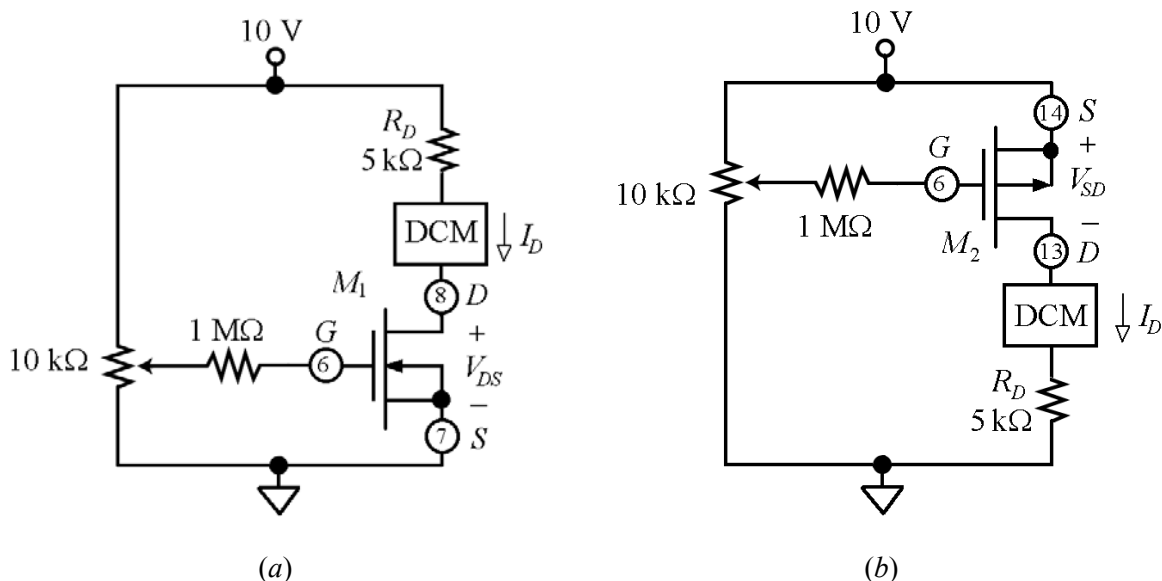
The hand calculations and PSpice simulations that you will perform in this and the following lab rely on the measurements taken for the *particular CD4007 sample*, so if you are careless and end up damaging it, you'll have to perform each measurement all over again! Just in case you wish to check whether the device is still in working condition or not, you may want to pre-wire in a separate area of your proto-board the circuit of Fig. 14, which uses all transistors to implement an oscillator. When in doubt, you may want to transfer your CD4007 sample there and check with the oscilloscope whether it still oscillates. This is not an absolute guarantee, but at least it gives a reasonable indication.

You are encouraged to compare the data you are measuring on your *particular* sample against those reported in the data sheets, which are *typical* in that they were obtained by averaging over a large number of samples. The data sheets can readily be downloaded from the Web (for instance, by visiting <http://www.google.com> and searching for CD4007UB or variants thereof.)

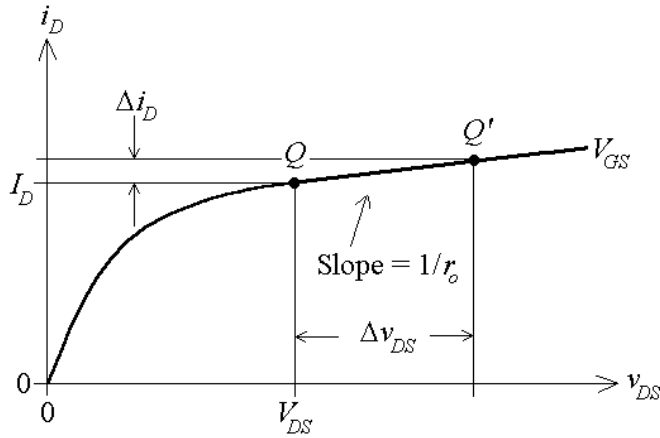
Henceforth, steps shall be identified by letters as follows: **C** for calculations, **M** for measurements, **P** for pre-lab preparations, and **S** for Spice simulations.

**Finding  $\lambda_n$  and  $\lambda_p$ :**

**MC1:** We use the circuits of Fig. 7 to find  $\lambda_n$  and  $\lambda_p$ . Mark one of the CD4007 ICs (the other is a spare).



**Fig. 7** – Test circuits to find  $\lambda_n$  and  $\lambda_p$ , respectively.



**Fig. 8** – Graphical illustration for finding  $\lambda_n$  and  $\lambda_p$ .

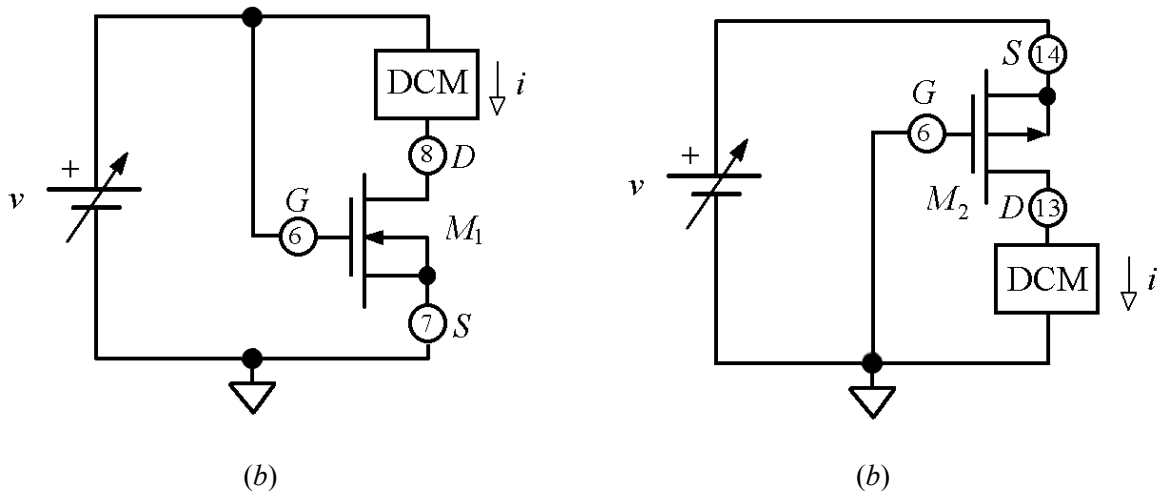
Turning first to the  $n$ MOSFET, assemble the circuit of Fig. 7a with power off (for  $R_D$  use  $2 \times 10 \text{ k}\Omega$  resistors in parallel). Using your multi-meter as a *digital current meter* (DCM), insert it in series between  $R_D$  and the drain  $D$ , as shown. Apply power and adjust the potentiometer for  $I_D = 1 \text{ mA}$ . With reference to Fig. 8, this will bias  $M_1$  at the operating point  $Q(I_D, V_{DS}) = Q(1 \text{ mA}, 5 \text{ V})$ . Now short out  $R_D$  with a wire to change the operating point from  $Q$  to  $Q'$  with  $\Delta V_{DS} = 5 \text{ V}$ , and measure the corresponding change  $\Delta I_D$ . Expect the latter to be small, so use as many digits as your ammeter will allow. Finally, find  $r_o = \Delta V_{DS} / \Delta I_D$  and  $\lambda_n = 1 / (r_o I_D - V_{DS})$ . Are your values typical?

**Note:** All your data will be afflicted by measurement uncertainties, so they must be expressed in the form  $X \pm \Delta X$  (e.g.  $\lambda_n = 0.045 \pm 0.002 \text{ V}^{-1}$ ).

**MC2:** Repeat Step MC1 for the  $p$ MOSFET of Fig. 7b, except that you now find your parameters as  $r_o = \Delta V_{SD} / \Delta I_D$ , and  $\lambda_p = 1 / (r_o I_D - V_{SD})$ . Again, are your values typical? How do their magnitudes compare with those of the  $n$ MOSFET of Step MC1?

**Finding  $k_n$ ,  $V_{m0}$ ,  $k_p$ , and  $V_{ip0}$ :**

**M3:** We use the circuits of Fig. 9 to find  $k_n$ ,  $V_{m0}$ ,  $k_p$ , and  $V_{ip0}$ . Turning first to the  $n$ MOSFET, assemble



**Fig. 9** – Test circuits to find  $k_n$ ,  $V_{m0}$ ,  $k_p$ , and  $V_{ip0}$ .

the circuit of Fig. 9a with the DCM in series with the drain  $D$ . Obtain  $v$  from one of your variable power and measure and record  $i$  for  $v = 0$  V, 1 V, 2 V, 3 V, 4 V, and 5V.

**C4:** Plot the data of Step M3 on  $x$ - $y$  paper, with  $x = v$  and with  $y = \sqrt{i/(1 + \lambda_n x)}$ , using the value of  $\lambda_n$  found in Step MC1. Hence, find the *best fit straight line*, determine its slope  $s$ , and obtain  $k_n = 2s^2$ . Moreover, obtain  $V_{m0}$  as the value of  $x$  where your line intercepts the  $x$ -axis. Is your value typical?

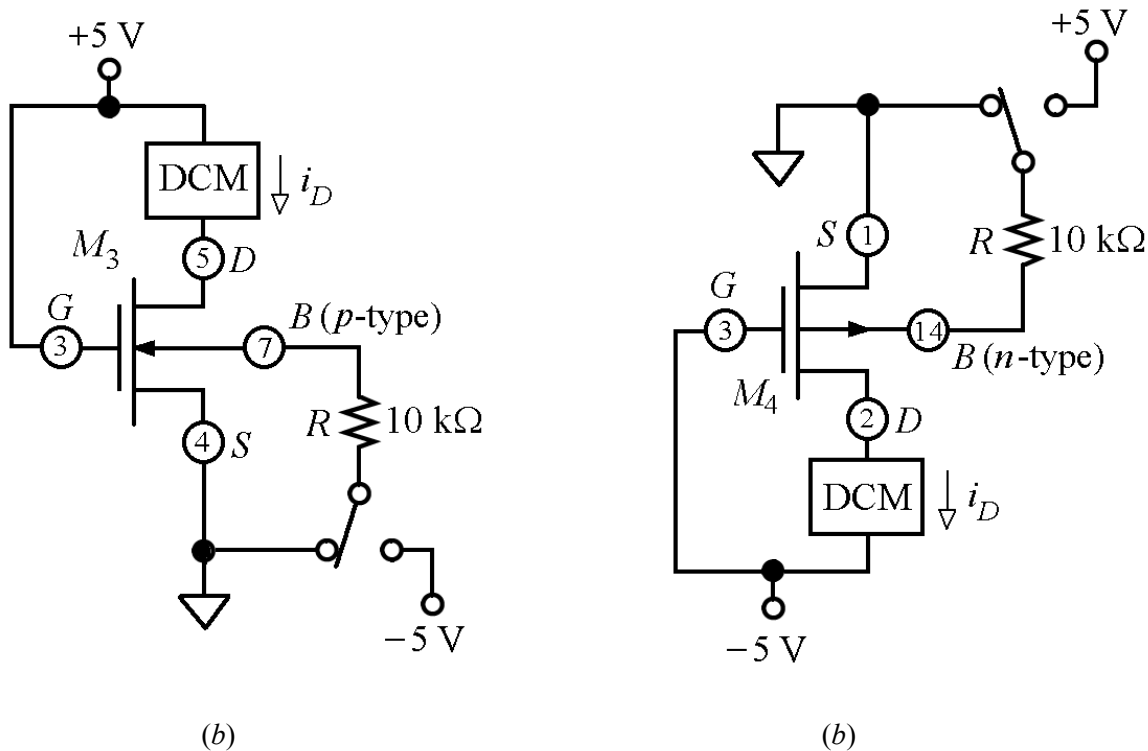
**M5:** Repeat Step M3 for the  $p$ MOSFET of Fig. 9b.

**C6:** Plot the data of Step M5 on  $x$ - $y$  paper, with  $x = v$  and with  $y = \sqrt{i/(1 + \lambda_p x)}$ , using the value of  $\lambda_p$  found in Step MC2. Hence, find the *best fit straight line*, determine its slope  $s$ , and obtain  $k_p = 2s^2$ . Moreover, obtain  $V_{p0}$  as the *negative* of the value of  $x$  where your line intercepts the  $x$ -axis. Is your value typical? How does it compare with that of the  $n$ MOSFET?

**Finding  $\gamma_n$  and  $\gamma_p$ :**

We use the circuits of Fig. 10 to find  $\gamma_n$  and  $\gamma_p$ . Turning first to the  $n$ MOSFET, we observe that the function of  $R$  is to switch the substrate voltage  $V_B$  from 0 V to  $-5$  V, and thus change the threshold voltage from  $V_{m0}$  to  $V_{m}(V_{SB} = 5$  V). We then exploit this change to indirectly find  $\gamma_n$  via Eq. (4). The reason for using  $R$  instead of a plain wire is to limit the substrate current in case of wiring errors, and thus protect the IC against possible destruction.

**MC7:** With power off, assemble the circuit of Fig. 10a, making sure that there is no other connecting



**Fig. 10** – Test circuits to find  $\gamma_n$  and  $\gamma_p$ .

wire left from the previous test circuits, particularly at pin 14. Next, apply power, and record first the DCM reading  $I_0$  with  $R$  switched to ground ( $V_{SB} = 0$  V), then the DCM reading  $I_1$  with  $R$  switched to  $-5$  V ( $V_{SB} = 5$  V). Finally, calculate the threshold voltage change

$$V_{tn} - V_{tn0} = (5 - V_{tn0}) \times (1 - \sqrt{I_1 / I_0}) \quad (15a)$$

and, hence, the body-effect coefficient

$$\gamma_n = \frac{V_{tn} - V_{tn0}}{\sqrt{2|\phi_p| + 5} - \sqrt{2|\phi_p|}} \quad (15b)$$

where you are to assume  $\phi_p = -0.3$  V. Is your finding typical?

**MC8:** Turn power off, remove all wires (particularly the one at pin 7), and assemble the circuit of Fig. 10b. Next, apply power, and record first the DCM reading  $I_0$  with  $R$  switched to ground ( $V_{BS} = 0$  V), then the DCM reading  $I_1$  with  $R$  switched to  $+5$  V ( $V_{BS} = 5$  V). Finally, calculate the threshold voltage change

$$|V_{tp}| - |V_{tp0}| = (5 - |V_{tp0}|) \times (1 - \sqrt{I_1 / I_0}) \quad (16a)$$

and, hence, the body-effect coefficient

$$\gamma_p = \frac{|V_{tp}| - |V_{tp0}|}{\sqrt{2\phi_n + 5} - \sqrt{2\phi_n}} \quad (16b)$$

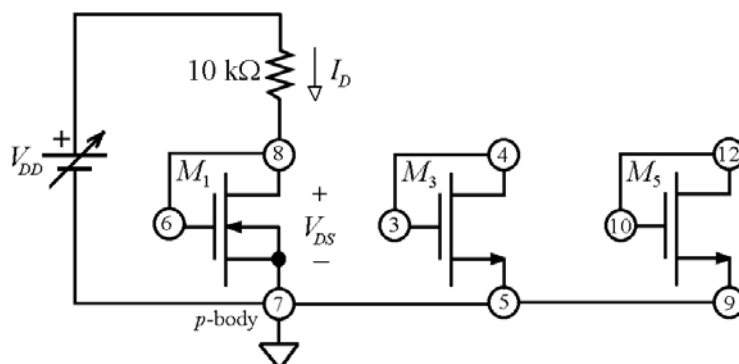
where you are to assume  $\phi_n = 0.3$  V. Is your finding typical?

Summarize your findings by tabulating  $k_n$ ,  $V_{tn0}$ ,  $\lambda_n$ ,  $\gamma_n$ , and  $k_p$ ,  $V_{tp0}$ ,  $\lambda_p$ ,  $\gamma_p$ . Express all data in the form  $X \pm \Delta X$ , as usual

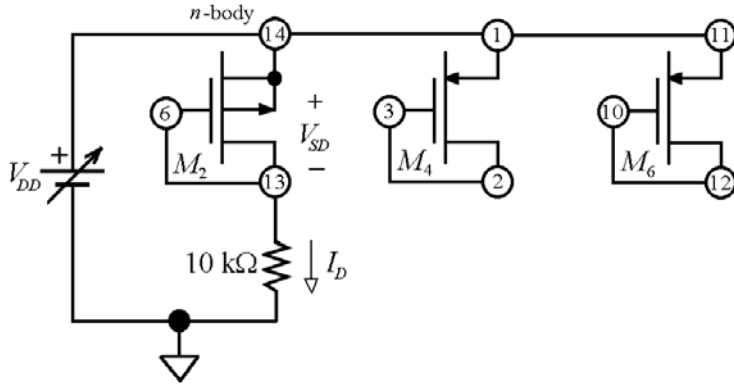
**S9:** Use PSpice to display the  $i_D$ - $v_{DS}$  characteristics of your  $n$ MOSFET, as well as the  $i_D$ - $v_{SD}$  characteristics of your  $p$ MOSFET. Do it both for the case of 0-V and 5-V body bias, compare, and comment.

### Transistor Mismatch:

Because of unavoidable fabrication process variations, there is generally a certain degree of mismatch among the three  $n$ MOSFETs, as well as mismatch among the three  $p$ MOSFETs. A thorough assessment



**Fig. 11** – Circuit to measure the offset voltages of the  $n$ MOSFETs.



**Fig. 12** – Circuit to measure the offset voltages of the pMOSFETs.

of the mismatches would require repeating all measurements also for the remaining transistors, a lengthy task. Here we shall limit ourselves to investigating mismatches only for the case of *diode-mode* operation, which is important in differential amplification such as with memory sense amplifiers. Specifically, we shall force the same current  $I_D$  through each transistor, and measure the resulting voltage  $v$ . Any mismatches in the values of  $k$ ,  $V_t$ , and  $\lambda$  will cumulatively result in mismatched values of  $V_{DS}$ . The difference between the voltages of a particular transistor pair is called the *offset voltage*.

**MC10:** For transistor  $M_1$  of Fig. 11, adjust  $V_{DD}$  for  $I_D = 1$  mA, and measure the corresponding value of  $V_{DS}$  (use as many digits as your DC voltmeter will allow). Repeat for transistor  $M_3$ , and then for transistor  $M_5$ . What is the offset voltage between  $M_3$  and  $M_1$ ? Between  $M_5$  and  $M_1$ ?

**MC11:** For transistor  $M_2$  of Fig. 12, adjust  $V_{DD}$  for  $I_D = 1$  mA, and measure the corresponding value of  $V_{SD}$  (use as many digits as your DC voltmeter will allow). Repeat for transistor  $M_4$ , and then for transistor  $M_6$ . What is the offset voltage between  $M_4$  and  $M_2$ ? Between  $M_6$  and  $M_2$ ? How do the offsets of the pMOSFETs compare with those of the nMOSFET?

### Dynamic Characterization:

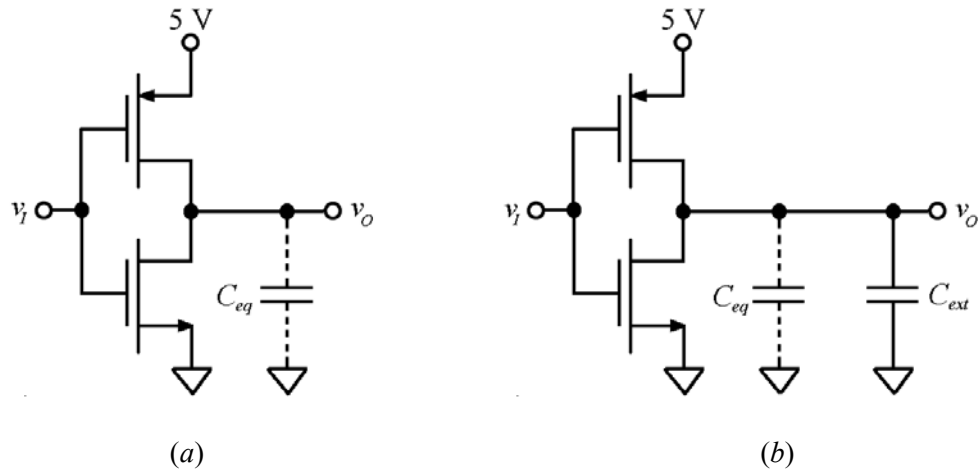
A MOSFET contains a variety of stray capacitances (gate-to-body, gate-to-source, gate-to-drain, drain-to-body, and source-to-body), whose effect is to limit the dynamics of the device. In digital applications, the main effect of limited transistor dynamics as well other parasitics associated with wiring, are the *propagation delays* of logic gates. We shall investigate this aspect using the basic CMOS inverter, which is the workhorse of digital systems.

Mercifully, the cumulative effect of all stray capacitances can be modeled with a single, *total equivalent capacitance*  $C_{eq}$  at the output node of the inverter, as depicted in Fig. 13a. The average propagation delay  $t_p$  of the inverter is then due to the limited current ability of its transistors to charge/discharge  $C_{eq}$  during output switching. Our next goal is to estimate the value of  $C_{eq}$ . It stands to reason to assume that  $t_p$  be proportional to  $C_{eq}$ , or

$$t_p = KC_{eq} \quad (17)$$

where  $K$  is a suitable proportionality constant, in ns/pF. It is apparent that the higher the current drive capabilities of the transistors, the smaller the value of  $K$ . While  $t_p$  can be measured,  $K$  and  $C_{eq}$  are unknown. We thus need another equation, and this is provided by *deliberately* loading the inverter with an external capacitance  $C_{ext}$  of known value, as illustrated in Fig. 13b. The total output capacitance is now  $C_{eq} + C_{ext}$ , and this increases the propagation delay to the new value

$$t_{p(\text{new})} = K(C_{eq} + C_{ext}) \quad (18)$$



**Fig. 13** – Lumped capacitance models for the investigation of the inverter’s dynamics.

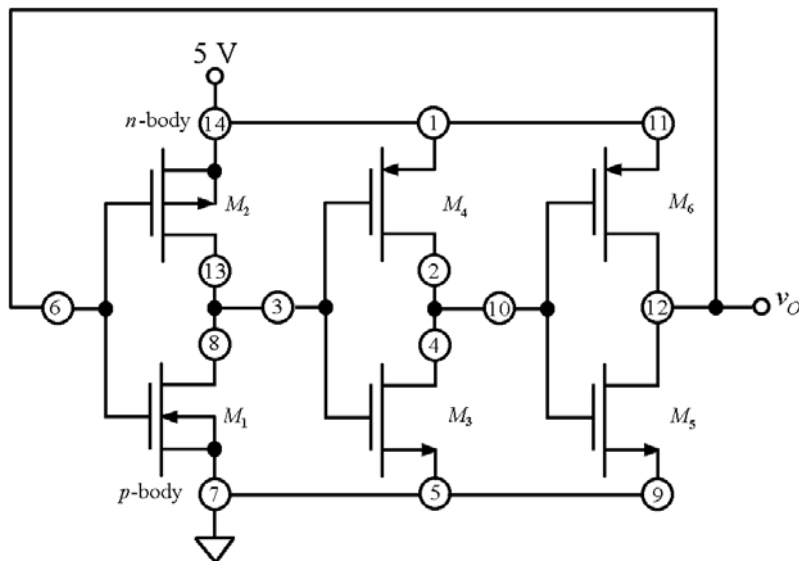
which also can be measured. Eliminating  $K$ , we readily find

$$C_{eq} = C_{ext} \frac{t_p}{t_{p(\text{new})} - t_p} \quad (19)$$

Once we know  $C_{eq}$ , we find  $K = t_p / C_{eq}$ .

An ingenious technique for measuring the average propagation delay  $t_p$  is to connect an *odd* number  $n$  of inverters in ring fashion, as illustrated in Fig. 14 for the case  $n = 3$ . The resulting circuit, known as a *ring oscillator*, will then automatically oscillate with a period that is easily found to be  $T = 2nt_p$ . After measuring  $T$  with the oscilloscope, we find  $t_p = T/2n$ .

**M12:** With power off, assemble the ring oscillator of Fig. 14. Apply power, and measure its period of oscillation  $T$ .



**Fig. 14** – Ring oscillator.

**Warning:** It is important to realize that connecting the probe to the output of any one of the inverters will add to the existing equivalent capacitance  $C_{eq}$  of that node also the capacitance  $C_p$  of the probe itself, thus increasing the actual period by an unknown error  $\Delta T$ . Such an error may or may not be significant, depending on the case.

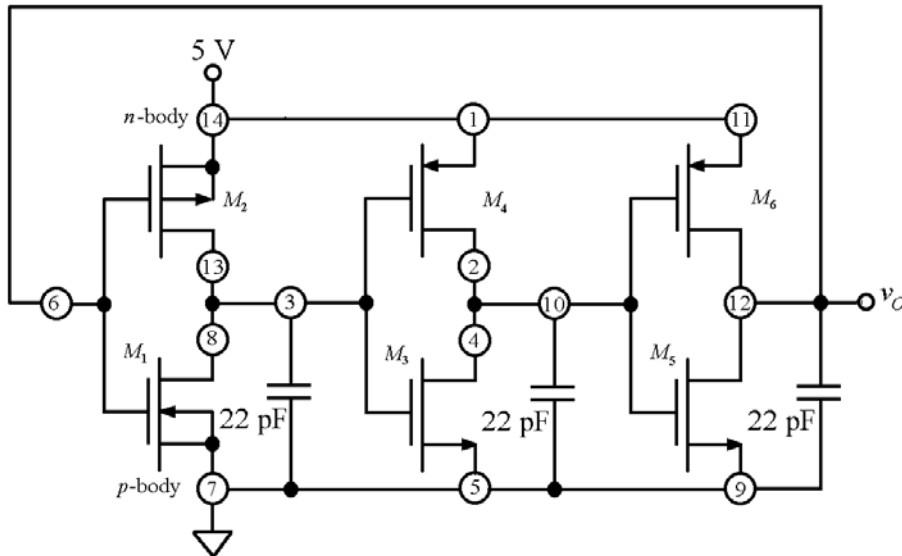
A simple way to find out is to connect also a second *identical* probe in *parallel* with the first, and observe the additional increase in the period, if any. If the circuit is linear, such an increase will be  $\Delta T$  itself! Consequently, once we measure  $\Delta T$ , we subtract it from our period reading to obtain a better estimate for the actual period value. For instance, if with *one* probe you measure a period of 55 ns, and with *two* probes you measure a period of 60 ns, then  $\Delta T = 60 - 55 = 5$  ns, so the actual period is  $T = 55 - \Delta T = 55 - 5 = 50$  ns.

It goes without saying that for this measurement it is critical to use low input capacitance probes, such as X10 probes as discussed in Appendix 2. Also, make sure that your probe is properly *compensated*, and keep all leads short to reduce the effect of stray capacitances!

**MC13:** With power off insert three 22-pF capacitors as shown in Fig. 15. Reapply power, and measure the new period  $T_{(new)}$ . Calculate the average propagation delay both *with* and *without* the 22-pF capacitors. Finally, estimate the values of  $C_{eq}$  and  $K$  using Eqs. (19) and (17). As usual, express all data in the form  $X \pm \Delta X$ .

**MC14:** Repeat Steps M12 and MC13, but with the supply voltage changed from 5 V to 10 V. Justify any changes in the values of  $C_{eq}$  and  $K$ .

**S15:** Using the various transistor parameters measured so far, perform a PSpice simulation of the ring counter of Fig. 14, and display the voltage waveform at the output of each inverter. Beware that since PSpice assumes default values of zero for all capacitances, you must *deliberately* include a capacitance  $C_{eq}$  at the output of each inverter. Finally, compare with the observations and measurements in the lab, and account for any possible differences.



**Fig. 15** – Ring oscillator with deliberate capacitive loading.