

LAB #4: TESTING A HOMEBREW OP AMP/VOLTAGE COMPARATOR

(Updated Dec. 23, 2002)

Objective:

To put the analog building blocks of Experiment # 3 to practical use by bread-boarding a homebrew op amp as well as a homebrew voltage comparator. To investigate some of the most relevant characteristics of the two circuits via calculation, measurement, and PSpice simulation.

Components:

1 × LM3046 IC BJT array, 1 × 2N2222 *npn* BJT, 5 × 2N3906 *pn*p BJTs, 2 × 1N4148 low-power diodes, 1 × 100-pF capacitor, 2 × 0.1-μF capacitors, 1 × 10-kΩ potentiometer, and resistors: 2 × 22 Ω, 2 × 100 Ω, 1 × 560 Ω, 2 × 1.0 kΩ, 3 × 3.3 kΩ, 2 × 10 kΩ, 2 × 20 kΩ, (all 5%, ¼ W).

Instrumentation:

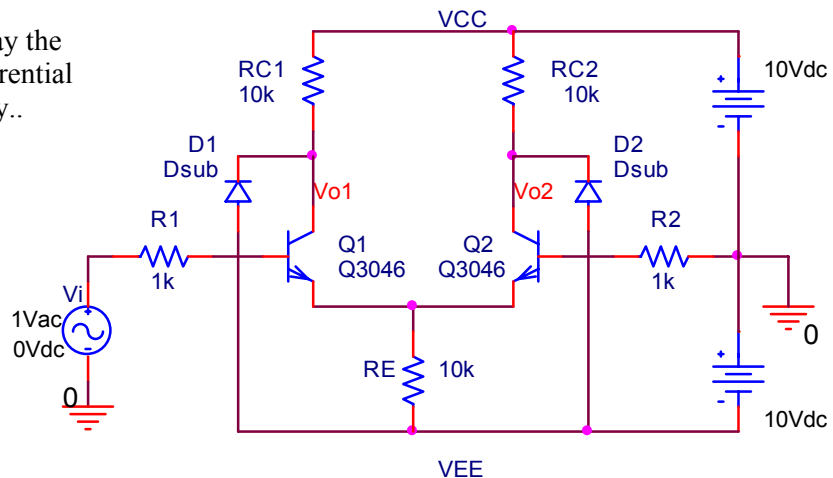
A dual adjustable regulated power supply, a digital multi-meter (DMM), a signal generator (sine wave, square wave), and a dual-trace oscilloscope.

PART I – THEORETICAL BACKGROUND

In this laboratory we are going to investigate two popular *high-gain amplifiers*: the *operational amplifier* and the *voltage comparator*. Before discussing similarities and differences between the two devices, we need to point out that their dynamic characteristics are limited by the internal capacitances of the transistors making them up. In the case of op amps we are especially interested in the frequency response, and in the case of voltage comparators in the transient response. To get an idea, we use PSpice to display both response types for the case of the *differential transistor pair*, the basic ingredient of both op amps and comparators.

Figure 1 shows a PSpice circuit to display the *frequency response* of the differential pair Q_1 and Q_2 of the LM3046 BJT Array that we are going to be using in this lab (note the inclusion of diodes D_1 and D_2 to model the isolation junction between the collector of each BJT and the *p*-type substrate, which is biased at the MNV.) As depicted in Fig. 2, the response is dominated by a *pole* near 1.6 MHz. At this

Fig. 1 – PSpice circuit to display the *frequency response* of the differential pair from the LM3046 IC Array..



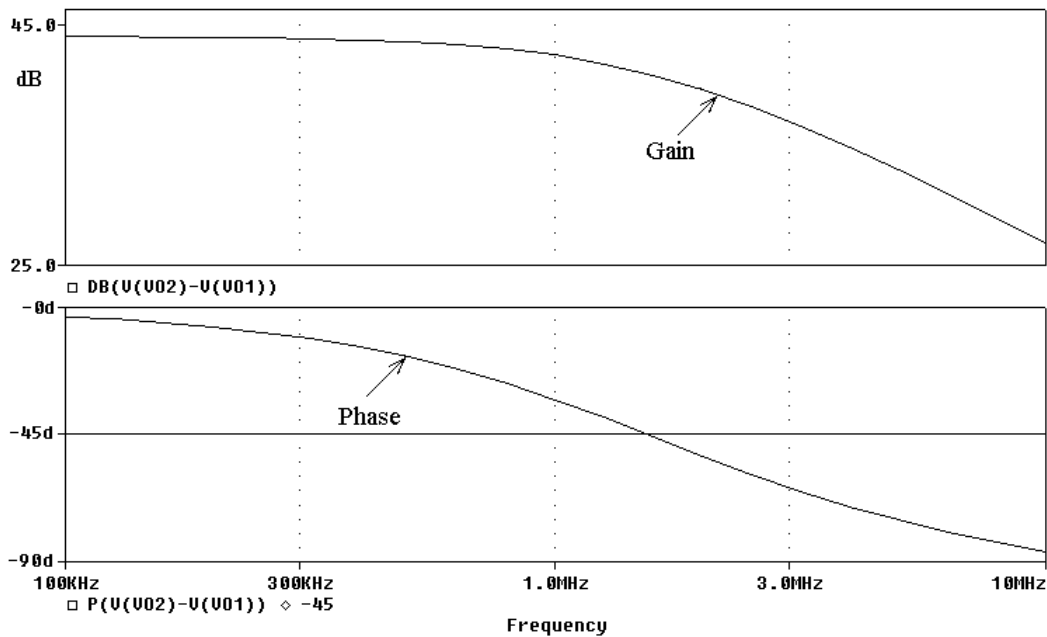


Fig. 2 - Frequency response of the circuit of Fig. 1.

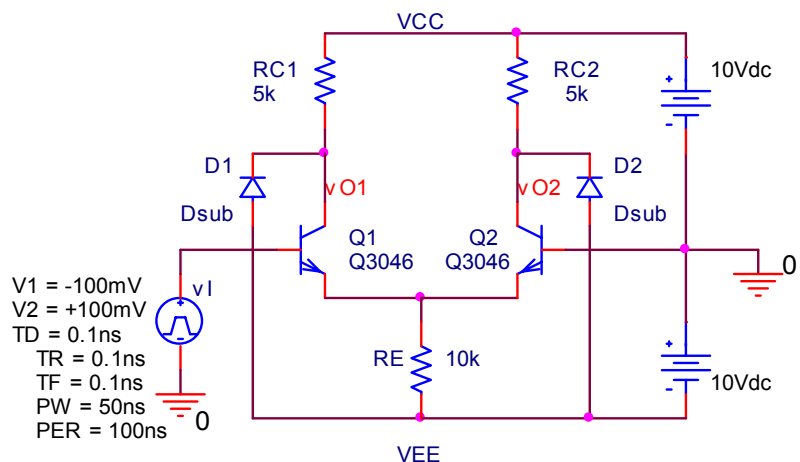
frequency, gain is 3-dB below its DC value, and the phase shift is -45° . The response starts to pick up phase shift about a *decade below* the pole frequency. This shift is -45° at the pole, and reaches -90° about a *decade above* the pole frequency.

Figure 3 shows a PSpice circuit to display the *transient response* of the same differential pair Q_1 and Q_2 . The response, depicted in Fig. 4, consists of exponential transients, as expected of a system dominated by one pole.

The Operational Amplifier:

An operational amplifier (op amp) is a *high-gain amplifier* designed to operate with *negative feedback*. Monolithic bipolar op amps typically consist of *four blocks*:

Fig. 1 – PSpice circuit to display the *transient response* of the differential pair from the LM3046 IC Array.



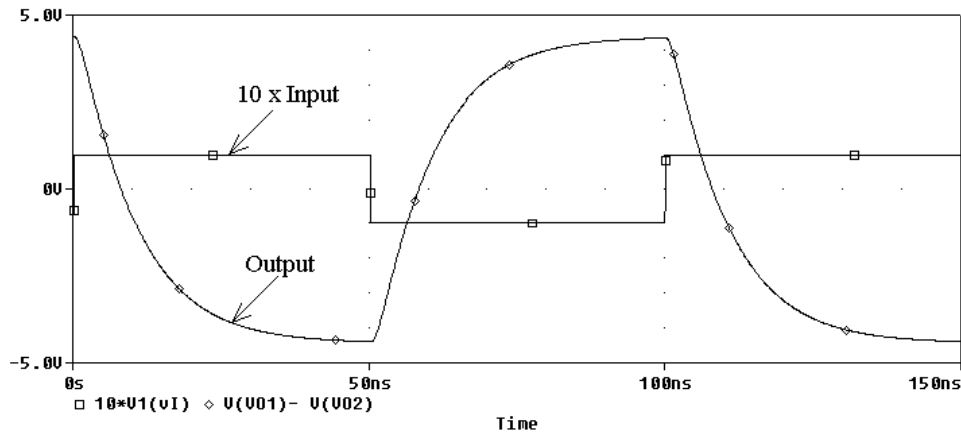


Fig. 4 – Transient response of the circuit of Fig. 3.

- The *input stage*, whose task is to provide high-gain differential amplification, high input impedance, and low input-bias current. This stage is usually implemented with a differential transistor pair, along with a current-mirror load to ensure high gain as well as dual-ended to single-ended conversion.
- The *intermediate stage*, whose task is to provide additional gain, and often also frequency compensation. In bipolar op amps, this stage is often implemented with a Darlington pair, which also serves the purpose of providing level shifting for the single-ended signal.
- The *output stage*, whose task is to provide power gain, along with low output impedance. This is usually implemented with a push-pull transistor pair.
- The *biasing network*, whose task is to suitably bias the aforementioned stages, and also ensure proper circuit startup at power turn-on. This network is based on a system of current mirrors.

As it is operated with *negative feedback*, an op amp is made part of a *loop* consisting of the *op-amp* itself in the *forward* direction, and a *feedback network* in the *backward* direction. As depicted in Fig. 5 for the case of the familiar noninverting amplifier, the task of the feedback network, consisting of R_1 and R_2 , is to feed the *portion* βV_o of the op amp's output back to the *inverting input* – hence the designation *negative feedback*. Were we to feed βV_o to the op amp's noninverting input; then we would have *positive feedback*. Once injected into a positive-feedback loop, a signal feeds upon itself, causing the amplifier's output to grow until it saturates. Perhaps the most common example of positive-feedback circuit is the flip-flop, which has only two possible states.

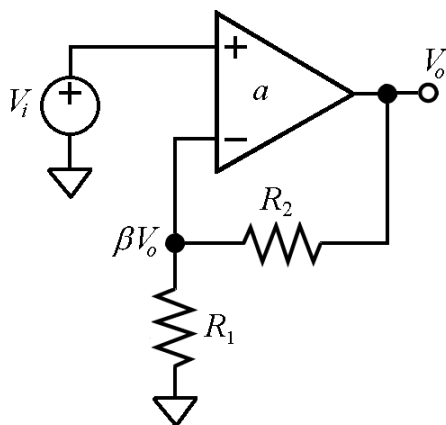


Fig. 5- The noninverting amplifier as a popular example of a negative feedback system. The resistive network *feeds back* to the *inverting input* the portion βV_o of the output. The quantity $\beta = R_1 / (R_1 + R_2)$ is called the *feedback factor*.

Far richer in terms of application potential is negative feedback. However, with this type of feedback the possibility arises for unwanted oscillations. Indeed, if the combined *phase shift* introduced by the amplifier and its feedback network ever reaches -180° , negative feedback will turn into positive feedback, and the circuit may end up oscillating! To be more specific, we note that a signal propagating around the loop experiences an overall amplification of $-\alpha\beta$, where the negative sign stems from the signal inversion occurring at the op amp's inverting input. For an op-amp circuit to break out into oscillation, two conditions must be met:

- the *overall phase shift* around the loop must reach -360° in order to turn negative feedback into positive feedback
- the *overall gain* around the loop at the frequency of -360° phase-shift must be *at least* 1 V/V (0 dB) to make feedback regenerative

The negative sign in the term $-\alpha\beta$ already provides -180° of phase shift, so the remainder of the overall phase shift is that contributed by the product $\alpha\beta$. The simplest circuit to analyze is the *voltage-follower*, for which $\beta = 1$. Then, the overall phase shift around the loop is $-180^\circ - \text{ph}(a)$, where $\text{ph}(a)$ represents the *phase angle* of the open-loop gain a .

To stave off unwanted oscillations, op amps are *frequency compensated*. Among the various compensation methods possible, the one that has gained prominence in IC op amps is *dominant-pole compensation*, so called because it is based on the idea of deliberately making a *single pole* dominate the open-loop response a of the amplifier over the frequency range of interest. This causes a to introduce a maximum phase shift of about -90° . Counting the aforementioned phase shift of -180° occurring at the inverting input, we thus have an overall phase shift of $-180^\circ - 90^\circ = -270^\circ$. This leaves a *phase margin* of $-270^\circ - (-360^\circ) = 90^\circ$.

Figure 6 illustrates the open-loop response before compensation and after dominant-pole compensation. In the example shown, the uncompensated response exhibits three poles. With each pole contributing a phase shift of -90° , the overall phase shift reaches -270° , indicating the existence of a frequency f_{-180° , somewhere between the second and third pole, where the phase shift is -180° . Once we include also the -180° shift at the op amp's inverting input, the overall shift reaches (and surpasses) -360° , a recipe for oscillation. However, with dominant-pole compensation, the phase shift over the frequency range of interest is only -90° as opposed to -270° . As mentioned, this leaves a phase margin of 90° .

It is evident that the price paid for the sake of staving off oscillations is a much premature roll-off of gain with frequency (-20 dB/dec). With this in mind, we can approximate the open-loop gain $a(jf)$ of a dominant-pole-compensated op amp as

$$a(jf) \cong \frac{a_0}{1 + jf / f_b} \quad (1)$$

where a_0 is the open-loop *DC gain*, f_b is the open-loop *bandwidth*, f is the input frequency, and $j^2 = -1$. One can readily see that the frequency at which the gain drops to unity, aptly called the *transition frequency*, is $f_i \cong a_0 f_b$. As an example, the popular 741 op-amp has $a_0 = 200,000$ V/V, $f_b = 5$ Hz, and $f_i = 1$ MHz. It is readily seen that this response has a pole at $s = -2\pi f_b$.

In IC op amps, dominant pole compensation is achieved by *deliberately* adding capacitance to the existing internal stray capacitance that is responsible for one of the poles of the uncompensated response – usually the first pole. As depicted in the figure, this pole must be moved to a low enough frequency to ensure that gain has already dropped to unity (0 dB) before the additional phase shift due to the op amp's higher-order poles comes into play. As a rule, a low-frequency pole requires a large capacitance. To

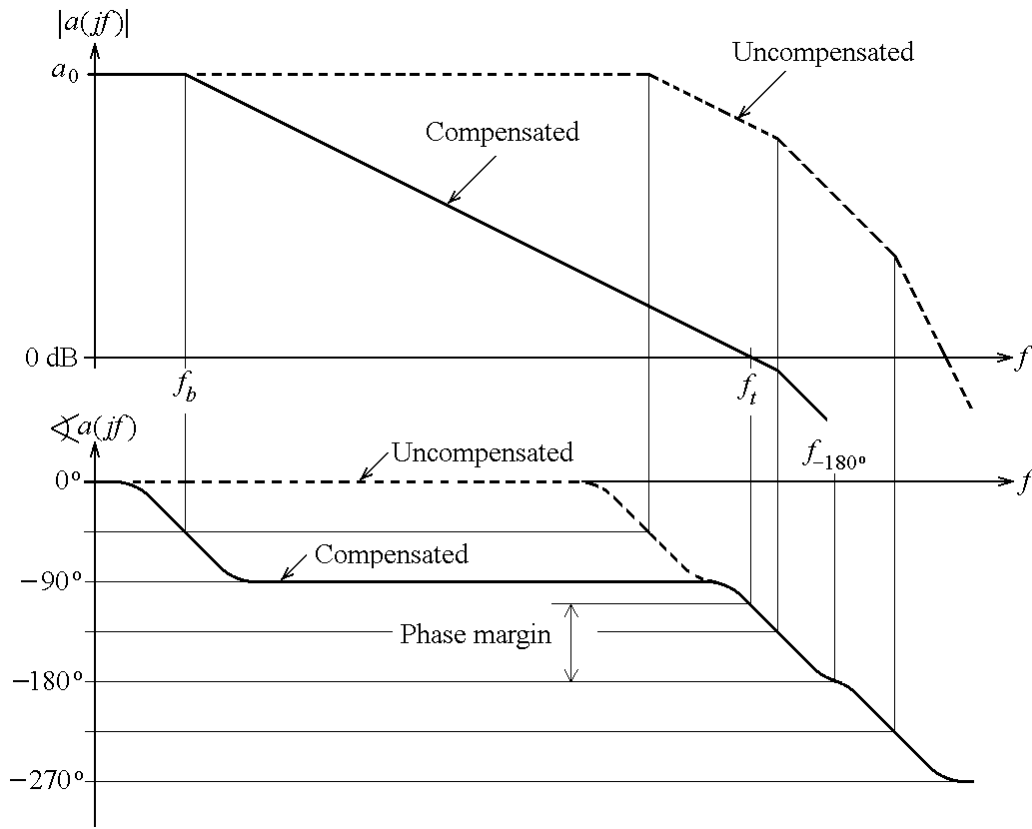


Fig. 6 – Bode plots (*magnitude* at top, *phase* at bottom) of an op amp’s open loop response, before and after dominant-pole compensation.

avoid the on-chip fabrication of an unrealistically large capacitor, IC manufacturers start out with a small and thus acceptable capacitor, and then place it in the feedback path of an internal *high-gain inverting stage* to dramatically increase its equivalent value via the *Miller effect*. For this reason, dominant-pole compensation is also referred to as *Miller compensation*. A good candidate for this capacitance-multiplying task is the Darlington pair forming the aforementioned second stage. As a rule, adding capacitance to lower the first pole affects also the remaining higher-order poles, but for simplicity this has not been shown in the plots of Fig. 6.

The Voltage Comparator:

High-gain amplifiers find also application either *without feedback* (open-loop mode), or with *positive feedback* (Schmitt-triggers). In these cases the amplifier is more aptly called a *voltage comparator* because all it takes is a slight difference between its inputs v_P and v_N to cause the output v_O to saturate. More specifically, the circuit yields

$$v_O = V_{OH} \quad \text{for } v_P > v_N \quad (2a)$$

$$v_O = V_{OL} \quad \text{for } v_P < v_N \quad (2b)$$

where V_{OH} and V_{OL} are the *high* and the *low* saturation limits of the device, usually logic levels such as

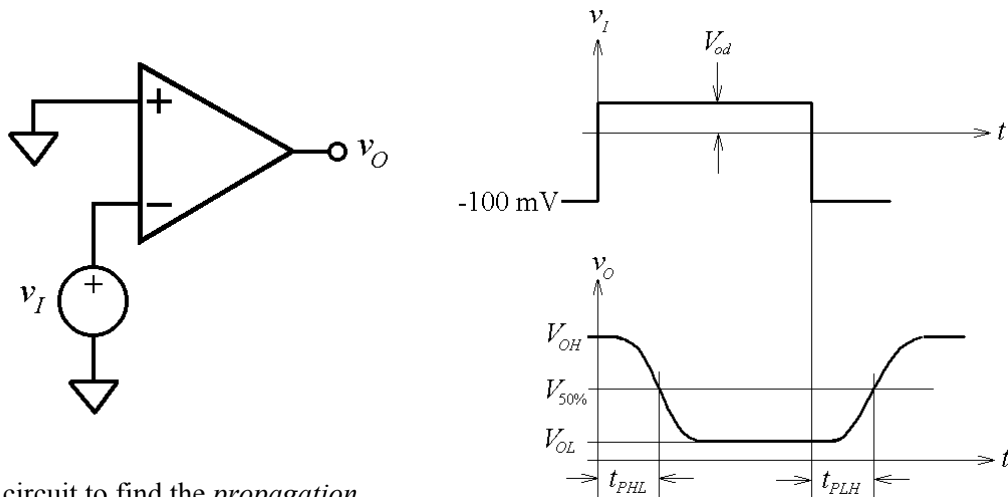


Fig. 7 - Test circuit to find the *propagation delays* of a voltage comparator.

$V_{OH} \cong 5 \text{ V}$ and $V_{OL} \cong 0 \text{ V}$.

A fundamental difference between an op amp and a comparator is that while negative feedback is designed to force the op amp to operate *within the linear region* of its VTC, the absence of negative feedback is designed to force the comparator to operate primarily in the two saturation regions of its VTC, that is, either at $v_O = V_{OL}$ or at $v_O = V_{OH}$. The compensation capacitor C_c that is mandatory in negative-feedback operation to stave off oscillations is actually detrimental in open-loop or in positive-feedback operation, as it slows down the response of the comparator unnecessarily. Consequently, comparators do not include any compensation capacitor. Moreover, the need for logic-level compatibility at the output usually results in different output-stage designs for voltage comparators as compared to op amps.

For comparators, an often critical feature is the speed of response. Speed is specified in terms of the *propagation delays* t_{PHL} and t_{PLH} . As illustrated in Fig. 7, the comparator is subjected to an input pulse characterized by a specific *overdrive* V_{od} , such as $V_{od} = 20 \text{ mV}$. Then, the amount of time, following the *leading edge* of v_I , that it takes for v_O to swing from V_{OH} down to the transition's *midpoint*, defined as

$$V_{50\%} = \frac{V_{OL} + V_{OH}}{2} \quad (3)$$

is denoted as t_{PHL} . Likewise, the amount of time, following the *trailing edge* of v_I , that it takes for v_O to swing from V_{OL} up to $V_{50\%}$ is denoted as t_{PLH} .

PART II – EXPERIMENTAL PART

This experiment is based on a LM3046 IC BJT array of the type of Lab #2, along with discrete BJTs of the 2N2222 (*nnp*) types and 2N3906 (*pnp*) types. The pin layouts for the three devices are shown in Fig. 8. Recall that in the LM3046 array, Q_1 and Q_2 are internally connected as a differential pair, the substrate is internally connected to Pin #13, also the emitter of Q_5 , and that this pin must always be connected to the *most negative voltage* (MNV) in the IC. The data sheets of the above devices can readily be downloaded from the Web (for instance, by visiting <http://www.google.com>). Recall that the LM3046 is a delicate device, so to avoid damaging it, make sure you always turn power off before making any

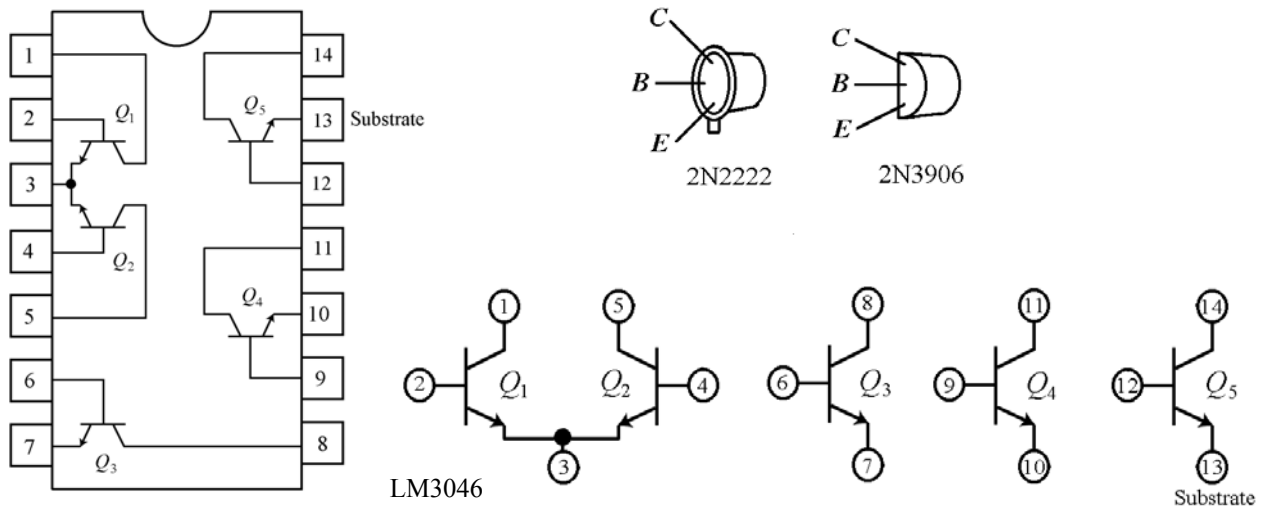


Fig. 8 - Pin layout for the 2N2222 *nnp* BJT, the 2N3906 *pnp* BJT, and the LM3046 IC *nnp* BJT array. **Note:** the substrate must be connected to the MNV.

circuit changes, and that before reapplying power, each lab partner checks separately that the circuit has been wired correctly. Also, refer to the Appendix for useful tips on how to wire proto-board circuits.

In this lab you are going to perform a variety of measurements as well as PSpice simulations. For the simulation of the 1N4148 diodes and the 2N2222/2N3906 BJTs, use the models already available in PSpice’s Library. For the BJTs of the LM3046 array, use the model called Q3946, along with the substrate diode model called Dsub, models that were employed above in the PSpice examples of Figs. 1 and 3. You can duplicate these examples by downloading their files from the Web. To this end, go to <http://online.sfsu.edu/~sfranco/CoursesAndLabs/Labs/445Labs.html>, and once there, click on **PSpice Examples**. Then, follow the instructions contained in the **Readme** file.

Henceforth, steps shall be identified by letters as follows: **C** for calculations, **M** for measurements, **P** for Prelab, and **S** for SPICE simulation.

A Homebrew Op Amp:

Figure 9 shows the circuit diagram of the op amp you are going to simulate and then try out in the lab. The *input* stage is made up of the differential pair Q_1 - Q_2 , along with the current mirror Q_6 - Q_7 as the active load. The *intermediate* stage is made up of the Darlington pair Q_8 - Q_9 , along with the current source Q_5 as the active load. The *output* stage is made up of the push-pull pair Q_{11} - Q_{12} , along with the biasing diodes D_1 - D_2 . The *biasing* network is made up Q_3 - Q_4 - Q_5 , with Q_4 forming a Widlar source. Frequency *compensation* is of the Miller type, and is provided by C_c . The BJTs of the LM3046 array are used to implement those stages in which matching is critical. In this respect it would be desirable that also Q_6 and Q_7 be matched. However, since *pnp* BJT arrays are not as readily available as *nnp* BJT arrays, we are using discrete *pnp* BJTs instead, along with the emitter-degeneration resistors R_3 and R_4 to swamp out the effect of any mismatches between V_{EB6} and V_{EB7} .

PS1: Draw the PSpice circuit schematic of the op amp of Fig. 9 (with the 10-k Ω potentiometer’s wiper set midway, or 5 k Ω on either side), and interconnect it as a *unity-gain voltage follower* with the input at ground, as shown in Fig. 10a. Though not specifically shown in Fig. 9, the substrate diodes of the LM3046 IC must be included for a realistic simulation. Then use PSpice to find

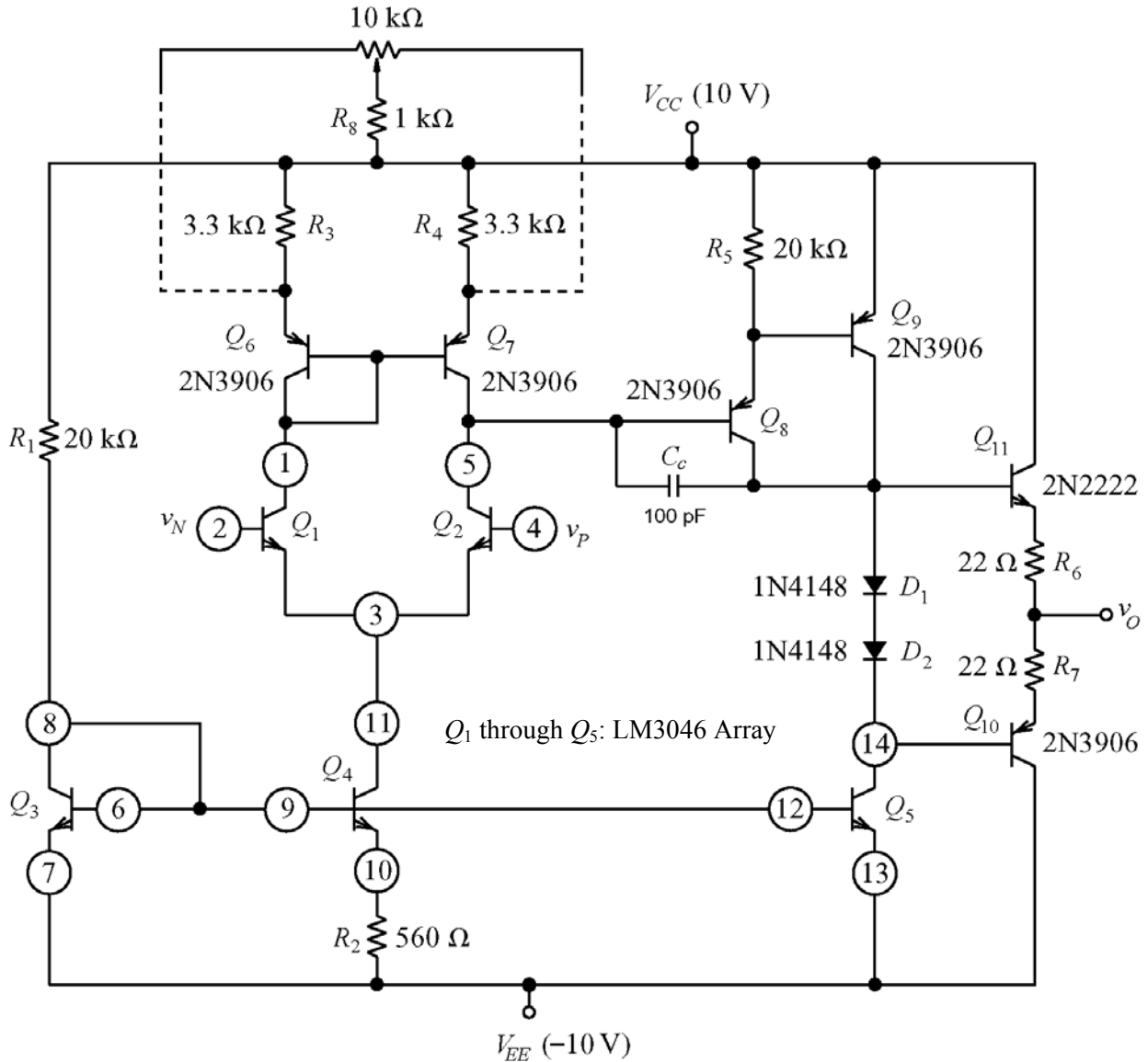


Fig. 9 – Homebrew op amp.

- the collector bias current I_C of each of the BJTs inside the op amp
- the input offset voltage V_{OS} , in this case coinciding with the DC voltage present at the output
- the input bias current $I_B = (I_P + I_N)/2$ and the input offset current $I_{OS} = I_P - I_N$
- the quiescent supply current I_Q of your entire circuit.

PS2: Use PSpice to plot the open-loop voltage transfer curve (VTC) of the op amp of Fig. 9 (with the 10-k Ω potentiometer's wiper still set midway). (For our purposes, we define the VTC as the plot of v_O versus v_P with v_N grounded.) Next, use this curve, along with the cursor facility of PSpice, to find

- the input offset voltage V_{OS} , given by horizontal shift from the point where $v_P = v_N = 0$ V
- the open-loop DC gain a_0 , given by the slope of the VTC near $v_O = 0$ V
- the output saturation voltages V_{OL} and V_{OH}

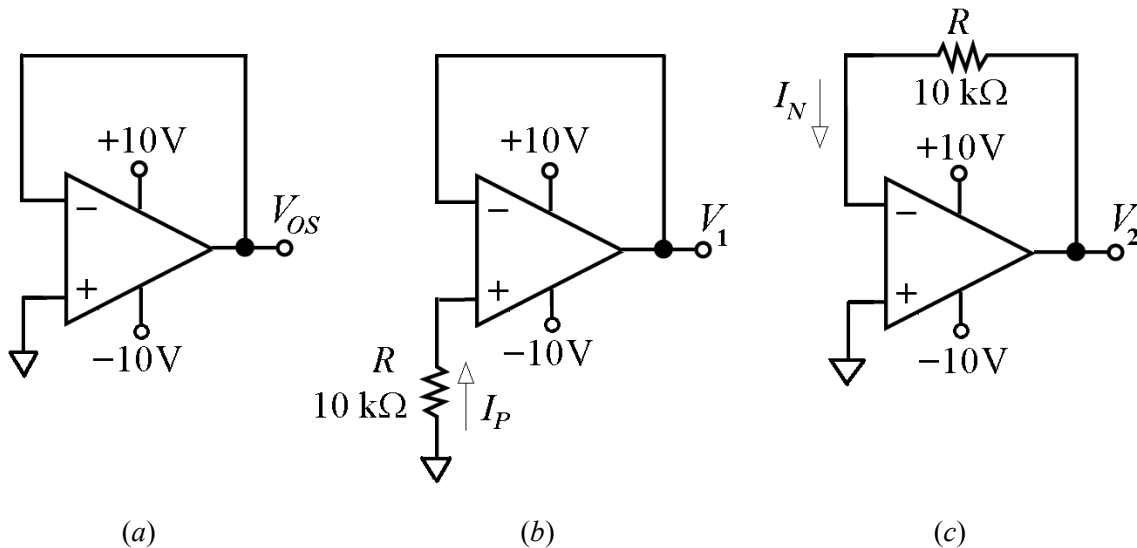


Fig. 10 – Test circuits to measure V_{OS} , I_P , and I_N .

How does the value of V_{OS} compare with that of Step PS1? Comment.

PS3: Using a combination of calculations and trials on the PSpice circuit of Step PS2, find a suitable *wiper setting* for the 10-k Ω potentiometer that will imbalance the input-stage's active load so as to shift the VTC horizontally until $v_O = 0$ V for $v_P = v_N = 0$ V.

PS4: For the offset-nulled op amp of Step PS3, use PSpice to find

- the *open-loop differential input resistance* r_{id}
- the *open-loop output resistance* r_o

PS5: For the offset-nulled op amp of Step PS3, use PSpice to plot the *small-signal open-loop frequency response* $a(jf)$ (both *magnitude* and *phase*), but *without connecting* the compensation capacitor C_c yet! (For our purposes, we define $a(jf) = V_o/V_p$ with V_n grounded.) Next, verify the existence of a frequency at which $\text{Ph}(a) = -180^\circ$, indicating that without C_c the op amp would oscillate if connected as a voltage follower. In fact, you may just want to verify this by performing the transient analysis of your op amp after connecting it as a voltage follower!

PS6: For the offset-nulled op amp of Step PS3, use PSpice to plot the *small-signal open-loop frequency response* $a(jf)$ (both *magnitude* and *phase*), but *now with the compensation capacitor* C_c in place. Then, determine from this plot the values of

- the *open-loop DC gain* a_0
- the *open-loop -3-dB frequency* f_b
- the *transition frequency* f_t

How does the value of a_0 compare with that found in Step PS2? How much phase shift does the op amp introduce at $f = f_t$? Comment.

Note: Take the value of 100 pF recommended for C_c only a *starting* value. You will find it quite instructive to run consecutive simulations for different values of C_c . You will observe that too small a value will result in excessive phase shift at $f = f_b$, while too large a value will lower f_t unnecessarily. In

fact, the best compromise is the value that results in a phase shift of -120° at $f=f_i$, which still ensures a phase margin of 60° . What is the corresponding value of C_c ?

PC7: Use the results of Step PS1 to predict the *slew rate* (SR) of your op amp as $SR = I_{C4}/C_c$. Use the results of Step PS6 to predict the *small-signal time constant* of your op amp as $\tau = 1/(2\pi f_i)$.

PS8: Configure the offset-nulled op amp of Step PS3 again as a *voltage follower*, and use PSpice to plot its *large-signal transient response* to a *square wave* alternating between -5 V and $+5$ V. Use the SR prediction of Step PC7 to specify an adequate period for your input square wave. Hence, determine from this plot the actual SR of your simulated circuit, compare with the predicted value of Step PC7, and account for any differences.

PS9: Configure the offset-nulled op amp of Step PS3 again as a voltage follower, and use PSpice to plot its *small-signal transient response* to a *square wave* of suitably small amplitude V_m and period T . To avoid slew-rate limiting effects, you must keep $V_m \leq SR \times \tau$. Also, for good visualization, choose $T \cong 5\tau$. Then, determine from this plot the actual value of τ of your simulated circuit, compare with the predicted value of Step PC7, and account for any differences

Trying out the Homebrew Op Amp in the Lab.

After all the above prelab work, we are now ready to try out our circuit experimentally. Thus, with power off, assemble the circuit of Fig. 9, but without interconnecting the 10-k Ω potentiometer yet. Make sure to keep leads short and to bypass both supply busses with 0.1- μ F capacitors. Figure 11 suggests a proto-board layout that will meet the above constraints reasonably well, and that you can use as a guideline for other circuits that you may want to breadboard in the future.

M10: With power still off, connect your op amp as in Fig. 10a. Next, apply power, and measure V_{OS} with the DVM. How does it compare with the value found via simulation in Step PS1? Finally, insert the 10-k Ω pot, and adjust its wiper until you drive V_{OS} to 0V. You have now nulled the input offset voltage!

MC11: Turn power off, and insert the 10-k Ω resistor shown in Fig. 10b. This is intended to cause the current I_P drawn by the *non-inverting input* to develop the voltage $V_P = -RI_P$, so that $V_1 = -RI_P$ (assuming the op amp is still offset-nulled!). Reapply power, measure V_1 , and calculate $I_P = -V_1/R$. How does it compare with the value found via simulation in Step PS1?

MC12: Turn power off, and connect the 10-k Ω resistor as in Fig. 10(c). By similar reasoning, the current I_N drawn by the *inverting input* will yield $V_2 = RI_N$ (assuming the op amp is still offset-nulled!). Reapply power, measure V_2 , and calculate $I_N = V_2/R$. How does it compare with the value found via simulation in Step PS1?

M13: We now wish to investigate the *frequency response* of our op amp using the test circuit of Fig. 12. Here, the op amp is configured to amplify the input v_i with the *closed-loop DC gain* $A_0 = 1/\beta = 1 + R_2/R_1 \cong 100$ V/V. To prevent v_o from clipping due to output-stage saturation, we must keep v_i suitably small, so we obtain it from the waveform generator v_s via a voltage divider such that $v_i = v_s R_4/(R_3 + R_4) \cong v_s/100$.

Thus, with power off, assemble the circuit of Fig. 12, keeping leads short. Also, while monitoring v_s with Ch. 1 of the oscilloscope set on DC, adjust the waveform generator so that v_s is a *sine wave* with a peak-to-peak amplitude of 5 V, 0-V DC offset, and initial frequency $f \sim 100$ Hz. Then, while monitoring v_o with Ch. 2 of the oscilloscope, gradually increase f while keeping the amplitude of v_s constant, until the amplitude of v_o drops to 70.7% of its low-frequency value. Record this frequency, which is the *closed-loop bandwidth* f_B of your op amp circuit. How does it compare with the value $f_B = \beta f_i \cong f_i/100$ predicted by theory? Comment.

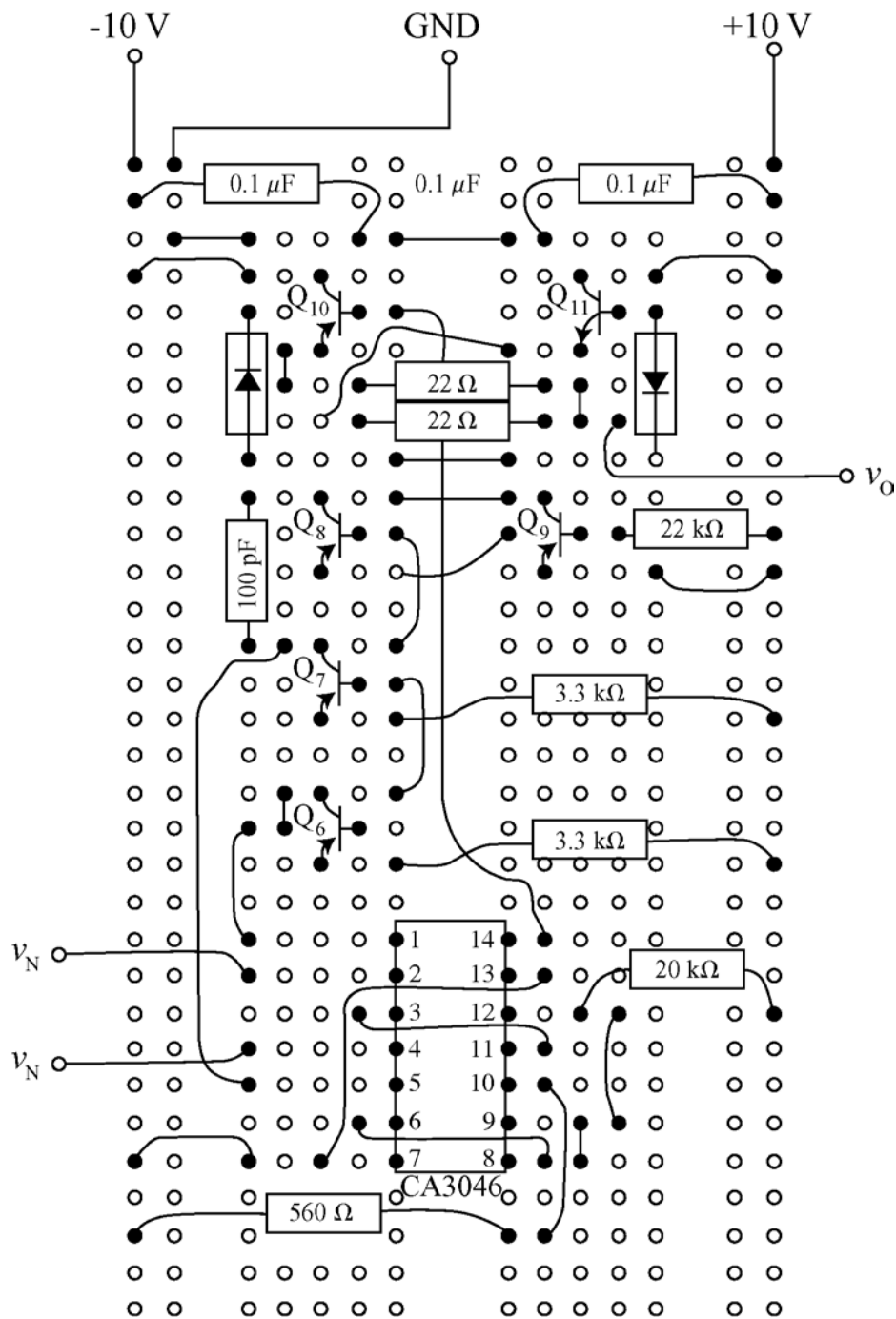


Fig. 11 – Suggested component layout on the proto-board.

M14: We now wish to observe the *small-signal transient response*. Thus, with power off, remove R_1 and R_4 from the circuit of Fig. 12, while leaving R_2 and R_3 in place. This again configures the op amp as a *voltage follower* (the reason for leaving R_2 and R_3 in place is to protect the op amp inputs against inadvertent overdrive). Reapply power, set the signal generator for a *square wave*, and adjust its

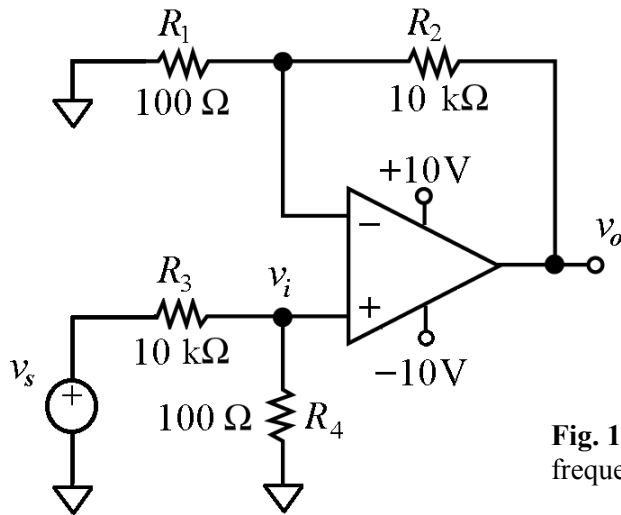


Fig. 12 – Test circuit to investigate the frequency response of the homebrew op amp.

amplitude and frequency so as to observe the *small signal* response under similar conditions as those anticipated by simulation in Step PS9. Measure the *time-constant* τ on the oscilloscope, compare with the value found via simulation in Step PS9, and account for any differences.

M15: We finally wish to observe the *large-signal transient response*. To this end, we still use the circuit of Step M14, but with the signal generator now adjusted so as to create similar conditions to those anticipated by simulation in Step PS8. Measure the *slew rate* SR on the oscilloscope, compare with the value found via simulation in Step PS8, and account for any differences.

A Homebrew Voltage Comparator:

Figure 13 shows the circuit schematic of the voltage comparator you are going to breadboard and investigate in the remainder of this lab. The current source Q_3 - Q_4 biases the differential pair Q_1 - Q_2 , which uses the current mirror Q_6 - Q_7 as an active load. The output of this gain stage is then converted to a TTL/CMOS-compatible voltage v_o by CE amplifier Q_5 . The 0.7-V drop provided by D_1 is designed to ensure that Q_5 goes convincingly off when $v_p < v_n$. Our investigation proceeds along similar lines to those of the homebrew op amp.

PS16: Draw the PSpice circuit schematic of the comparator of Fig. 13, and use PSpice to plot its VTC (v_o versus v_n with v_p grounded). Hence, use this curve to find

- the *output saturation voltages* V_{OL} and V_{OH}
- the *slope* at $v_o = V_{50\%}$, representing the *DC gain* a_0
- the amount of *horizontal shift* of $V_{50\%}$ from the origin, representing the *input offset voltage* V_{OS}
- the 10-k Ω potentiometer setting that will null V_{OS}

PS17: Configure your offset-nulled comparator as in Fig. 7 above, and use PSpice to plot its transient response for an input overdrive $V_{od} = 20$ mV. Hence, use the cursor facility of PSpice to find t_{PHL} and t_{PLH} .

Trying out the Homebrew Voltage Comparator in the Lab:

We now wish to try out our comparator experimentally. Thus, with power off, assemble the circuit of Fig. 13 (considering the fair amount of similarity with the homebrew op amp, especially in the input and biasing stages, you can recycle a good portion of the circuit already hardwired as per Fig. 11.)

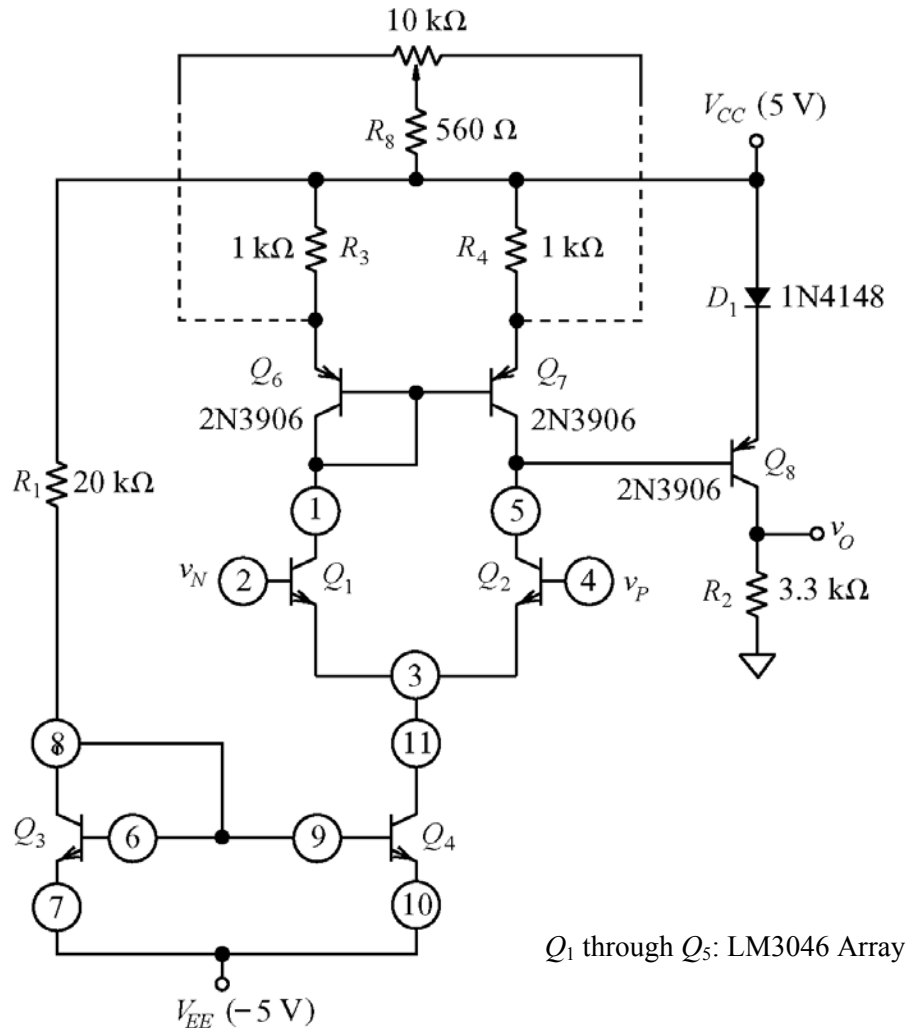


Fig. 13 - Homebrew voltage comparator.

M18: Connect the comparator's inputs to ground via two 100- Ω resistors R_1 and R_2 , as shown in Fig. 14 (don't connect R_3 and R_4 yet). Apply power, and while monitoring v_O with the oscilloscope, vary the potentiometer's wiper to make v_O saturate first at $v_O = V_{OL}$, then at $v_O = V_{OH}$. Record these values and compute $V_{50\%}$ via Eq. (3). How do these values compare with the simulated ones of Step PS16?

Finally, vary the potentiometer's wiper until you drive v_O as close to $V_{50\%}$ as possible. You have now nulled the input offset voltage!

M19: With power off, insert also the two 10-k Ω resistors R_3 and R_4 , as shown, and adjust the signal generator so that v_S is a pulse train alternating between 0 V and 2 V (with this arrangement, R_3 establishes an overdrive of 20 mV, and R_4 a baseline of -100 mV.) Finally, use the oscilloscope to measure the propagation delays t_{PLH} and t_{PHL} of your comparator. Compare with those of Step PS17, and comment.

Note: You may want to vary the amplitude of v_S and see how the amount of overdrive V_{od} affects the propagation delays. Comment on your observations.

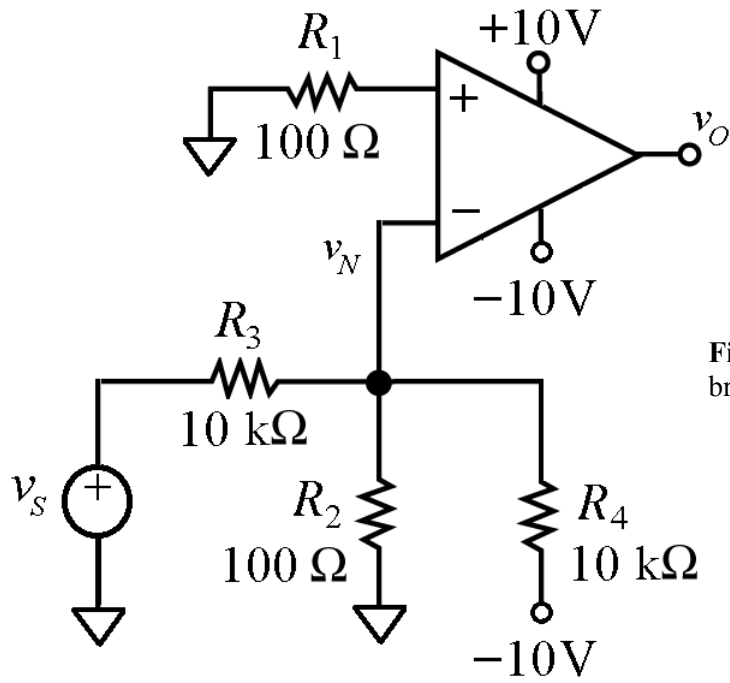


Fig. 14 – Test circuit to measure the home-brew comparator's *propagation delays*.