

LAB #3: ANALOG IC BUILDING BLOCKS

Updated: Dec. 23, 2002

Objective:

To investigate fundamental analog IC building blocks, such as current sources, current mirrors, active loads, and output stages.

Components:

1 × CA3046 IC BJT array, 1 × 2N2222 *nnp* BJT, 1 × 2N3906 *pnp* BJT, 3 × 0.1- μ F capacitors, 1 × 10-k Ω potentiometer, and resistors: 2 × 22 Ω , 2 × 100 Ω , 2 × 1.0 k Ω , 2 × 3.3 k Ω , 2 × 10 k Ω , and 4 × 100 k Ω (all 5%, ¼ W).

Instrumentation:

An adjustable regulated dual power supply, a digital multi-meter (DMM), a signal generator (sine wave), and a dual-trace oscilloscope.

Preliminary Considerations:

In this lab we are going to investigate the basic building blocks of BJT op amps: *current sources*, (basic, Wilson-type, and Widlar-type), *active loads*, and *output stages*. Each block will be tried out in the lab and also simulated via PSpice. Figure 1 shows a PSpice circuit to display the *i-v* characteristic of a basic current mirror. Figure 2 shows the characteristic, where we note a slight slant due to the finite output resistance of the collector. Moreover, the circuit exhibits current-mirror behavior only for $V_O \geq V_{CE(sat)} \cong 0.2$ V. For lower values of V_O , Q_2 saturates, and I_O undergoes even a polarity reversal in the vicinity of $V_O = 0$. You can duplicate this PSpice example on your own by downloading its appropriate files from the Web. To this end, go to <http://online.sfsu.edu/~sfranco/CoursesAndLabs/Labs/445Labs.html>, and once there, click on [PSpice Examples](#). Then, follow the instructions contained in the **Readme** file.

EXPERIMENTAL PART

This experiment is based on the CA3046 BJT array of Lab # 2, along with discrete BJTs of the 2N2222 (*nnp*) and 2N3906 (*pnp*) types. The pin layouts for the three device types are shown in Fig. 2. Recall that in the CA3046 array, Q_1 and Q_2 are internally connected as a differential pair, the substrate is internally connected to Pin #13 (also the emitter of Q_5), and that this pin must always be at the *most negative voltage* (MNV) in the IC. The data sheets of all of the above devices can be downloaded from

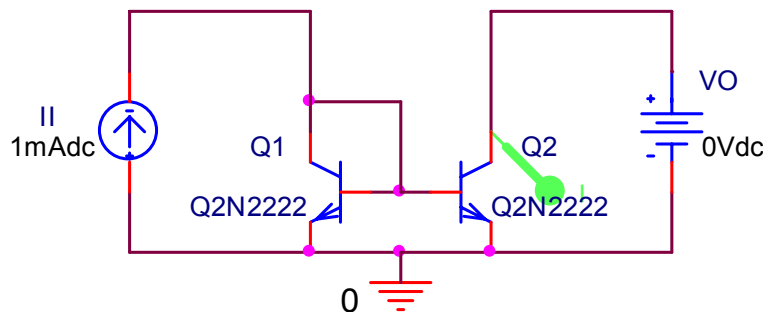


Fig. 1 – Pspice circuit to plot the *i-v* characteristic of a current mirror.

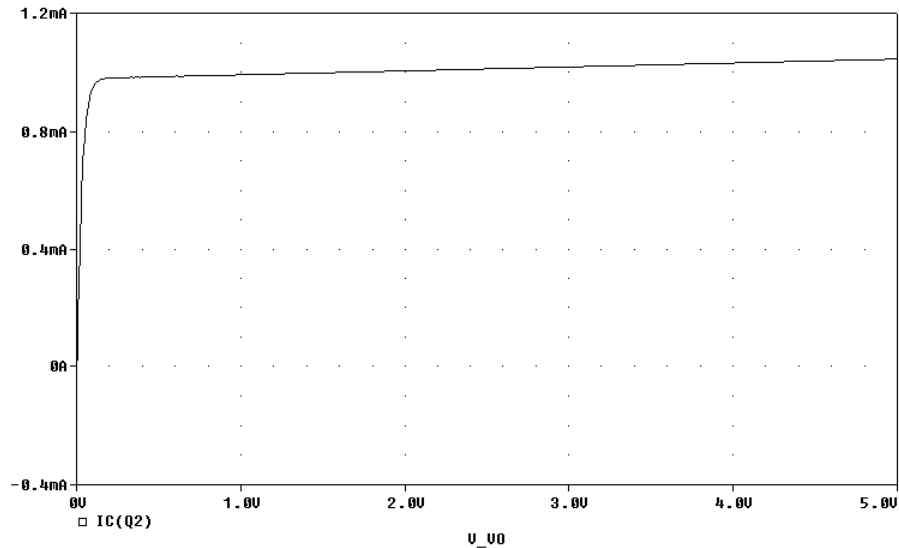


Fig. 2 - The i - v characteristic of the current mirror of Fig. 1.

the Web (for instance, by visiting <http://www.google.com>, and searching for the given part numbers).

The CA3046 is a delicate device, so to avoid damaging it, make sure you always turn power off before making any circuit changes, and that before reapplying power, each lab partner checks separately that the circuit has been wired correctly. Also, refer to the Appendix for useful tips on how to wire protoboard circuits.

Henceforth, steps shall be identified by letters as follows: **C** for calculations, **M** for measurements, **P** for Prelab calculations, and **S** for SPICE simulation.

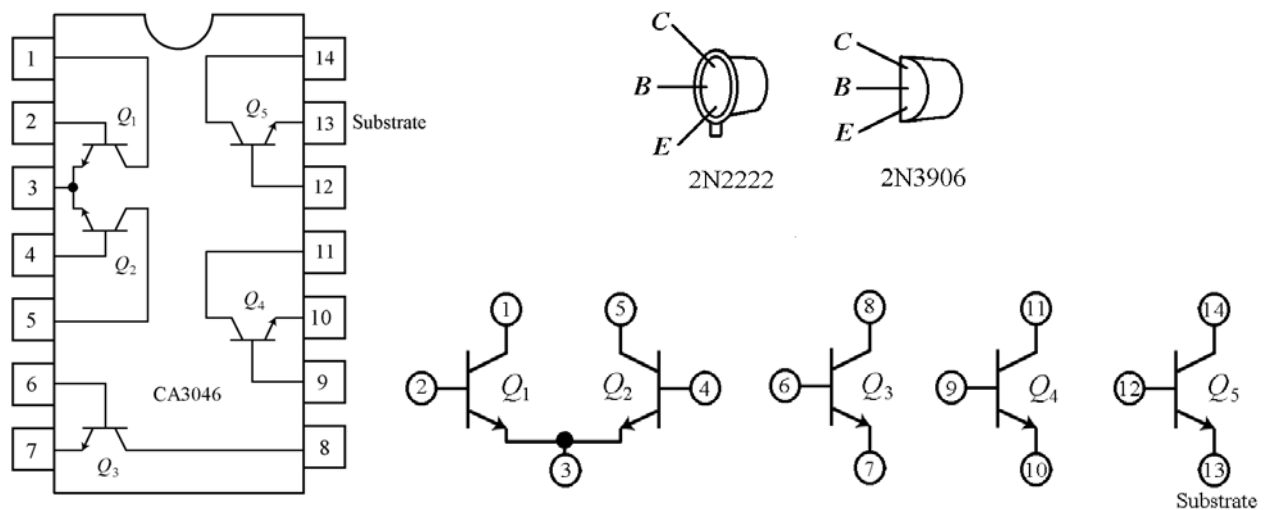


Fig. 3 - Pin layout for the 2N2222 *nnp* BJT, the 2N3906 *pnp* BJT, and the CA3046 BJT array.

Note: The substrate of the CA3046 (Pin #13) must be connected to the MNV.

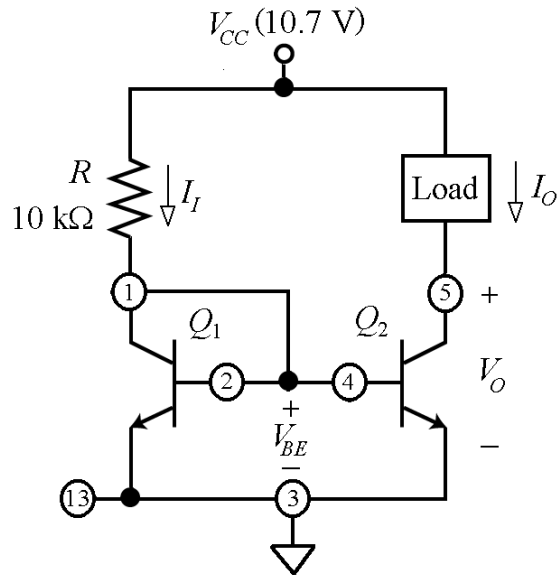


Fig. 4 – Basic current source

Basic Current Source:

In its simplest form, shown in Fig. 4, a current source utilizes Q_1 to generate a suitable voltage drop V_{BE} to bias Q_2 , the device intended to act as a current source (actually, in this case Q_2 is *sinking* current from the load, so a more appropriate designation would be *current sink*). The function of R is to establish a *reference current* $I_I = (V_{CC} - V_{BE})/R$ through Q_1 . This circuit gives, for $V_O \geq V_{CE(EOS)} \cong 0.2$ V,

$$I_O = I_I \frac{I_{s2}}{I_{s1}} \left(1 - \frac{2}{\beta_F} \right) \times \left(1 + \frac{V_O - V_{BE}}{V_A} \right) \quad (1a)$$

where I_{s1} and I_{s2} are the *collector saturation* currents of Q_1 and Q_2 , β_F is the mean current gain, and V_A is the *Early voltage*.

Ideally, we would like $I_O = I_I$ (hence the reason why the circuit is also called a *current mirror*). Moreover, for true current-source behavior, I_O should be *independent* of V_O . In practice, I_O will deviate somewhat from I_I as a result of mismatches between I_{s1} and I_{s2} as well as an error term due to finite β_F . Moreover, I_O exhibits a dependence on V_O , however weak. We model this dependence with a *finite output resistance* R_o . For the present circuit,

$$R_o = r_o \quad (1b)$$

where r_o is the collector's small-signal output resistance of Q_2 . Its value is found as $r_o = V_A/I_O$.

PC1: Assuming V_{CC} has been adjusted for $I_I = 1.00$ mA in the circuit of Fig. 4, use the data obtained experimentally in Lab #2 for Q_1 and Q_2 of the LM3046 BJT Array to predict I_O and R_o for the case in which the load is a resistance $R_L = 6.8$ k Ω

MC2: With power off, assemble the circuit of Fig. 5a, keeping leads short and bypassing the power supply with a 0.1- μ F capacitor as recommended in the Appendix. Next, apply power and adjust V_{CC} so that the digital current meter (DCM) reads $I_I = 1.00$ mA. Once I_I has been calibrated, turn again power off and insert the DCM as in Fig. 5b. Then, reapply power, and measure I_O . How does it compare with the value predicted in Step PC1? Account for any possible discrepancies.

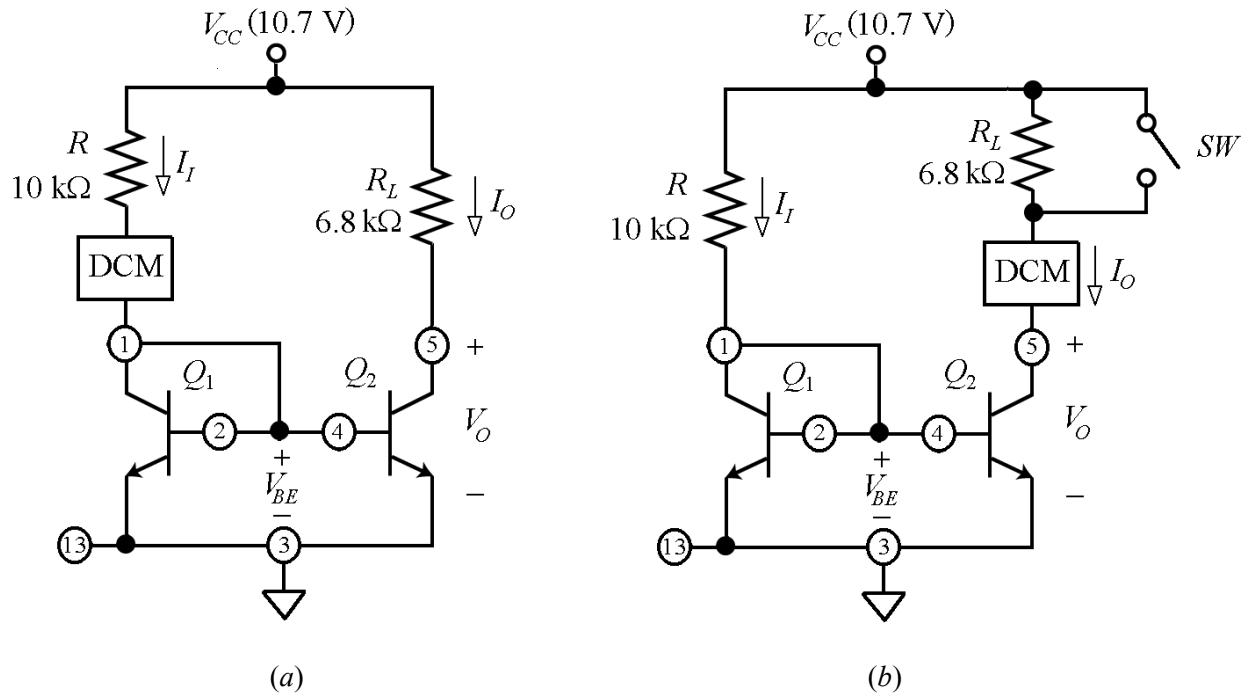


Fig. 5 – Test circuits to (a) calibrate and (b) characterize the basic current source of Fig. 4.

Finally, short out R_L with a wire (that is, close switch SW), record the corresponding change ΔI_C , and calculate $R_o = \Delta V_O / \Delta I_C$, where $\Delta V_O = R_L I_O$. How does R_o compare with the value predicted in Step PC1? Account for any possible discrepancies.

PS3: Use PSpice to display the *output characteristic* (that is, to plot I_O versus V_O) of the current source of Fig. 4 over the range $0 \leq V_O \leq 10$ V. For a realistic simulation, use the model Q3036 developed in Lab #2 for the BJTs of the LM3046 array. Compare simulated data with experimental data, and account for any discrepancies.

Wilson Current Source:

Adding to the basic source of Fig. 4 a third BJT in the manner of Fig. 6 offers the double benefit of reducing the error term due to finite β_F , and increasing R_o via negative feedback. The improved source, called the *Wilson current source* for its inventor, gives, for $V_O \geq V_{BE} + V_{CE(sat)}$,

$$I_O = I_I \frac{I_{s2}}{I_{s1}} \left(1 - \frac{2}{\beta_F^2} \right) \times \left(1 + \frac{V_O - 2V_{BE}}{(\beta_0/2)V_A} \right) \quad (2a)$$

and

$$R_o = \frac{\beta_0}{2} r_o \quad (2b)$$

PC4: Assuming V_{CC} has been adjusted for $I_I = 1.00$ mA in the Wilson source of Fig. 6, use the data obtained experimentally in Lab #2 for Q_1 , Q_2 , and Q_3 of the LM3046 BJT Array to predict I_O and R_o for the case in which the load is a resistance $R_L = 6.8$ k Ω

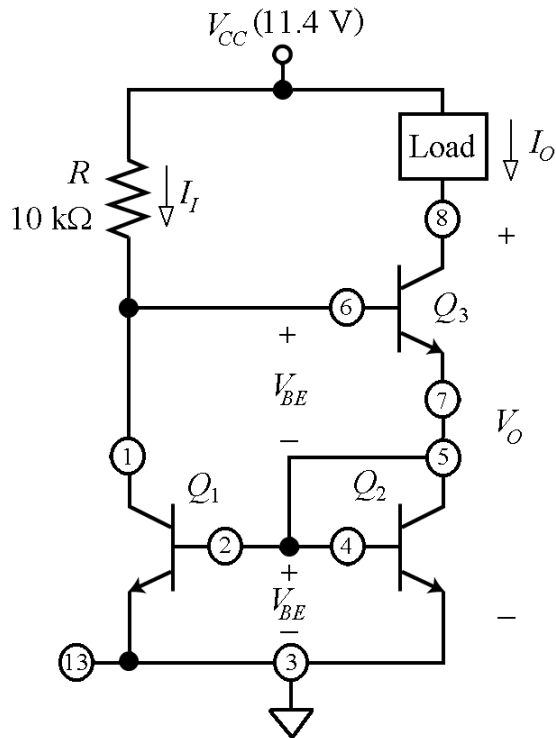


Fig. 6 – Wilson current source.

MC5: Repeat Step MC2, but for the Wilson source of Fig. 6. How do the experimental values of I_O and R_o compare with those predicted in Step PC4? Account for any differences.

CS6: Repeat step PS3, but for the Wilson source of Fig. 6. Discuss how closely simulation reflects experimentation.

Widlar Current Source:

The source of Fig. 4 is unsuited to the generation of low currents as it would require unrealistically large values of R . This inconvenient is avoided by inserting a resistance in series with Q_2 's emitter to decrease V_{BE2} by a prescribed amount ΔV_{BE} , and thus reduce I_O accordingly. The result is the *Widlar current source* of Fig. 7, so called for its inventor.

To test this source for different values ΔV_{BE} and I_O , we use the setups of Fig. 8. Here, the function of the diode and corresponding resistor to bias Q_2 's collector at about 0.7 V, and thus ensure the same collector bias conditions as Q_1 . We then use a potentiometer to establish different values for ΔV_{BE} .

M7: With power off, assemble the circuit of Fig. 8a with the wiper initially all the way up so as to ensure $\Delta V_{BE} = 0$. Keep leads short and bypass the power supply with a 0.1- μ F capacitor as usual. Apply power and adjust V_{CC} so that the digital current meter (DCM) reads $I_O = 1.00$ mA. Once adjusted, the power supply should not be changed again. We are now ready to perform a series of I_O and ΔV_{BE} measurements as follows:

- In Fig. 8a adjust the potentiometer so that $I_O = (1.00 \text{ mA})/2$. Turn power off, reconfigure the circuit as in Fig. 8b, reapply power, and use the digital voltmeter (DVM) to measure the corresponding value of ΔV_{BE} . Record this value for later use.
- Repeat, but with the potentiometer now adjusted for $I_O = (1.00 \text{ mA})/10$.
- Repeat, but with the potentiometer now adjusted for $I_O = (1.00 \text{ mA})/20$.

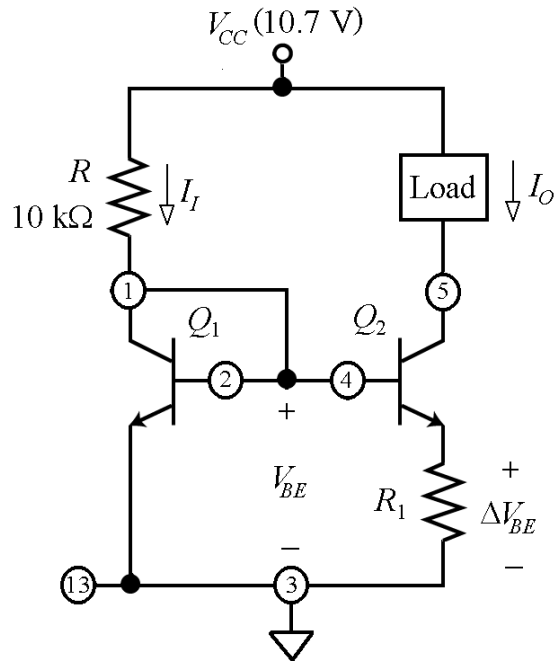


Fig. 7 – Widlar current source.

- Repeat, but with the potentiometer now adjusted for $I_O = (1.00 \text{ mA})/100$. (If the potentiometer's range is insufficient, use a suitable series resistance.)
- Finally, discuss your findings in light of the useful rule-of-thumb: To change I_O by one octave (or by one-decade), you need to change V_{BE} by 18 mV (or by 60 mV).

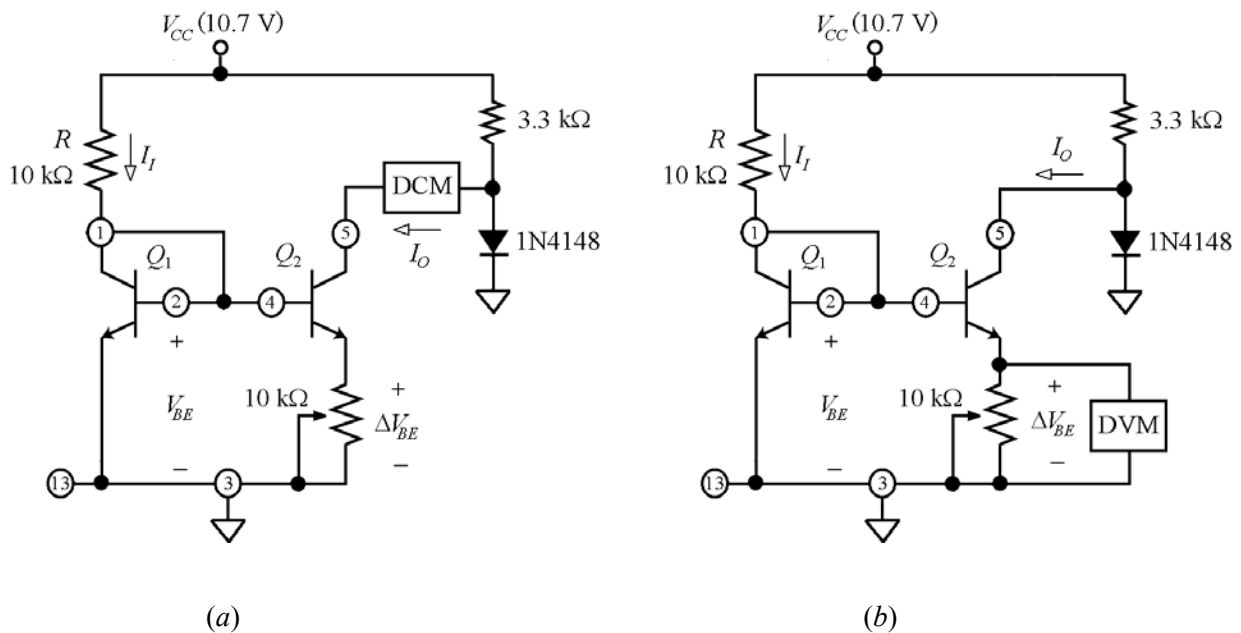


Fig. 8 – Test circuits to investigate the Widlar current source of Fig. 7.

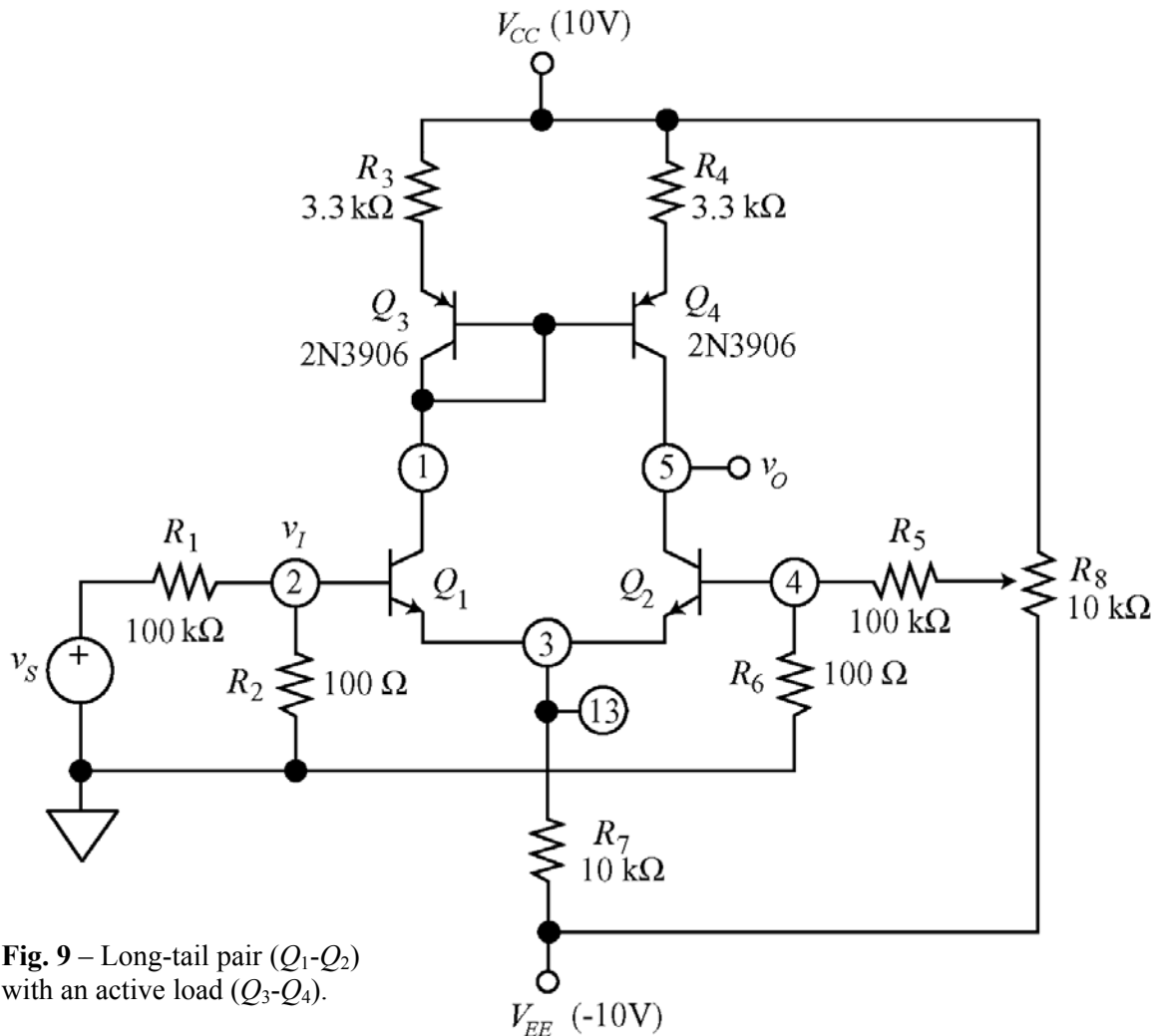


Fig. 9 – Long-tail pair (Q_1 - Q_2) with an active load (Q_3 - Q_4).

Active Loads:

An important current-mirror application is as an *active load* for a long-tail pair, as exemplified in Fig. 9. This configuration provides *much higher voltage gain* than in the case of a passive (resistive) load, and also converts a double-ended input to a *single-ended* output. In Fig. 9, the *npn* BJTs Q_1 and Q_2 form the long-tail pair, and the *pnp* BJTs Q_3 and Q_4 form the current-mirror active load. Moreover, we use the voltage at Pin #2 as the *signal input*, and the voltage at Pin #4 for *output offset adjustment*. In this lab we use discrete devices for Q_3 and Q_4 , which are unlikely to be matched. So, we include the emitter-degeneration resistors R_3 and R_4 to develop voltage drops much larger than any mismatches between V_{EB3} and V_{EB4} , thus forcing Q_3 and Q_4 to conduct virtually identical currents.

In the following we express a signal in the familiar form

$$v_S = V_S + v_s \quad (3)$$

where

- v_S is the *total* signal
- V_S is its *DC component*
- v_s is its *AC component*

With this in mind, we find the *small-signal voltage gain* and *output resistance* to be, respectively,

$$a = \frac{v_o}{v_i} = g_m R_o \quad (4)$$

$$R_o = r_{on} // \{r_{op}[1 + g_m(r_{\pi p} // R_4)]\}$$

where subscripts *n* and *p* identify parameters of the *npn* and *pnp* BJTs, respectively. Given the large amount of degeneration introduced by R_4 , we have $r_{op}[1 + g_m(r_{\pi p} // R_4)] \gg r_{on}$, indicating that we can approximate

$$R_o \cong r_{on} \quad (5)$$

and thus spare ourselves the need to characterize also the *pnp* BJTs. Equation (5) provides us for quick estimates for *a* and R_o , namely

$$a = \frac{V_{A2}}{V_T} \quad R_o = \frac{V_{A2}}{I_{C2}} \quad (6)$$

It is apparent that the present circuit provides a gain on the order of 10^3 V/V (or higher), and an output resistance on the other of $10^5 \Omega$ (or higher). With such a high gain, we use the input voltage divider consisting of R_1 and R_2 to scale down the waveform generator output v_S to a sufficiently small input $v_I = v_S R_2 / (R_1 + R_2) \cong v_S / 1000$. The entire circuit can then be modeled as in Fig. 10, with the DC component V_{DC} being adjustable via the 10-k Ω potentiometer of Fig. 9. We also observe that the upper and lower saturation limits for v_o in Fig. 9 are, respectively,

$$V_{OL} = -V_{BE2} + V_{CE2(sat)} \quad (7a)$$

$$V_{OH} = V_{CC} - V_{R_4} - V_{EC4(sat)} \quad (7b)$$

It is apparent that the output voltage range is maximized when V_{DC} is set *half-way* between V_{OL} and V_{OH} .

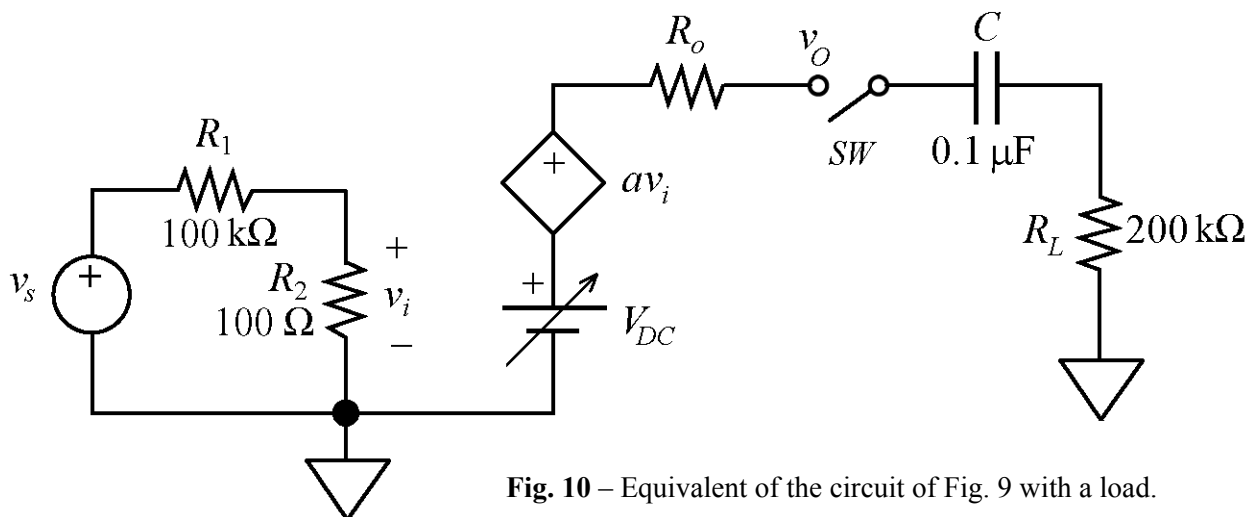


Fig. 10 – Equivalent of the circuit of Fig. 9 with a load.

Our objective is to determine a and R_o experimentally. To find a , we perform an *open-circuit* (or *unloaded*) measurement of the output AC component. Denoting its value as $v_{o(\text{unloaded})}$, we then calculate

$$a = \frac{v_{o(\text{unloaded})}}{v_i} \quad (8)$$

To find R_o , we intentionally *load down* the output with a load resistance of known value R_L and measure

$$v_{o(\text{loaded})} = \frac{R_L}{R_o + R_L} v_{o(\text{unloaded})}$$

Then, we solve for R_o as

$$R_o = R_L \left(\frac{v_{o(\text{unloaded})}}{v_{o(\text{loaded})}} - 1 \right) \quad (9)$$

For the above measurements to be reliable, it is important that you perform your output measurements with a *high-impedance probe*, such as a 10-M Ω X10-probe.

MC8: With power off, assemble the circuit of Fig. 9, keeping leads short, connecting the substrate (pin 13) to the MNV in the IC (-0.7 V), and bypassing both supplies via 0.1- μF capacitors, as recommended in the Appendix. To limit the amount of ground noise pickup, keep the distance between the bottom leads of R_2 and R_2 as short as possible. Next, apply power, and while monitoring v_s with Ch.1 of the scope set on DC, and v_o with Ch. 2 of the scope also set on DC (for Ch. 2 use a X10 probe!), proceed as follows:

- Adjust the waveform generator so that v_s is a 1-kHz *sine wave* with $V_S = 0$ V and $v_s = 1$ V peak-to-peak (this makes $v_i = 1$ mV peak-to-peak).
- Adjust the 10-k Ω potentiometer for $V_O \cong 4.5$ V, which should be about half-way between V_{OL} and V_{OH} .
- Gradually increase the amplitude of v_s until v_o just begins to clip both at the top (V_{OH}) and at the bottom (V_{OL}). (For symmetric clipping, you may need to readjust the 10-k Ω pot slightly.) Finally, record the corresponding values of V_{OH} and V_{OL} , compare them with the values predicted by Eq. (7), and justify any discrepancies.

• **MC9:** Without altering the 10-k Ω pot setting of Step MC8, reduce the amplitude of v_s until $v_o = 5.0$ V peak-to-peak. Record the corresponding peak-to-peak amplitude of v_s , and find the experimental gain as $a = 1000(v_o/v_s)$, where the factor of 1000 stems from the presence of the input attenuator made up of R_1 and R_2 . Compare with the value predicted for a by Eq. (6), and justify any differences.

MC10: With everything as in Step MC9, connect an output load $R_L = 200$ k Ω (use 2×100 k Ω in series) as shown in Fig 10. Here, the purpose of the 0.1- μF capacitor is to load down only v_o , while leaving V_O undisturbed. As a consequence, v_o will change from the value $v_{o(\text{unloaded})} = 5.0$ V to a new value, aptly called $v_{o(\text{loaded})}$. Record this new value, and then use Eq. (9) to find R_o . Compare with the value predicted for R_o by Eq. (6), and justify any differences.

MC11: Remove the output load so as to return to the conditions, and then:

- Lower the waveform generator's frequency f to verify that the circuit amplifies by a all the way down to DC (for practical purposes, go as far down as $f \sim 10$ Hz).

- Raise f until the peak-to-peak amplitude of v_o drops from 5.0 V to $5/\sqrt{2} \cong 3.55$ V. This represents the -3 -dB frequency, which for the present circuit is

$$f_{-3 \text{ dB}} = \frac{1}{2\pi R_o C_{eq}} \quad (10)$$

where R_o is the output resistance found in Step MC10, and C_{eq} is the *net stray capacitance* of the output node. This capacitance is $C_{eq} = C_{\mu 2} + C_{\mu 4} + C_p + C_w$, where, $C_{\mu 2}$ and $C_{\mu 4}$ are the B-C junction capacitances of Q_2 and Q_4 , C_p is the capacitance of the probe, and C_w the capacitance of the wires.

- Using Eq. (10), along with the experimental values of R_o and $f_{-3 \text{ dB}}$, estimate C_{eq} , and comment on its value.

S12: Simulate the circuit of Step MC9 via PSpice, and devise a way to find both a and R_o . Compare with the measured values, and justify any discrepancies.

Note: For Q_3 and Q_4 use the BJT models available in PSpice's Library; and for Q_1 and Q_2 use the model Q3036 developed in Lab #2.

Output Stages:

The role of an output stage is to provide *power gain* with *high input impedance* and *low output impedance*. The natural candidate for this task is the emitter follower. However, in order to provide both current sourcing and sinking capabilities, two such followers are needed, an *npn* type to *source* and a *pnnp* type to *sink* current. The result is known as the *push-pull* configuration, of which Fig. 11 shows a simple realization. Here R_1 and R_2 are used to sense the collector currents of Q_1 and Q_2 , as well as to limit these currents in case of output overloading, and R_S is used to protect the bases of the BJTs against input overdrive.

M13: With power off, assemble the circuit of Fig. 11, keeping leads short and bypassing both supplies

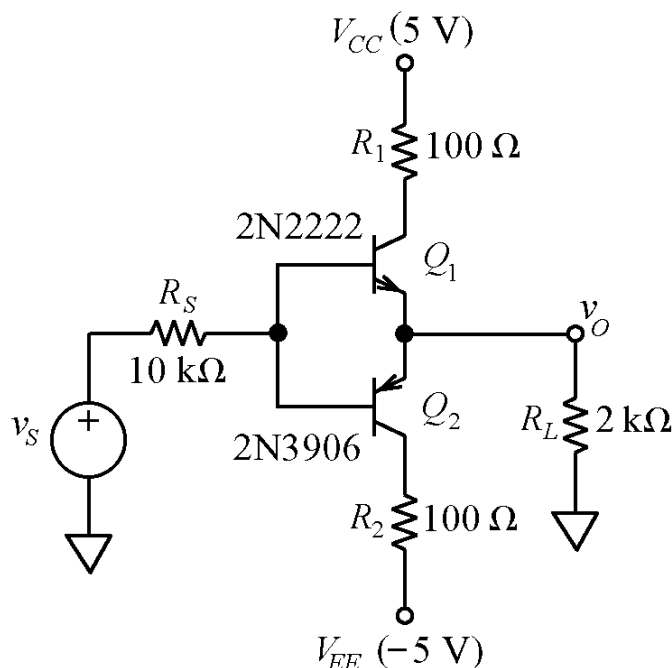


Fig. 11 –Push-pull output stage.

with 0.1- μF capacitors (implement the 2-k Ω load with two 1.0-k Ω resistors in series). Next, apply power, adjust the waveform generator so that v_s is a 100-Hz *triangle wave* with 0-V DC and about ± 7.5 -V peak values, and use the oscilloscope in the *x-y* mode to observe the *voltage-transfer curve* (VTC) of the circuit. Record the curve on paper, label all breakpoints, slopes, and saturation levels, and justify them in terms of circuit operation and given component values.

M14: Switch the oscilloscope to the usual dual-trace display mode, and adjust the waveform generator so that v_s is a 1-kHz *sine wave* with $V_s = 0$ V.

- Starting with $v_s = 0$ V, gradually increase its amplitude until you just begin to see an ac signal v_o appear at the output. For what range of values of v_s can we say that both BJT's are essentially off? Confirm this by observing the voltages of the current-sensing resistances R_1 and R_2 .
- Raise v_s to ± 5 -V peak values, and record v_o as well as the collector currents of the BJTs, which can be found via Ohm's law from the voltages across R_1 and R_2 , and justify your findings in terms of circuit operation and the given component values.
- Repeat, but with v_s raised to about ± 7.5 -V peak values; and comment.

S15: Simulate the circuit of Fig. 11 via PSpice, and display its VTC as well as its input and output waveforms as per Step M14.

Reducing Output Distortion:

The large amount of distortion afflicting the basic push-pull stage of Fig. 11 in connection with the

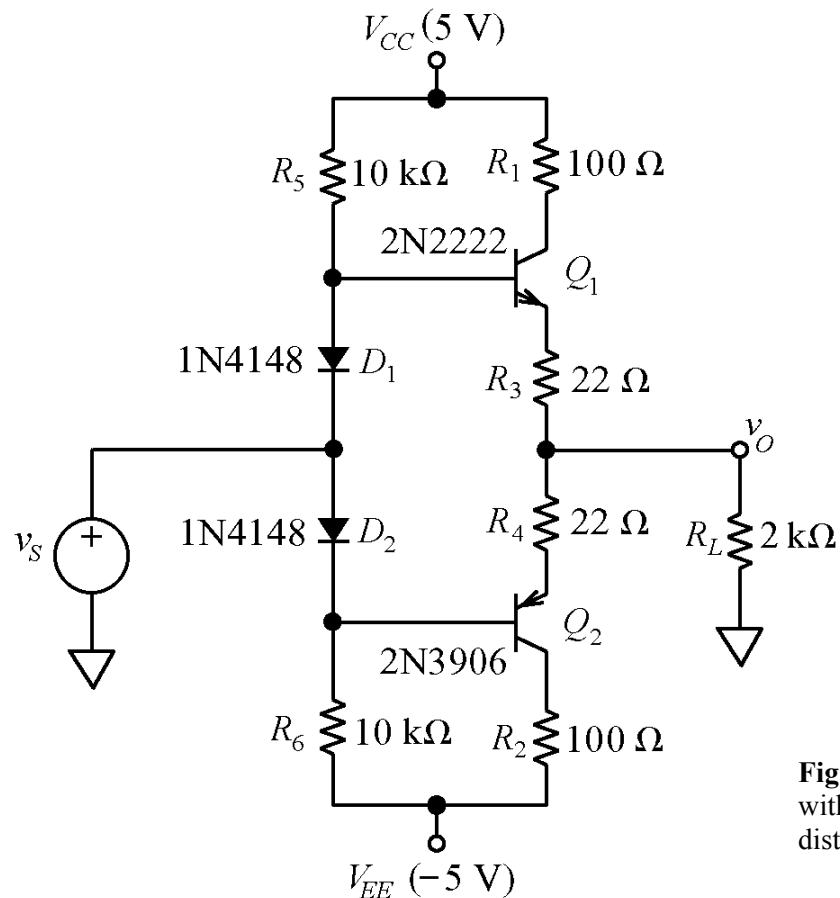


Fig. 12 – Push-pull output stage with provision for zero-crossing distortion elimination.

waveform's zero-crossings is dramatically reduced if we pre-bias the BJTs with two V_{BE} drops, in the manner depicted in Fig. 12. Here, the pre-bias function is provided by D_1 and D_2 , while R_3 and R_4 serve the purpose of protecting Q_1 and Q_2 against possible thermal runaway.

M16: Proceeding as in Steps M13 and M14:

- Display the VTC of the circuit of Fig. 12, record it on paper, label all breakpoints, slopes, and saturation levels, and justify them in terms of circuit operation and the given component values.
- Apply a 1-kHz *sine wave* of 0-V DC and variable amplitude, and verify that the circuit yields $v_o \cong v_s$ all the way *down to small amplitudes*. What is the *upper limit* on the amplitude of v_s before the circuit starts to distort? Justify quantitatively in terms of the VTC just observed.

MC17: Using the DVM, measure V_O as well as the voltage drops V_{R_1} and V_{R_2} across R_1 and R_2 for the following values of V_S : -5 V , -4 V , -3 V , \dots , 0 V , \dots , $+4\text{ V}$, $+5\text{ V}$. Then, tabulate V_O as well as the collector currents $I_{C1} = V_{R_1} / R_1$ and $I_{C2} = V_{R_2} / R_2$, and comment.

Note: To synthesize the above voltages, connect the 10- k Ω potentiometer between the sup[ply voltages and obtain the desired voltage from the wiper.

S18: Simulate the circuit of Fig. 12 via PSpice, compare with the findings of Steps M16 and M17, and justify any differences.