LAB #2: BJT CHARACTERISTICS AND THE DIFFERENTIAL PAIR

(Updated August 11, 2003)

Objective:

To characterize an IC array of matched BJTs. To assess the degree of matching. To appreciate the benefits of matching via the differential pair.

Components:

1 × LM3046 IC BJT array, 2 × 0.1-μF capacitors, 1 × 10-kΩ potentiometer, and resistors: 2 × 100 Ω, 5 × 10 k Ω, 1 × 100 kΩ, and 1 × 1.0 MΩ (all 5%, ¼ W).

Instrumentation:

A dual adjustable regulated power supply, a digital multi-meter (DMM), a signal generator (sine wave), and a dual-trace oscilloscope.

PART I – THEORETICAL BACKGROUND

Figure 1 shows the voltage polarities and current directions for the *npn* and the *pnp* BJTs. Note that the polarities and directions of one device are *opposite* to those of the other. Moreover, by KCL, we have $i_C + i_B = i_E$ for both transistors.

When a low-power *npn* BJT is biased in the *forward-active* (FA) *region*, characterized by the conditions

$$v_{BE} = V_{BE(\text{on})} \cong 0.7 \text{ V} \qquad (1a)$$

$$v_{CE} \geq V_{CE(\text{EOS})} \cong 0.2 \text{ V} \qquad (1b)$$

its *collector* current i_C depends on the applied *base-emitter* voltage drop v_{BE} and the operating *collector-emitter* voltage v_{CE} as

$$i_C = I_{sn} e^{v_{BE}/V_T} \left(1 + \frac{v_{CE}}{V_{An}}\right) \qquad (2)$$

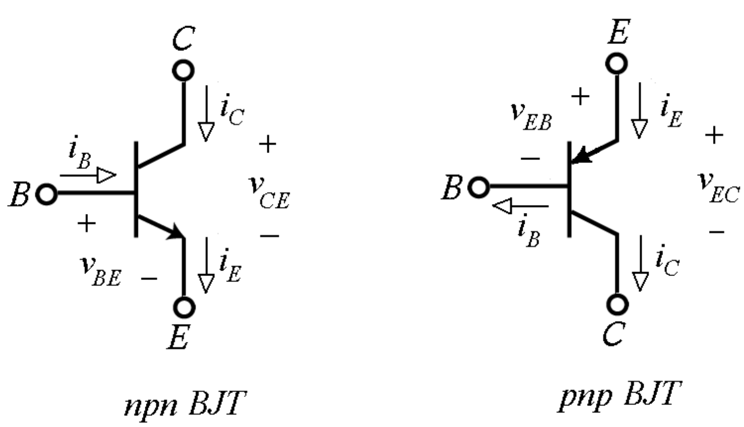


Fig. 1 – BJT symbols with *current directions* and *voltage polarities*.

where

- I_{sn} is a scale factor known as the *collector saturation current* of the *npn* BJT
- V_T is a scale factor known as the *thermal voltage*
- V_{An} is yet another scale factor known as the *Early voltage* of the *npn* BJT

At room temperature, $V_T \cong 26$ mV. Moreover, for a low-power BJT, the room-temperature value of I_{sn} is typically on the order of fAs (1 FA = 10^{-15} A), and V_{An} is on the order of 10^2 V. The extrapolated value of i_C in the limit $v_{CE} \to 0$ is $i_C = I_{sn}[\exp(v_{BE}/V_T)]$.

The dependence of i_C upon v_{BE} for a fixed value of v_{CE} is the familiar *pn*-junction *exponential characteristic*, which enjoys a number of significant properties:

- To effect an *octave* change in i_C we need to change v_{BE} by 18 mV
- To effect a *decade* change in i_C we need to change v_{BE} by 60 mV
- At room-temperature, the voltage drop v_{BE} exhibits a temperature coefficient of about –2 mV/°C
- The *slope* of the curve at a particular operating point I_C, called the *transconductance* g_m (in mA/V or also in 1/Ω), depends on how far up we are on the curve, according to

$$g_m = \frac{I_C}{V_T} \tag{3}$$

To get a practical feel, remember that at $I_C = 1$ mA we have $g_m = 1/26 = 38.5$ mA/V = 1/(26 Ω).

Similar considerations hold for *pnp* BJTs, provided we *reverse* all *current directions* and *voltage polarities*. Thus, the forward-active conditions of Eq. (1) become, for a *pnp* BJT,

$$v_{EB} = V_{EB(\text{on})} \cong 0.7 \text{ V} \tag{4a}$$

$$v_{EC} \geq V_{EC(\text{EOS})} \cong 0.2 \text{ V} \tag{4b}$$

and Eq. (2) is rephrased as

$$i_C = I_{sp} e^{v_{EB}/V_T} \left(1 + \frac{v_{EC}}{V_{Ap}}\right) \tag{5}$$

Likewise, the extrapolated value of i_C in the limit $v_{EC} \to 0$ is $i_C = I_{sp}[\exp(v_{EB}/V_T)]$.

An insightful way of illustrating BJT operation is by plotting i_C versus v_{CE} for different values of i_B. The PSpice circuit of Fig. 2 uses the popular 2N2222 *npn* BJT to generate such a plot for incremental steps in i_B of 2 μA each. The resulting family of curves, shown in Fig. 3, reveals *three regions* of operation for the BJT:

- For $i_B = 0$, we get $i_C = 0$, indicating that the BJT is operating in the ***cutoff*** **(CO)** ***region***. In this region, the *base-emitter* (BE) *junction* and the *base-collector* (BC) *junction* are either reverse biased, or not sufficiently forward-biased to carry convincing currents, so both junctions act essentially as *open circuits*.
- For $i_B > 0$, the BJT is *on*. The region corresponding to $i_C > 0$ and $v_{CE} > V_{CE(\text{EOS})} \cong 0.2$ V is called the ***forward-active*** **(FA)** ***region***. Here, the *BE junction is forward biased* at $v_{BE} = V_{BE(\text{on})} \cong 0.7$ V, and the *BC junction is reverse biased*, or at most it is forward-biased at 0.7 – 0.2 = 0.5 V, which is *insufficient*

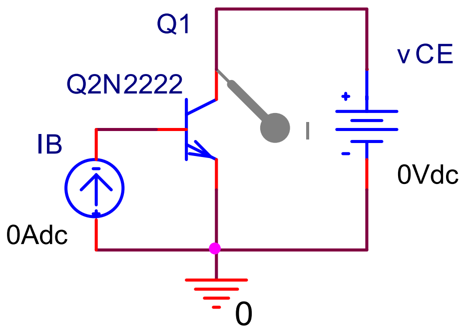


Fig. 2 – PSpice circuit to plot i_C versus v_{CE} for different values of i_B.

to make it carry a convincing amount of forward current. In FA, the i_C versus v_{CE} curves are almost *horizontal*, indicating *current-source* behavior by the CE port there. If we project the FA curves to the left, they all converge to the *same point*, on the v_{CE} axis. This point is located at $-V_{An}$, the Early voltage appearing in Eq. (2).

- For $v_{CE} < V_{CE(\mathrm{EOS})} \cong 0.2$ V, the curves turn almost *vertical*, indicating *voltage-source* behavior by the CE port there. The curves merge together at approximately $v_{CE} = V_{CE(\mathrm{sat})} \cong 0.1$ V, and this region of operation is called the ***saturation region***. The borderline between the FA and the saturation regions is aptly called the *edge of saturation* (EOS).

Regardless of whether a BJT is of the *npn* or *pnp* type, its terminal currents in the *FA region* are related as

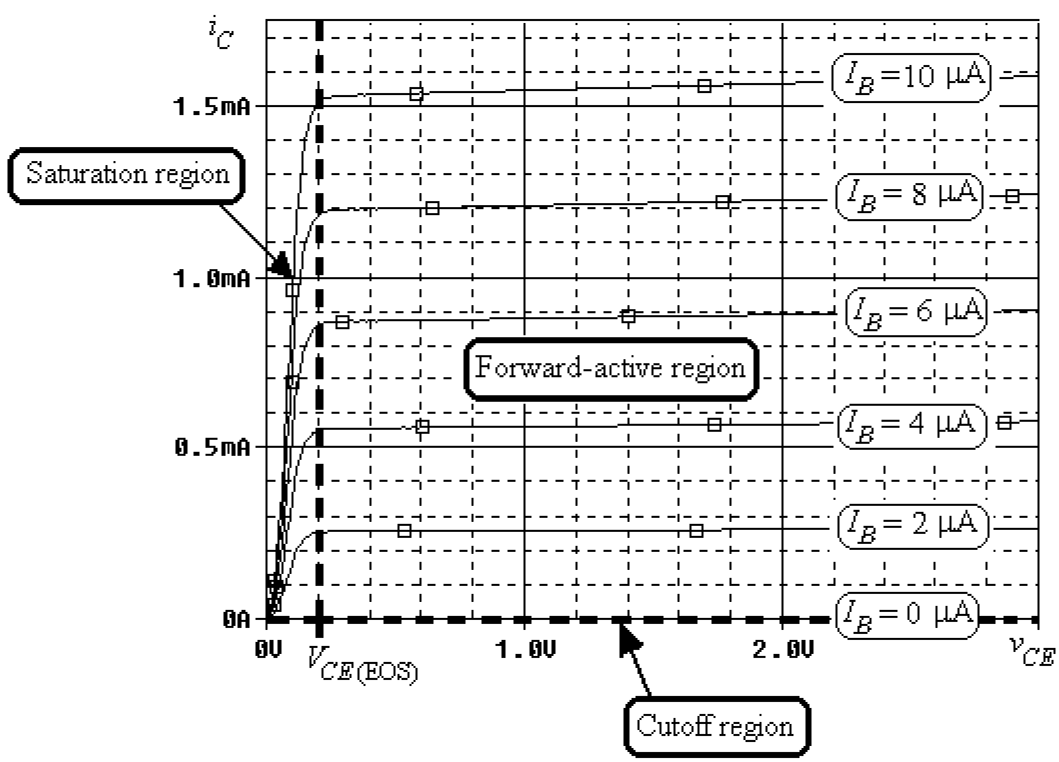


Fig. 3 – Illustrating the *three* regions of operation of an *npn* BJT.

$$i_C = \alpha_F i_E = \beta_F i_B \qquad i_B = \frac{i_C}{\beta_F} = \frac{i_E}{\beta_F + 1} \qquad i_E = \frac{i_C}{\alpha_F} = (\beta_F + 1) i_B \tag{6}$$

where

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \qquad \alpha_F = \frac{\beta_F}{\beta_F + 1} \tag{7}$$

Typically, α_F is very close to unity (such as $\alpha_F \cong 0.99$), and β_F, known as the *forward current gain*, is on the order of 10^2.

BJT Models:

As we know, it is convenient to express a *total signal* such as the collector current i_C as the sum

$$i_C = I_C + i_c \tag{8}$$

where

- I_C is the *DC component*, also known as *large signal*
- i_c is the *AC component*, also known as *small signal*

We work with DC signals when dealing with transistor *biasing*, and we work with AC signals when dealing with *amplification*, where we are interested in finding AC *gain* as well as the *input* and *output resistances*.

- To signify how a BJT relates DC voltages and currents (upper-case symbols with upper-case subscripts) we use *large signal models*
- To signify how a BJT relates AC voltages and currents (lower-case symbols with lower-case subscripts) we use the *small-signal model*.

As far as *large signal models* go, a BJT admits a different model in each region of operation:

- In the *CO region* a BJT draws only leakage currents, which for practical purposes are usually neglected. So, both junctions act essentially as *open circuits*.
- In the *FA region* the BE port acts as a *battery*, namely, $V_{BE(\text{on})} \cong 0.7$ V for the *npn* BJT and $V_{EB(\text{on})} \cong 0.7$ V for the *pnp* BJT, while for both BJTs the CE port acts as a *dependent current source* $I_C = \beta_F I_B$. The two BJT models are shown in Fig. 4.
- In the *saturation region* the CE port too acts as a *battery*, namely, $V_{CE(\text{sat})} \cong 0.1$ V for the *npn* BJT and $V_{EC(\text{sat})} \cong 0.1$ V for the *pnp* BJT, so the two BJT models are as in Fig. 5.

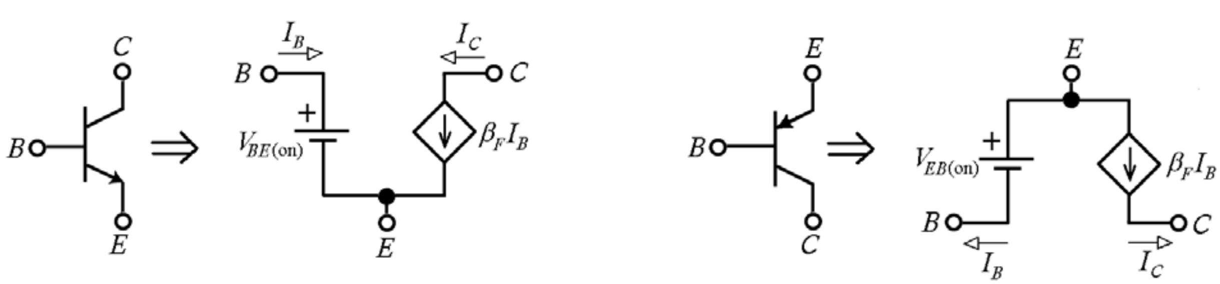


Fig. 4 – *Large-signal* BJT models in *the FA region*.

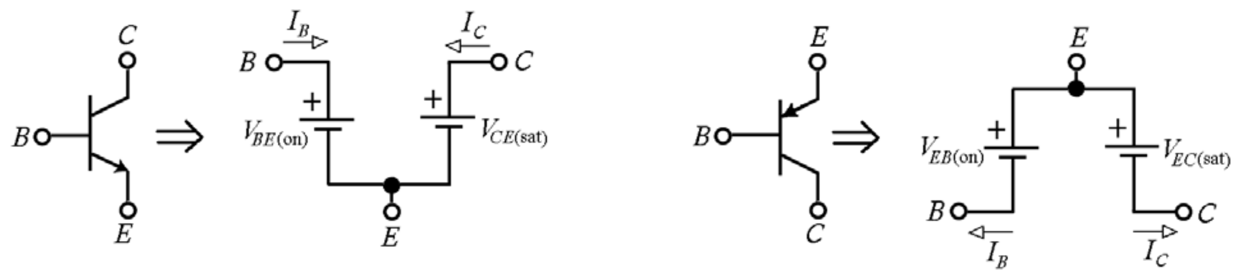


Fig. 5 – *Large-signal* BJT models in the *saturation region*.

To gain additional insight into BJT operation, we use the PSpice circuit of Fig. 6 to sweep the BJT sequentially through each of its three operating regions. The resulting voltage transfer curves (VTCs), shown in Fig. 7, allow us to make the following observations:

- For $v_B < V_{BE(\text{on})}$ the BJT is in cutoff, and $i_C = 0$. Consequently, $v_E = 0$ and $v_C = V_{CC} = 6$ V.
- As v_B approaches $V_{BE(\text{on})}$, the BJT reaches the *edge of conduction* (EOC), and past that it enters the *FA region*, where it becomes fully conductive. Henceforth, we have $v_E = v_B - V_{BE(\text{on})} \cong v_B - 0.7$ V, that is, the emitter will *follow* the base, albeit with an offset of about –0.7 V. Moreover, the circuit yields

$$v_C = V_{CC} - R_C i_C = V_{CC} - R_C \alpha_F i_E \cong V_{CC} - \alpha_F R_C \frac{v_B - V_{BE(\text{on})}}{R_E} \cong \left(V_{CC} + \frac{R_C}{R_E} V_{BE(\text{on})}\right) - \frac{R_C}{R_E} v_B$$

Rewriting as $v_C \cong B + A_v v_B$, with B a suitable constant, we note that in the FA region the BJT *amplifies* v_B with the gain

$$A_v \cong -\frac{R_C}{R_E} \tag{8}$$

or $A_v \cong -(3/1) = -3$ V/V in the example shown. Figure 7 confirms this. Equation (8) forms the basis

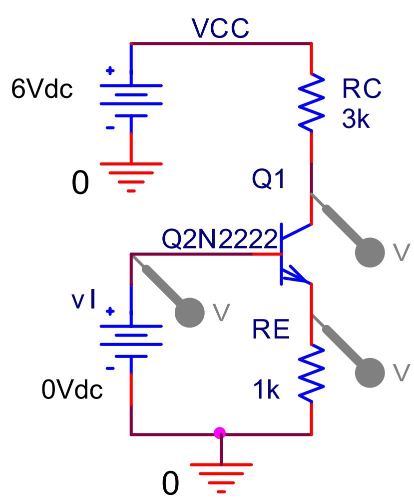


Fig. 6 – PSpice circuit to display the emitter and collector VTCs

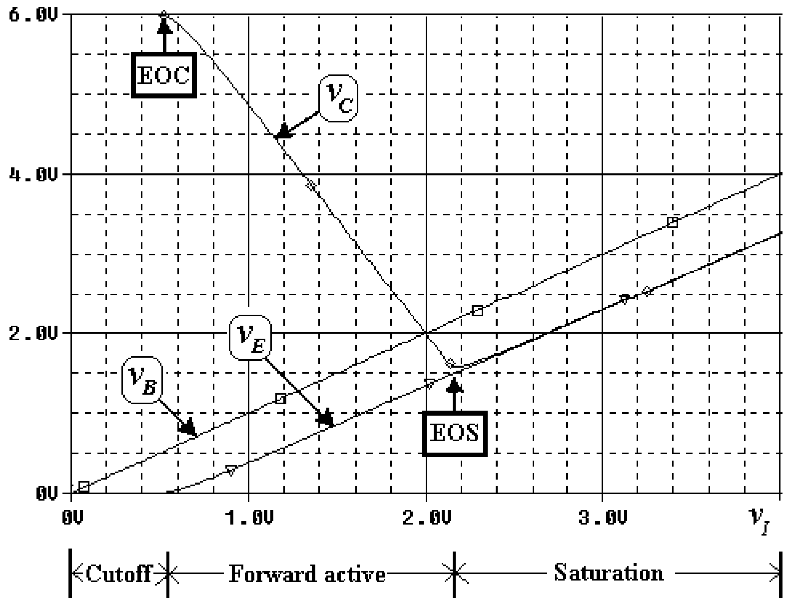


Fig. 7 – Voltage transfer curves for the circuit of Fig. 6.

of the familiar **rule of thumb**: The gain of the circuit of Fig. 6 is approximately equal to the *ratio of the collector resistance* R_C *to the emitter resistance* R_E.

- As the BJT is pushed further into the FA region, v_C continues to drop at the rate of –3 V/V, until it comes within $V_{CE(\text{EOS})}$ ($\cong$ 0.2 V) of v_E. As we know, this point is the *edge of saturation* (EOS).
- Past the EOS, the BJT is in *full saturation*, and v_C is now forced to ride about 0.1 V *above* v_E, which in turn we know to be riding about 0.7 V *below* v_B. Consequently, v_C will now be *rising* with v_B, albeit with an offset of –0.6 V.

When used as an *amplifier*, a BJT is operated in the *FA region* where we illustrate its way of relating voltage and current *variations* via the *small signal model.* Due to its exponential characteristic, the BJT is a highly nonlinear device. However, if we stipulate to keep its *signal variations sufficiently small* (hence the designation *small-signal*), then the model can be kept linear – albeit approximate. For BJTs, the small-signal constraint is

$$v_{be} << 2V_T \cong 52 \text{ mV} \tag{10}$$

While the large-signal models are different for the two BJT types because they have *opposite* voltage polarities and current directions, the small-signal model is the *same* for the two devices because it involves only *variations*. This common model is shown in Fig. 8, where we can consider the dependent source as controlled either by v_{be} or by i_b, depending on which one is more convenient for AC analysis calculations. The parameters appearing in the small-signal model depend on the *bias current* I_C as

$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \beta_0 \frac{V_T}{I_C} \qquad r_o = \frac{V_A}{I_C} \qquad r_\mu = \beta_0 r_o \tag{11}$$

where β_0 is the *small signal current gain*, usually taken to equal β_F. To get a practical feel, we use the typical values $\beta_0 \cong 100$ and $V_A \cong 100$ V to find the at $I_C = 1$ mA a low-power BJT has typically

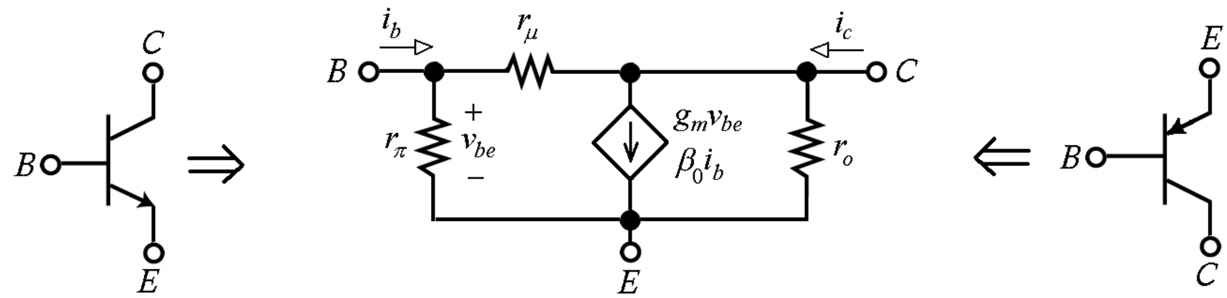


Fig. 8 – *Small-signal* BJT model (valid for $v_{be} << 2V_T \cong 52$ mV).

$g_m = \dfrac{1}{26\ \Omega}$ $\qquad r_\pi \cong 2.6$ kΩ $\qquad r_o \cong 100$ kΩ $\qquad r_\mu \cong 10$ MΩ

As we move from *E*, to *B*, to *C*, the resistance levels change from *small*, to *medium*, to *large*. Moreover, r_μ is so large that except for a few particular cases, it is generally ignored.

Figure 9 shows the *AC equivalent* of a generalized BJT circuit, whose properties are worth listing because they simplify the AC analysis of a variety of BJT amplifiers. Ignoring r_μ, we have:

- The resistance seen looking into ***the base*** is

$$R_b = r_\pi + (\beta_0 + 1)R_E \tag{12}$$

indicating that the emitter resistance R_E, when reflected to the base, gets *multiplied* by $(\beta_0 + 1)$. If $R_E = 0$, then $R_b = r_\pi$.

- The resistance seen looking into the ***emitter*** is

$$R_e = r_e + \frac{R_S}{\beta_0 + 1} \tag{13}$$

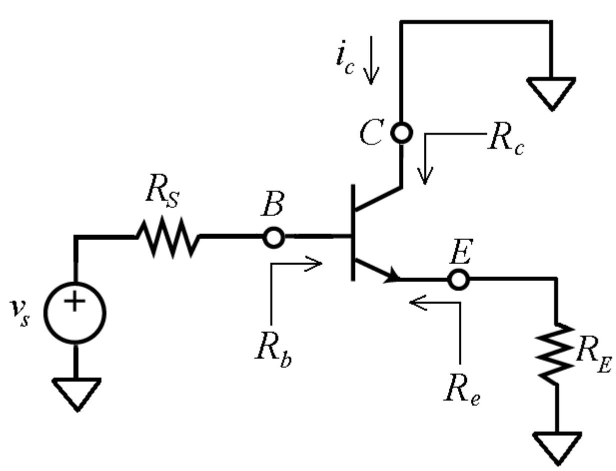


Fig. 9 – A generalized AC equivalent.

where $r_e = \alpha_F/g_m \cong 1/g_m$ is the resistance seen looking into the emitter in the limit $R_S \to 0$. As we know, at $I_C = 1$ mA we have $r_e = 26\ \Omega$. Equation (13) indicates that the base resistance R_S, when reflected to the emitter, gets *divided* by $(\beta_0 + 1)$. Comparing Eqs. (12) and (13), we see that the resistance transformation by the BJT works both ways in reciprocal fashion, as in the case of the familiar transformer. In fact, the word *transistor* was coined to signify <u>trans</u>formation of a re<u>sistor</u>!

- The resistance seen looking into the ***collector*** is

$$R_c \cong r_o\left(1+\frac{g_m R_E}{1+(R_S+R_E)/r_\pi}\right) \tag{14a}$$

indicating that the presence of R_E effectively *raises* the collector resistance from r_o to the value of Eq. (14*a*). It often occurs that $(R_S + R_E) << r_\pi$, in which case we have

$$R_c \cong r_o(1 + g_m R_E) \tag{14b}$$

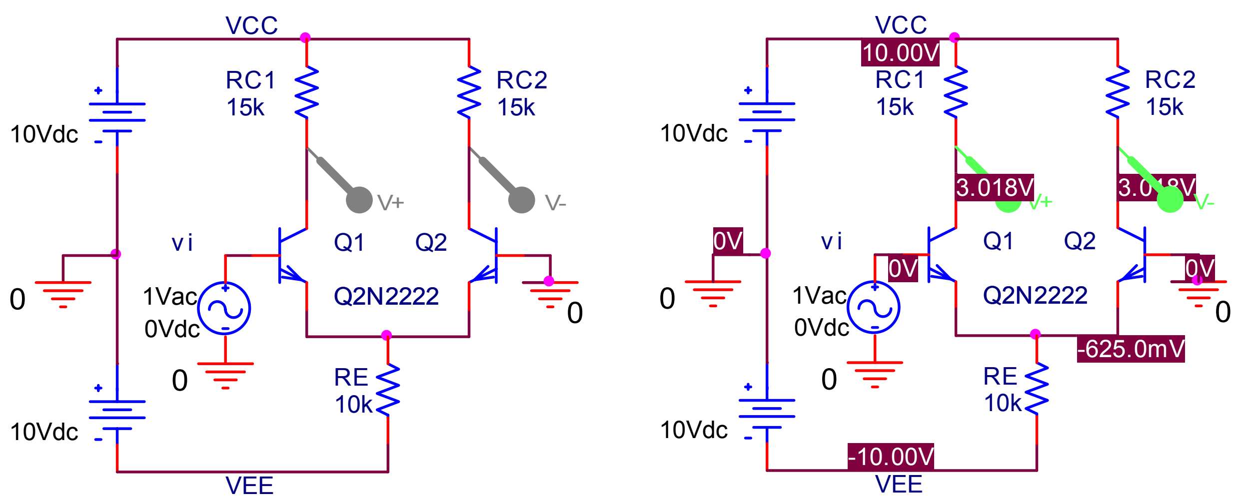
In the special cases in which R_c becomes comparable with r_μ, the latter can no longer be ignored, and the actual output resistance seen looking into the collector must be corrected as $R_{c(\text{actual})} = R_c // r_\mu$, with R_c as given in Eq. (14).

- The collector current change i_c stemming from a small-signal base voltage change v_b is expressed as $i_c = G_m v_b$, where

$$G_m = \frac{g_m}{1+g_m R_E} \tag{15}$$

It is apparent that $G_m < g_m$, indicating that the presence of R_E *reduces* the BJT's transconductance. This loss is referred to as *degeneration*, and R_E is said to introduce *emitter degeneration*. In the limit $g_m R_E >> 1$, we get $g_m = 1/R_E$, that is, the transconductance no longer depends on the BJT, but is set *externally* by R_E. This offers important advantages, as we'll see as we move along.

We conclude by illustrating the PSpice simulation of an *emitter-coupled pair* of 2N2222 BJTs.



(*a*) (*b*)

Fig. 10 – (*a*) PSpice emitter-coupled amplifier and (*b*) its DC bias voltages

The circuit is shown in Fig. 10*a*. After directing PSpice to perform the *Bias Point Analysis*, we obtain the labeled schematic of Fig. 10*b*. Moreover, after directing PSpice to perform a one-point *AC analysis* at f = 10 kHz, we find that the *small-signal gain* of the circuit is $A_v \cong -247$ V/V. You will find it instructive to confirm the above data (both DC and AC) via hand calculations! You can also duplicate all PSpice examples of this lab on your own by downloading their appropriate files from the Web. To this end, go to http://online.sfsu.edu/~sfranco/CoursesAndLabs/Labs/445Labs.html, and once there, click on **PSpice Examples**. Then, follow the instructions contained in the **Readme** file.

PART II – EXPERIMENTAL PART

This experiment is based on the LM3046 integrated circuit (IC), an array of five general-purpose matched *npn* BJTs fabricated on the same substrate. As shown in Fig. 11, Q_1 and Q_2 are internally connected as a differential pair, and the substrate is internally connected to pin 13, also the emitter of Q_5. To avoid inadvertently turning on the parasitic diodes between the common substrate and the collectors of the BJTs, we must ensure that pin 13 is always at the *most negative voltage* (MNV) in the IC itself. The LM3046 is a delicate device, so to avoid damaging it, make sure you always turn power off before making any circuit changes, and that before reapplying power each lab partner checks separately that the circuit has been wired correctly. Also, refer to the Appendix for useful tips on how to wire proto-board circuits.
You are also urged to compare the data taken on your *particular* IC sample with those reported in the data sheets, which are *typical*. The latter can readily be downloaded from the Web (for instance, by visiting http://www.google.com and searching for LM3046 or variants thereof.)

Henceforth, steps shall be identified by letters as follows: **C** for calculations, **M** for measurements, **P** for Prelab, and **S** for SPICE simulations.

Characterization of Monolithic BJTs:

In the first part of our experiment we shall characterize the BJTs of our array, observe the parameter distribution among the various samples, and draw conclusions about the degree of matching

MC1: Mark one of the 3046 ICs (the other is a spare), and assemble the circuit of Fig. 12 with power off (keep leads short, and bypass the power-supply to ground via a 0.1-µF capacitor, as recommended in the Appendix.) Then, while monitoring I_C with the *digital current meter* (DCM), apply power and adjust the potentiometer until I_C = 0.5 mA. This biases BJT Q_1 at the operating point $Q(I_C, V_{CE})$ = (0.5 mA, 5 V), as shown in Fig. 13. Next, short out R_C with a wire (that is, close *SW*) so as to effect the change ΔV_{CE} = 5 V

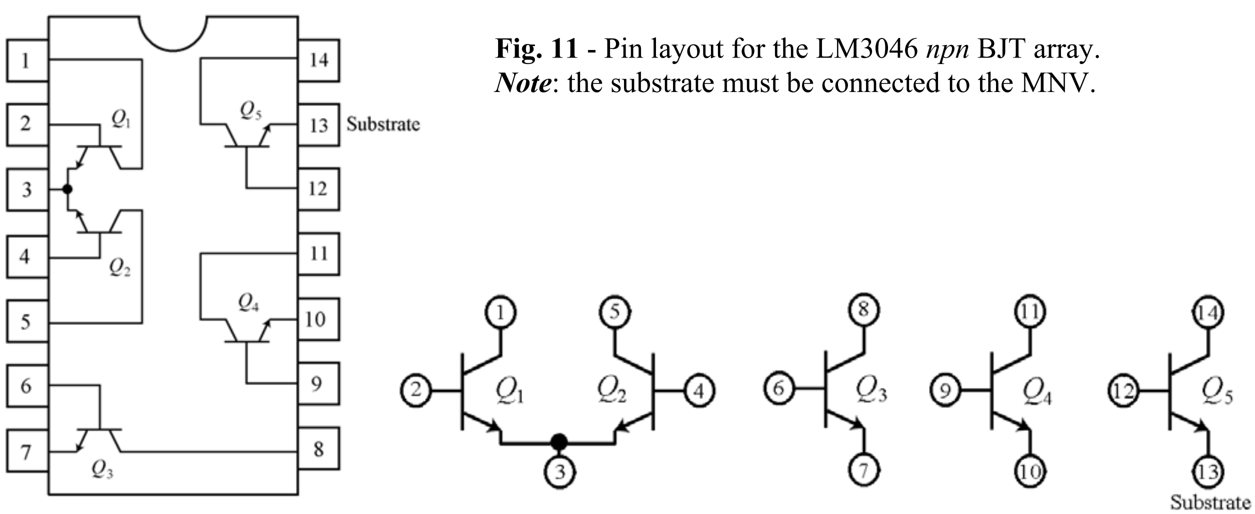


Fig. 11 - Pin layout for the LM3046 *npn* BJT array.
Note: the substrate must be connected to the MNV.

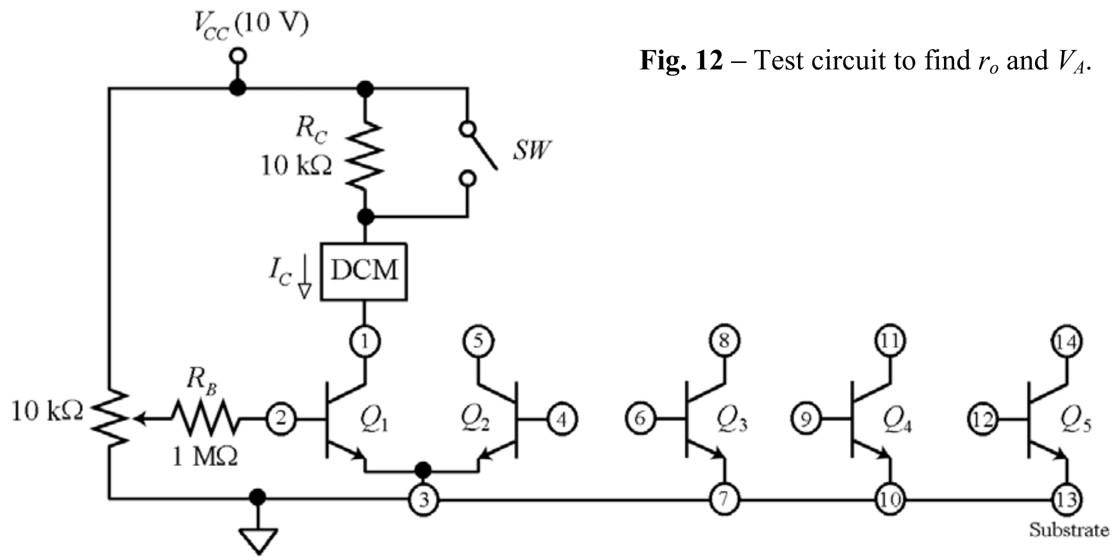


Fig. 12 – Test circuit to find r_o and V_A.

and thus move the operating point from Q to Q' (see again Fig. 13). Record the corresponding change ΔI_C (this change is small, so use as many digits as your instrument will allow). Finally, compute

$$r_o = \Delta V_{CE}/\Delta I_C \qquad (16a)$$

$$V_A = r_o I_C - V_{CE} \qquad (16b)$$

where $I_C = 0.5$ mA and $V_{CE} = 5$ V. As usual, express your results in the form $X \pm \Delta X$ (e.g. $V_A = 90 \pm 5$ V), where ΔX represents the estimated uncertainty of your measurement.

MC2: Repeat Step MC1, but for *each* of the remaining BJTs, *one at a time* (don't forget to turn power off as you move R_B and the DCM from one BJT to the next!). Record all five V_A values for later analysis.

MC3: Assemble the circuit of Fig. 14*a*, and adjust V_{CC} for $I_C = 1.0$ mA, starting out with $V_{CC} \cong 10.7$ V, as

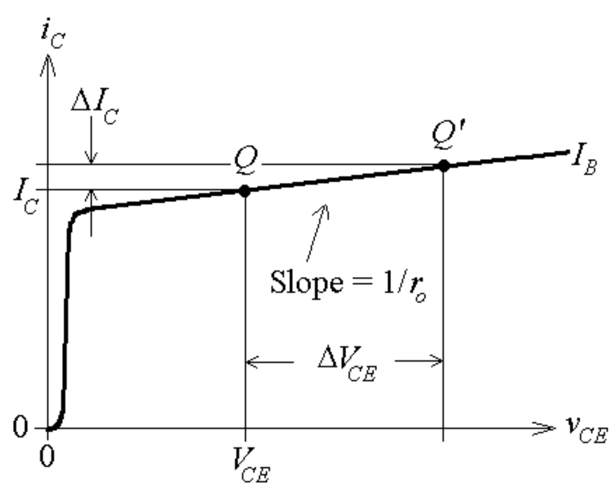


Fig. 13 – Graphical determination of r_o.

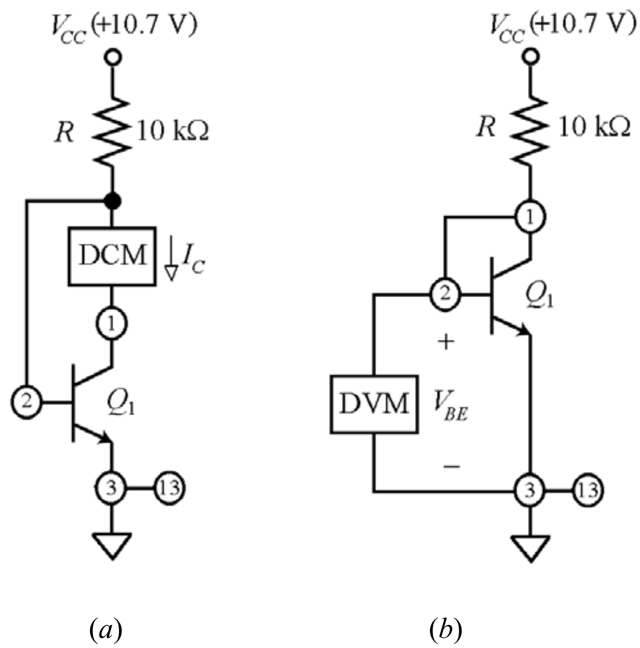


Fig. 14 – Test circuits to (*a*) set I_C, and (*b*) to measure V_{BE}.

shown (once this adjustment has been made, V_{CC} should not be changed till further notice.) Next, turn power off, insert the DCM in series with the base as in Fig. 15, reapply power, measure I_B, and calculate

$$\beta_F = \frac{I_C}{I_B} \tag{17}$$

where I_C = 1.0 mA. As usual, express your result in the form $X \pm \Delta X$ (e.g. $\beta_F = 97 \pm 1$).

MC4: Using the same R and V_{CC} settings of Step MC3, measure I_B for *each* of the remaining BJTs, *one*

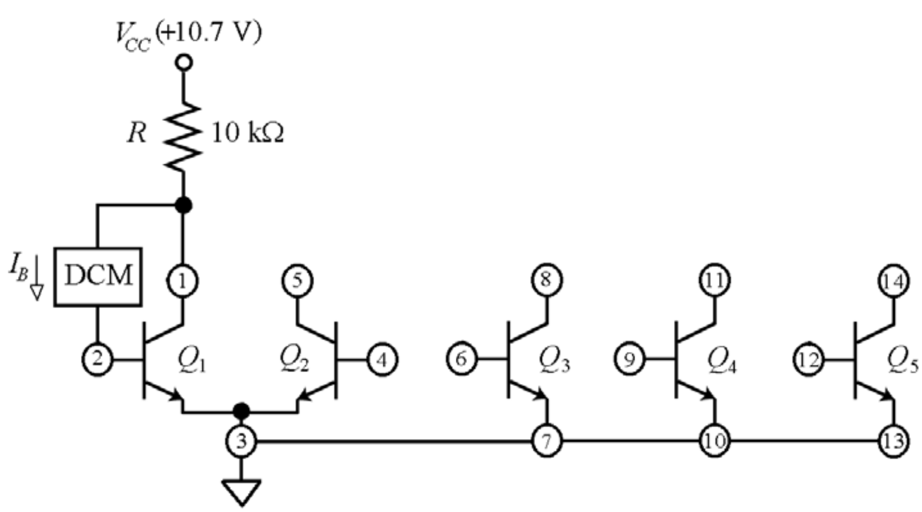


Fig. 15 – Test circuit to measure the individual-BJT *base currents*.

at a time (don't forget to turn power off as you move R and the DCM from one BJT to the next!), and find β_F. Record all five β_F values for later analysis.

Note: Since the V_{BE}s of the BJTs are matched, the 1.0-mA value set for I_C in Step MC3 will vary negligibly as we move R from Q_1 to each of the remaining BJTs, so there is no point readjusting it.

M5: Returning to Q_1, connect it now as in Fig. 14*b* with power off. Next, apply power (you should still have I_C = 1.0 mA!), and measure and record Q_1's base-emitter voltage drop V_{BE1}(1 mA).

M6: Turn power off and reconnect Q_1 as in Fig. 14*a*, but now with R = 100 kΩ. Apply power and adjust V_{CC} for I_C = 0.1 mA. Then, with power off reconnect Q_1 as in Fig. 14*b*, reapply power, and measure and record its new base-emitter voltage drop V_{BE1}(0.1 mA).

C7: We can now write two equations in the unknowns I_{s1} and V_T,

$$1.0 \text{ mA} = I_{s1} e^{V_{BE1}(1 \text{ mA})/V_T} \left(1 + \frac{V_{BE1}(1 \text{ mA})}{V_{A1}} \right) \tag{18a}$$

$$0.1 \text{ mA} = I_{s1} e^{V_{BE1}(0.1 \text{ mA})/V_T} \left(1 + \frac{V_{BE1}(0.1 \text{ mA})}{V_{A1}} \right) \tag{18b}$$

where V_{A1} is the Early voltage found in Step MC1, V_{BE1}(1.0 mA) is the voltage drop measured in Step M5, and V_{BE1}(0.1 mA) that measured in Step M6. Thus, substitute the given data and solve the two equations to obtain the experimental values of I_{s1} and V_T. Are they typical?

Offset Voltages:

Let us define the *offset voltage* of Q_2 with respect to Q_1 as $V_{OS21} = V_{BE2} - V_{BE1}$. If the two BJTs are biased at the *same operating points*, this offset is $V_{OS21} = V_T \ln (I_{s1}/I_{s2})$. Conversely, given that we already know I_{s1}, we can find I_{s2} as

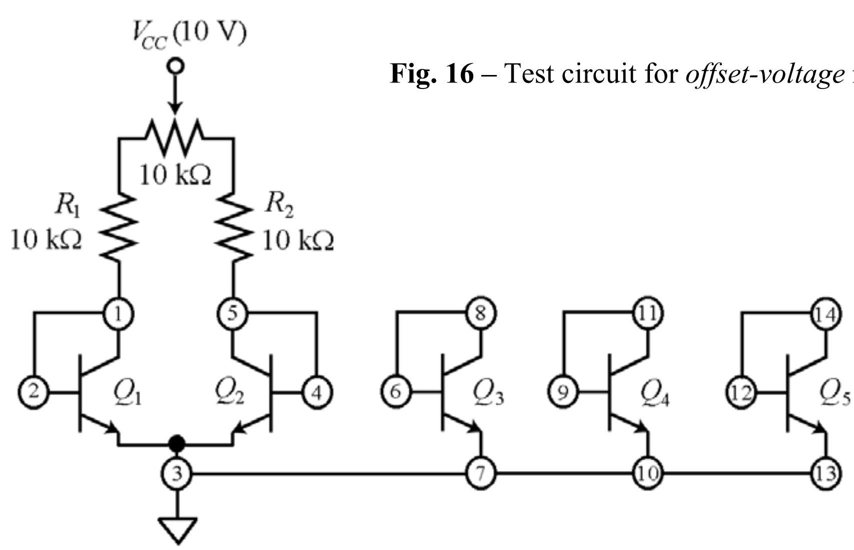


Fig. 16 – Test circuit for *offset-voltage* measurements.

$$I_{s2} = \frac{I_{s1}}{\exp(V_{OS21}/V_T)} \tag{19}$$

By similar reasoning, we find the saturation currents of the remaining BJTs as $I_{s3} = I_{s1}/\exp(V_{OS31}/V_T)$, $I_{s4} = I_{s1}/\exp(V_{OS41}/V_T)$, and $I_{s5} = I_{s1}/\exp(V_{OS51}/V_T)$.

To ensure *identical* collector currents, we connect two 10-kΩ resistors and a 10-kΩ potentiometer in the manner of Fig. 16, and adjust the wiper so as to ensure *equal* resistances (nominally 15 kΩ) from the wiper to the bottom terminals of R_1 and R_2 (make this adjustment with the ohmmeter *before* actually inserting the resistances in your circuit!).

MC8: After the resistance adjustment just described, assemble the circuit of Fig. 16 with power off. Next, apply power and find V_{OS21} as the voltage difference between Pin #4 and Pin #2, and find I_{S2} via Eq. (19).

MC9: Without altering the wiper's setting, repeat Step MC8, but for Q_3, Q_4, and Q_5. For instance, to find V_{OS31}, move R_2 from Pin #5 to Pin #8, measure the voltage difference between Pin #6 and Pin #2, and adapt Eq. (19) to the calculation of I_{s3}. Make sure you make your circuit changes with power off!

C10: Prepare a table with the values of β_F, V_A, and I_s for the five BJTs, and calculate their *mean values* as well as their *standard deviations*. Do likewise for the four offset voltages. Comment on your results.

Advantages of Matching in IC Design:

In the rest of this experiment we shall investigate the advantages of matched components in IC design. To this end, consider first the familiar *CE amplifier* of Fig. 17*a*, whose unloaded gain we know to be $A_v \cong -g_m R_C$. Its most serious drawback is the need for a large capacitor C_E to ensure a low impedance from emitter to ground. A large capacitor cannot be fabricated in IC form. Moreover, the capacitor acts as a short only for ac signals above a certain frequency. As we approach DC, it becomes an open, making

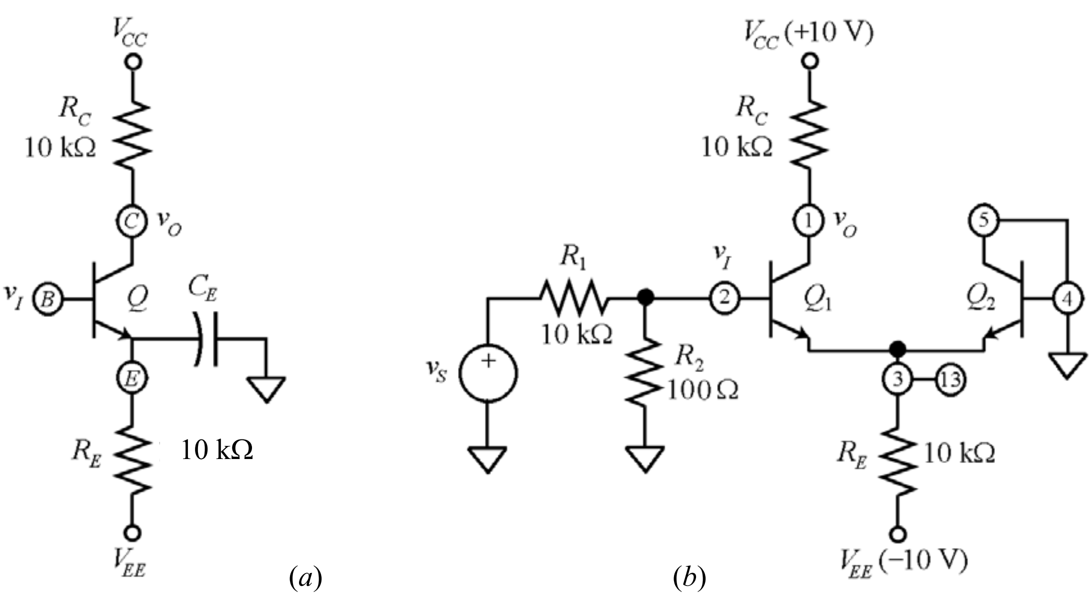


Fig. 17 – Comparing discrete and integrated design.

the transconductance *degenerative* and causing the gain to drop to $A_v \cong -[g_m/(1 + g_m R_E)]R_C \cong -R_C/R_E$.

The above drawbacks are ingeniously eliminated by replacing the capacitor with a matched BJT connected as a diode, as in Fig. 17*b*. This diode occupies far less space than a capacitor, provides low impedance all the way down to dc, and its own voltage drop V_{BE2} tracks any temperature variations in V_{BE1} to ensure a stable operating point for Q_1, and, hence, a stable gain.

C11: Using the results of previous measurements and assuming $V_S = 0$ V in the circuit of Fig. 17*b*, estimate the small-signal gain $A_v = v_o/v_i$ as well as the output DC component V_O. For signal notation, refer to Eq. (8).

M12: With power off, assemble the circuit of Fig. 17*b*, keeping leads short and bypassing both supplies with 0.1-μF capacitors. Then apply power, and while monitoring v_S with Ch.1 of the oscilloscope set on DC, adjust the waveform generator so that v_S is a 1-kHz sine wave with a peak-to-peak amplitude of 1 V and 0-V DC offset. This will result in a 10-mV peak-to-peak amplitude for v_i, small enough to guarantee the validity of the small-signal BJT models, as per Eq. (10).

Next, observe the output with Ch.2 of the oscilloscope set on AC, and measure the peak-to-peak value of v_o. What is the value of the gain $A_v = v_o/v_i$? How does it compare with that predicted in Step C11? Finally, switch Ch. 2 of the oscilloscope to DC, record the output DC offset V_O, compare it with that predicted in Step C11, and justify any differences.

The Differential Pair:

Transistor Q_2 in Fig. 17*b* is actually underutilized. Turning it into a full-fledged amplifier as in Fig. 18 doubles the overall gain and also makes the circuit symmetric in the sense that we now have balanced inputs and balanced outputs. Moreover, with perfect component matching, the output offset is now 0 V. The result is the familiar *differential pair*, also called *long-tail pair*, whose *differential-mode gain* is

$$A_{dm} = \frac{v_{od}}{v_{id}} = -g_m (r_o \,//\, R_C) \qquad (20)$$

where $v_{id} = v_{i1} - v_{i2}$, $v_{od} = v_{o1} - v_{o2}$, $g_m = g_{m1} = g_{m2}$, $r_o = r_{o1} = r_{o2}$, and $R_C = R_{C1} = R_{C2}$.

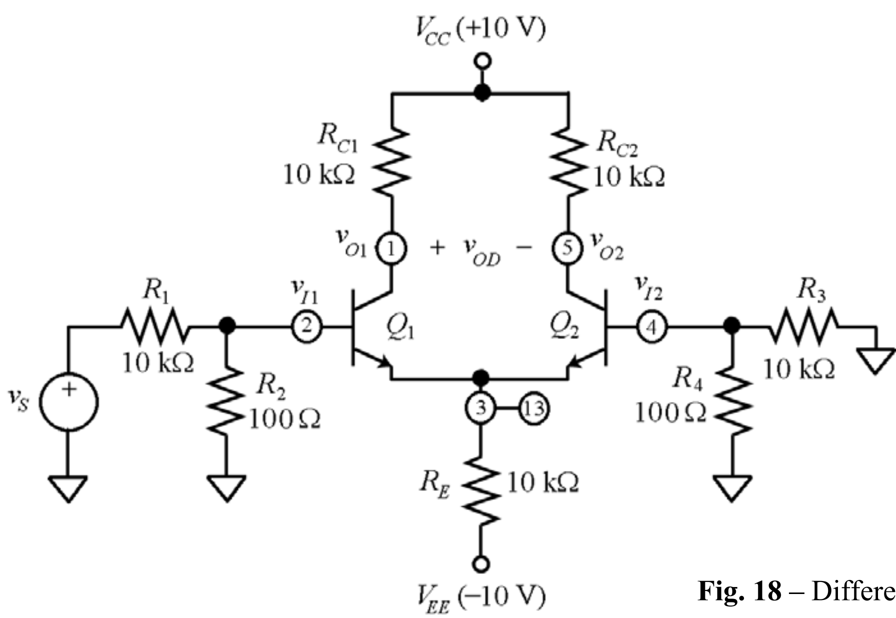


Fig. 18 – Differential pair

M13: With power off, assemble the circuit of Fig. 18. Next, apply power, and with v_S still set as in Step M12, observe v_{O1} and v_{O2} with Ch.1 and Ch. 2 of the oscilloscope, both set first on DC, and then on AC. How do the two signals compare with each other? What happens if you ground the left terminal of R_1, lift the right terminal of R_3 off ground, and apply v_S there?

Finally, configure your oscilloscope so that now it displays the *difference* $v_{od} = v_{o1} - v_{o2}$. Measure its peak-to-peak amplitude, and use it to find $A_{dm} = v_{od}/v_{id}$. How does it compare with the value predicted by Eq. (20)? Justify any possible differences.

S14: Simulate the circuit of Fig. 18 via PSpice (DC as well as AC analysis). Compare the gain found via simulation with that found via measurement, and justify any possible differences.

Remark: For a realistic simulation, you need to create a PSpice model for your LM3046 BJTs. To this end, click the BJT in your PSpice schematic to select it, and then click **Edit → PSpice Model** to set its parameter values to those found experimentally. In our simplified characterization, we specify only the values of I_s, β_F, and V_A,, so the model statement will look like

```
.model Q3046    NPN(Is=* Bf=* Vaf=*)
```

where the asterisks indicate the mean values found above experimentally, such as: `(Is=2.5fA Bf=110 Vaf=80)`

M15: We now wish to visualize the *voltage transfer curve* (VTC) of our circuit. With power off, remove R_2 and R_4 from the circuit of Fig. 18, and while monitoring v_S with Ch.1 of the oscilloscope set on DC, adjust it for a 100-Hz *triangle wave* with 0-V DC offset and a peak-to-peak amplitude a bit over 1 V. Next, observe v_{O1} with Ch.2 of the oscilloscope set on DC, and justify the large amount of distortion observed.

Now switch the oscilloscope to the X-Y mode, and observe and record the VTC for v_{O1}. Then, repeat for v_{O2}. Identify the portions of the two VTCs over which the circuit would behave fairly linearly, yielding reasonably low distortion. What is the corresponding voltage range for the input?

S16: Use PSpice to display the *differential VTC* of the circuit of Fig. 18, that is, the plot of the *output difference* $v_{OD} = v_{O1} - v_{O2}$ versus the *input difference* $v_{ID} = v_{I1} - v_{I2}$. Comment on your findings.

Effect of Mismatches on the Differential Pair:

We are now going to investigate the effect of component mismatches upon the performance of the differential pair.

MC17: With power off, assemble the circuit of Fig. 19, but without connecting R_3 yet. Apply power, measure the *output offset error* E_O with the DVM, and find the input offset voltage of your circuit as $V_{OS} = E_O/A_{dm}$, where A_{dm} is the differential-mode gain measured in Step M13. Hence, justify the output offset error quantitatively in terms of the *input offset* measurement of Step MC8, as well as any mismatch between R_{C1} and R_{C2} (to measure these resistors and thus find their mismatch, pull them out of the circuit!)

M18: Turn again power off, insert R_3, reapply power, and while monitoring E_O with the DVM, vary the potentiometer's wiper until you drive E_O to zero. This shows one of several possible ways of *nulling* the overall output offset error!

MC19: Turn power off and (without changing the wiper's setting!) insert R_{B1} and R_{B2} as shown in Fig. 20. The purpose of these resistors is to sense the base current I_{B1} and I_{B2} and produce an additional input offset error. Reapply power, measure the new value of E_O, and find the *input offset current* I_{OS} of your

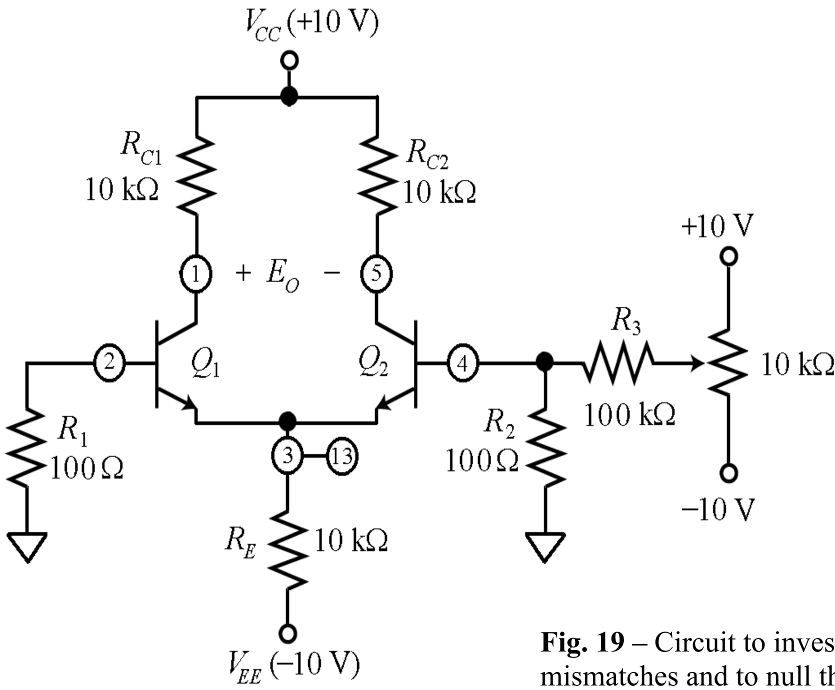


Fig. 19 – Circuit to investigate the effect of component mismatches and to null the output offset error E_O.

differential pair from $R_B I_{OS} = -E_O/A_{dm}$, where $R_B = R_{B1} = R_{B2}$, and $I_{OS} = I_{B2} - I_{B1}$. Hence, justify I_{OS} quantitatively in terms of the mismatch between β_{F1} and β_{F2} found in Step MC4.

M20: Vary the potentiometer's wiper until you drive E_O again to zero. You have now compensated for the error due to cumulative effect of mismatches between V_{BE1} and V_{BE2}, $R_{C1}$and R_{C2}, and $\beta_{F1}$and β_{F2}.

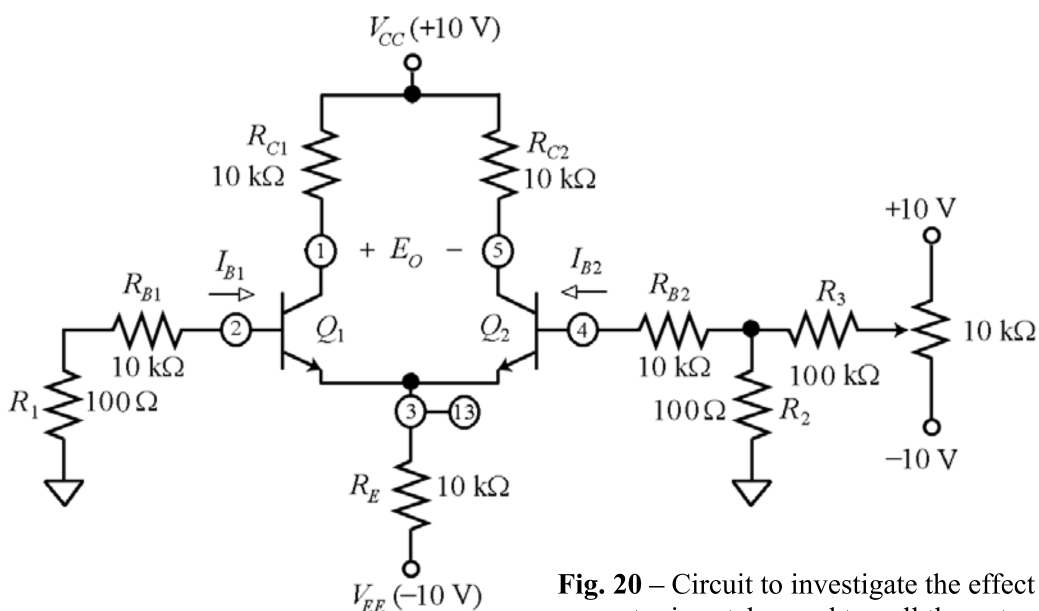


Fig. 20 – Circuit to investigate the effect of input current mismatches and to null the output offset error..