

LAB #2: OPERATIONAL AMPLIFIER CHARACTERISTICS

Updated March 15, 2004

Objective:

To measure the most common parameters of a 741 op amp: The input *bias* and *offset currents* I_B and I_{OS} , the *input offset voltage* V_{OS} , the *power-supply* and *common-mode rejection ratios* $PSRR$ and $CMRR$, the *output saturation limits* V_{OH} and V_{OL} , the *output short-circuit current* I_{SC} , the *open-loop dc gain* A_{OL0} , the *gain-bandwidth product* GBP , the *small-signal rise time* t_R , and the *slew rate* SR . To assess the faithfulness of the 741 *macro-model* available in the PSpice library.

Components:

1 × 741C op amp, 1 × 10-kΩ potentiometer, 1 × 100-kΩ potentiometer, 2 × 0.1-μF capacitors, and resistors: 2 × 100 Ω, 1 × 2 kΩ, 3 × 10.0 kΩ, 2 × 100 kΩ, and 2 × 1.0 MΩ (all 5%, ¼ W).

Instrumentation:

A dual ±15-V regulated variable power supply, a 5-V fixed dc source, a waveform generator (sinewave and square-wave), a high-sensitivity (10 -μV or better) digital multi-meter, and a dual-trace oscilloscope.

PART I – THEORETICAL BACKGROUND

Ideally, an op amp has (a) *infinite open-loop gain regardless of frequency*, it draws (b) *zero currents* at its input pins, and it can provide (c) *any voltage or current* at its output pin.

In a practical op amp, the open loop gain is not only *finite*, but it *rolls off with frequency*. Moreover, the input pins draw tiny currents I_P and I_N , where labels P and N denote, respectively, the *non-inverting* and the *inverting* input pins. Also, if we tie the input pins together so that $v_N = v_P$, the output v_O will not be zero due to mismatches in the internal circuits processing v_P and v_N ; if we wish to drive it to zero, a tiny corrective voltage must be applied between the input pins, called the *input offset voltage* V_{OS} . Finally, a practical op amp can only swing v_O within a limited range, $V_{OL} \leq v_O \leq V_{OH}$, where V_{OL} and V_{OH} are the lower and upper *output saturation limits*. Similarly, it can supply an output current i_O of no more than a specified value called the *output short-circuit current* I_{SC} .

The most popular op amp is the μA741, developed by Fairchild in the late nineteen-sixties and since then available from virtually any analog IC manufacturer. You can download the 741 data sheets from the website of any analog IC manufacturer, or you can perform your own search using, for instance, <http://www.google.com> and searching for “741 operational amplifier” or variants thereof.

The quantities I_P , I_N , and V_{OS} are referred to as *dc imperfections*. The mean of I_P and I_N is called the *input bias current* I_B , and their difference the *input offset current* I_{OS} ,

$$I_B = \frac{I_P + I_N}{2} \qquad I_{OS} = I_P - I_N \qquad (1)$$

The data sheets of the 741C version give the following typical (maximum) room-temperature values: $I_B = 80$ nA (500 nA), $I_{OS} = 20$ nA (200 nA), $V_{OS} = 2.0$ mV (6.0 mV). Note that I_{OS} and V_{OS} may be positive or negative, depending on the direction of mismatch between the internal circuits processing each input.

The input offset voltage V_{OS} varies, with *temperature* (for a general-purpose op amp, the thermal

drift is typically $\partial V_{OS} / \partial T \cong 5 \mu\text{V}/^\circ\text{C}$), as well as with the *power supply* and the *common-mode input voltage*. Denoting the supply voltages as $\pm V_S$, we define the *power-supply rejection ratio (PSRR)* as

$$\frac{1}{PSRR} = \left| \frac{\partial V_{OS}}{\partial V_S} \right| \quad (2)$$

For instance, if it is found that V_{OS} changes by $50 \mu\text{V}$ for every 1-V change in V_S , then we have $1/PSRR = 50 \times 10^{-6} / 1$, or $PSRR = 2 \times 10^4$. This is also expressed in decibels as $PSRR_{\text{dB}} = 20 \log_{10} (2 \times 10^4) = 86$ dB. Similar considerations hold for the *common-mode rejection ratio (CMRR)*, defined as

$$\frac{1}{CMRR} = \left| \frac{\partial V_{OS}}{\partial v_{CM}} \right| \quad (3)$$

where v_{CM} is the *common-mode input voltage* to the op amp, in turn defined as

$$v_{CM} = \frac{v_P + v_N}{2} \quad (4)$$

Since we know that when operated in the negative-feedback mode the op amp yields $v_N \rightarrow v_P$, we can approximate $v_{CM} \cong v_P$. The 741C data sheets give the following typical as well as worst-case values: $PSRR = 15 \mu\text{V}/\text{V}$ ($50 \mu\text{V}/\text{V}$), and $CMRR = 95$ dB (80 dB). Ideally, we'd want $PSRR = CMRR = \infty$.

With $\pm V_S = 15$ V, the 741C data sheets report $I_{SC} \cong 25$ mA. Moreover, with a typical output load of 2 k Ω , they give $V_{OH} \cong +13$ V and $V_{OL} \cong -13$ V.

At low frequencies the open-loop gain A_{OL} , though not infinite, is still fairly large. This gain is aptly called the *DC gain* and is denoted as A_{OL0} . For the 741C op amp, $A_{OL0} = 200,000$ V/V typical ($50,000$ V/V minimum). An op amp provides a high gain only up to some frequency called the *open-loop gain bandwidth* f_b , after which gain rolls with frequency until a frequency f_t is reached, at which gain becomes unity, or 0 dB. Above f_t gain is less than unity; hence, f_t is called the *transition frequency*. The 741C op amp typically has $f_b \cong 5$ Hz and $f_t \cong 1$ MHz. For most op amps, including the 741 type, *gain rolls off at a constant rate* of -20 dB/dec, indicating that we can express the open-loop gain $A_{OL}(jf)$ mathematically as

$$A_{OL}(jf) = \frac{A_{OL0}}{1 + jf / f_b} \quad (5)$$

For the 741C op amp, $A_{OL}(jf) = (2 \times 10^5 \text{ V/V}) / [1 + jf / (5 \text{ Hz})]$. The *gain-bandwidth product* is defined as $GBP = |A_{OL}| \times f$. For an op amp with a gain rolloff of -20 dB/dec, this product is constant for $f \gg f_b$,

$$GBP = A_{OL0} \times f_b = f_t \quad (6)$$

The **frequency response** of an op amp is readily visualized via PSpice using suitable op amp models called *macro-models*. The PSpice circuit of Fig. 1 is used to display both the *open-loop gain* of the basic op amp and the *closed-loop gain* of the non-inverting amplifier configuration, which is obtained by applying negative feedback around the basic op amp via R_1 and R_2 . An important parameter arising in negative feedback applications is the *feedback factor* β , representing the *portion* of v_O being fed back to the *inverting input* as v_N , or $\beta = v_N / v_O$. Using the voltage divider formula,

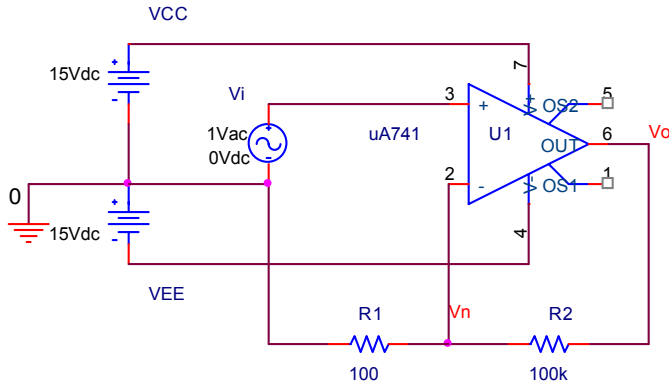


Fig. 1 – PSpice circuit to plot the open and closed loop gains.

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{1}{1 + R_2/R_1} \quad (7)$$

Figure 2 indicates a closed-loop gain of the type

$$A_{CL}(jf) = \frac{A_{CL0}}{1 + jf/f_B} \quad (8)$$

where A_{CL0} and f_B are the *closed-loop dc gain* and the *closed-loop bandwidth*, respectively. We have

$$A_{CL0} = \frac{1}{\beta} = 1 + \frac{R_2}{R_1} \quad (9a)$$

and

$$f_B = \beta f_t = \frac{f_t}{1 + R_2/R_1} \quad (9b)$$

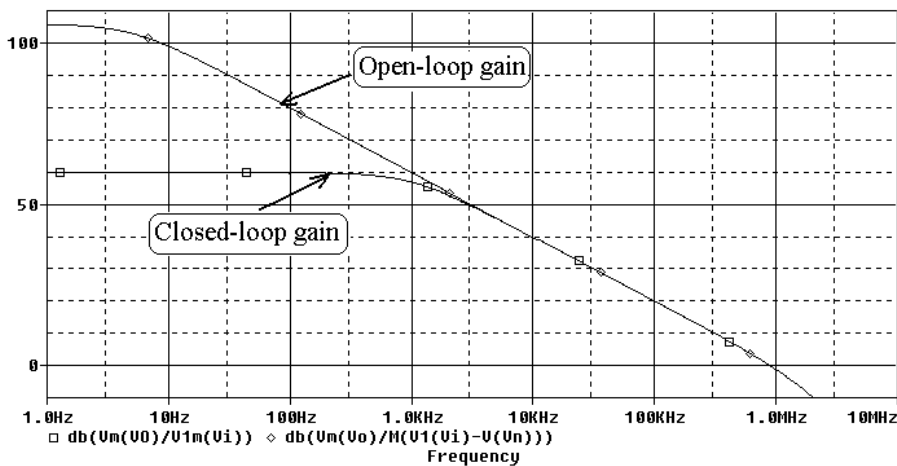


Fig. 2 – Gain plots for the circuit of Fig. 1.

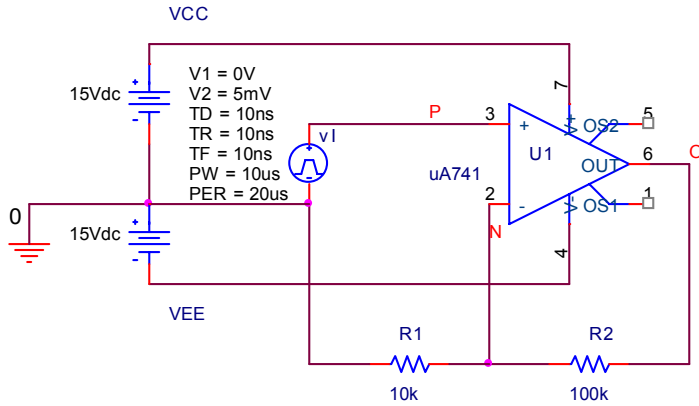


Fig. 3 – PSpice circuit to plot the *small-signal transient response*.

In our example, $A_{CL0} \cong 10^3 \text{ V/V} = 60 \text{ dB}$, and $f_B \cong 1 \text{ kHz}$. We also note that for $f \gg f_B$ the *GBP* is again constant and it is the same as in the open-loop case, namely, $GBP = f_i = 1 \text{ MHz}$.

You can simulate this circuit on your own by downloading its appropriate files from the Web. To this end, go to <http://online.sfsu.edu/~sfranco/CoursesAndLabs/Labs/301Labs.html>, and once there, click on **PSpice Examples** and follow the instructions contained in the **Readme** file.

If we feed our amplifier with an *input step* of sufficiently *small amplitude*, the response is an *exponential transient* governed by the time constant

$$\tau = \frac{1}{2\pi\beta f_i} \quad (10)$$

The amount of time it takes for this transient to swing from 10% to 90% of its final value is called the *rise time* t_R . It is readily seen that $t_R = \tau \ln 9 = 0.35/\beta f_i$. The **transient response** too can be visualized via PSpice, and Fig. 3 shows a circuit to do it for the case $\beta = 1/11$. We now have $t_R = 0.35/(10^6/11) = 3.85 \mu\text{s}$, a result that you can readily verify by studying the output waveform of Fig. 4. On the other hand, had

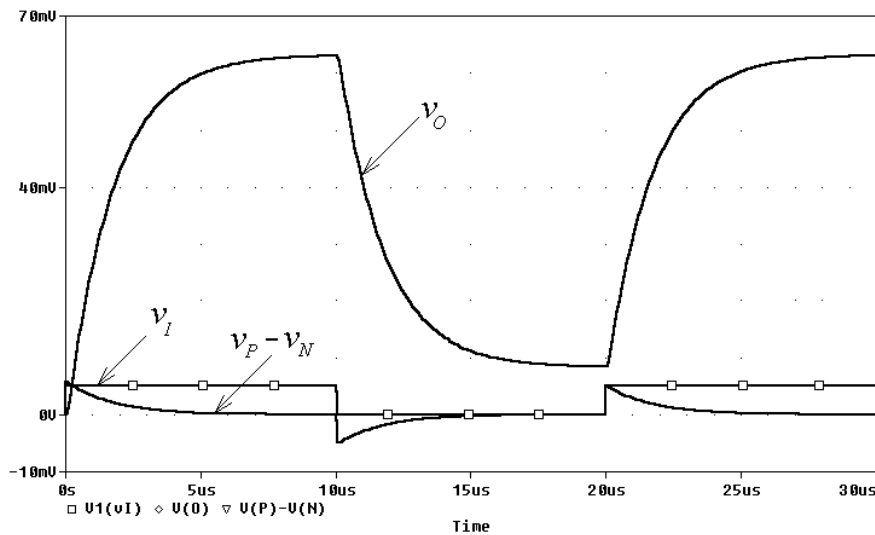


Fig. 4 – *Small-signal* transient response of the circuit of Fig. 3.

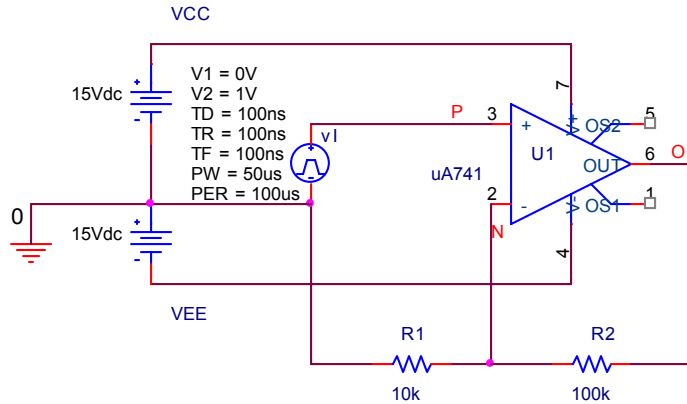


Fig. 5 – PSpice circuit to plot the large-signal transient response.

the same op amp been configured as a voltage follower ($\beta = 1$), then we would have had $t_R = 350$ ns.

If the amplitude of the input step is gradually increased, a point is reached at which the output becomes *slew-rate limited*, and the initial portion of the transient becomes a linear ramp *ramp*. The slope of this ramp is called the *slew rate* (SR). The 741C data sheets give $SR \cong 0.5$ V/ μ s. We use the circuit of Fig. 5 to visualize a slew-rate limited response, and the result is shown in Fig. 6.

The borderline between small-signal and large-signal transient response occurs when the maximum slope of the exponential transient becomes equal to the slew rate. As we know, the slope is maximum at the onset of the transient, and its value is V_{om}/τ , where V_{om} denotes the amplitude of the output transient. Imposing $V_{om}/\tau = SR$, we find the borderline output amplitude to be $V_{om} = \tau SR = SR/(2\pi\beta f_i)$. In our example, $V_{om} = 0.5 \times 10^6 / (2\pi \times 10^6 / 11) = 0.875$ V. This corresponds to an input step amplitude $V_{im} = V_{om}/11 \cong 80$ mV.

It is interesting to observe that in both responses, the op amp yields $v_P - v_N \rightarrow 0$ only once the transient has died out. During the transient, particularly at its onset, v_N is quite different from v_P . Can you exercise your engineering judgement to justify this?

For a sine-wave input, it is of interest to know the borderline frequency above which the output

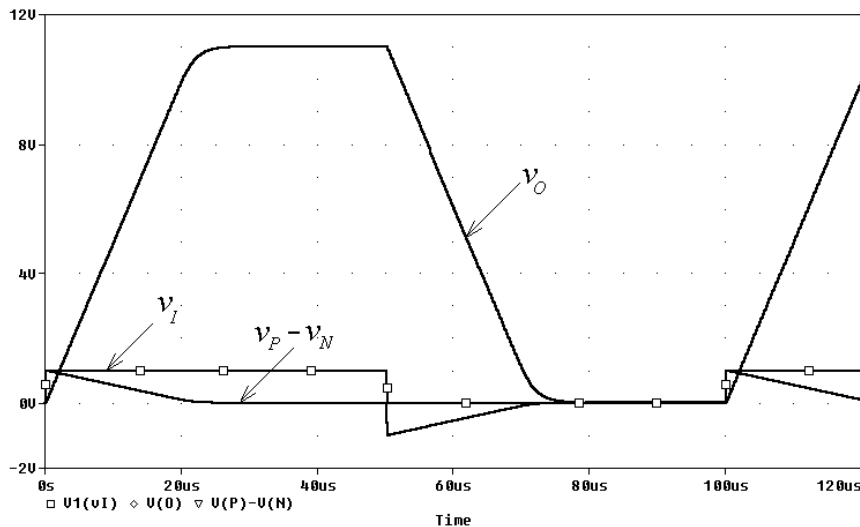


Fig. 6 – Large-signal transient response of the circuit of Fig. 5.

will distort due to slew-rate limiting. Expressing the output as $v_o(t) = V_{om}\sin(2\pi ft)$, we note that the maximum slope occurs at the zero crossings of $v_o(t)$, where slope is $2\pi fV_{om}$. Letting $2\pi fV_{om} \leq SR$ gives

$$f \leq \frac{SR}{2\pi V_{om}} \quad (11)$$

In the case in which V_{om} is as large as it can be, before output clipping occurs, the upper limit provided by Eq. (11) is called the *full-power bandwidth (FPB)*. For a 741C operating with $V_{om} = 10$ V, we get $FPB \cong 8$ kHz.

PART II – EXPERIMENTAL PART

The 741 data sheets give *typical* data, that is, data that were obtained by averaging over a large number of samples. The 741 macro-model is based on typical data. In this lab we shall characterize a *particular* 741 sample, and compare against the data sheets to assess how close our sample is to typical, as well as how realistic the PSpice simulations are.

Like all integrated circuits, op amps are delicate devices that must be used with care to avoid permanently damaging them. Refer to the Appendix for useful tips on how to construct op amp circuits. In particular, always use two 0.1- μ F capacitors to bypass the ± 15 -V power supplies, and always *turn off power before making any changes* in a circuit. Failure to do so may destroy your device, indicating that the measurements performed up to that point will have to be repeated on a different sample.

Henceforth, steps shall be identified as follows: **C** for calculations, **M** for measurements, and **S** for SPICE simulation. Moreover, each measured value should be expressed in the form $X \pm \Delta X$ (e.g. $V_{OS} = 1.52$ mV \pm 0.01 mV), where ΔX represents the estimated uncertainty of your measurement, something you have to figure out based on measurement concepts and techniques learned in Engr 206 and Engr 300.

Finding V_{OS} , I_P , I_N , and $PSRR$:

Mark one of the 741 samples available in your kit (the other is a spare), and proceed as instructed.

M1: With power off, assemble the circuit of Fig. 7(a), using the instructions of the Appendix as guidelines for good circuit-assembly habits. Apply power, and measure the output with your digital

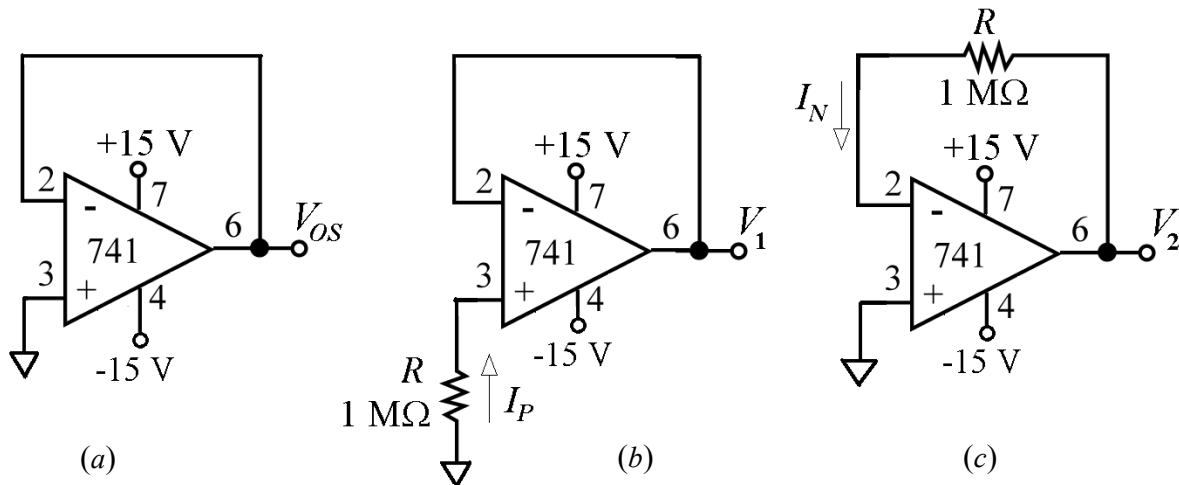


Fig. 7 – Test circuits to measure V_{OS} , I_P , I_N , and $PSRR$.

multi-meter configured as a DC voltmeter with the *highest sensitivity available* (10 μV or better). Given that the op amp is working as a voltage follower, the output reading is simply the input offset voltage V_{OS} . How does it compare with the value given in the data sheets? Comment.

Warning: Because of thermal drift, the least significant digits of your multi-meter are likely to fluctuate, so it is up to you to decide how to interpret your readings, and to justify your decision.

MC2: Turn power off, and insert the 1-M Ω resistor shown in Fig. 7(b). This is intended to cause the current I_P drawn by the *non-inverting input* to develop the voltage $V_P = -RI_P$, so that $V_1 = V_{OS} - RI_P$, by the superposition principle. Apply power, measure V_1 , and calculate $I_P = (V_{OS} - V_1)/R$, with V_{OS} as found in Step M1. For accurate results, you may wish to measure R with the ohmmeter.

MC3: Turn power off, and connect the 1-M Ω resistor as in Fig. 7(c). By similar reasoning, the current I_N drawn by the *inverting input* will yield $V_2 = V_{OS} + RI_N$. Apply power, measure V_2 , and calculate $I_N = (V_2 - V_{OS})/R$, with V_{OS} again as found in Step M1.

C4: Using Eq. (1), calculate I_B and I_{OS} . Hence, compare with their data-sheet values, and comment.

MC5: Turn power off, configure the circuit again as in Fig. 7(a), and lower the supply voltages from $\pm 15\text{ V}$ to $\pm 10\text{ V}$, thus effecting a power-supply change $\Delta V_S = 5\text{ V}$. Apply power, measure the new value of V_{OS} , and find the difference ΔV_{OS} between the current reading and that of Step M1, which you may wish to repeat, just to make sure that the offset hasn't drifted meanwhile. Finally, use Eq. (2) to find $1/PSRR \equiv |\Delta V_{OS}/\Delta V_S|$, in $\mu\text{V}/\text{V}$. Compare with the value given in the data sheets, and comment.

The Difference Amplifier:

To understand the implications of various op amp imperfections, we examine a very popular circuit, namely, the *difference amplifier* of Fig. 8a. As we know, if its resistances are in equal ratios

$$\frac{R_4}{R_3} = \frac{R_2}{R_1} \quad (12)$$

then the circuit gives

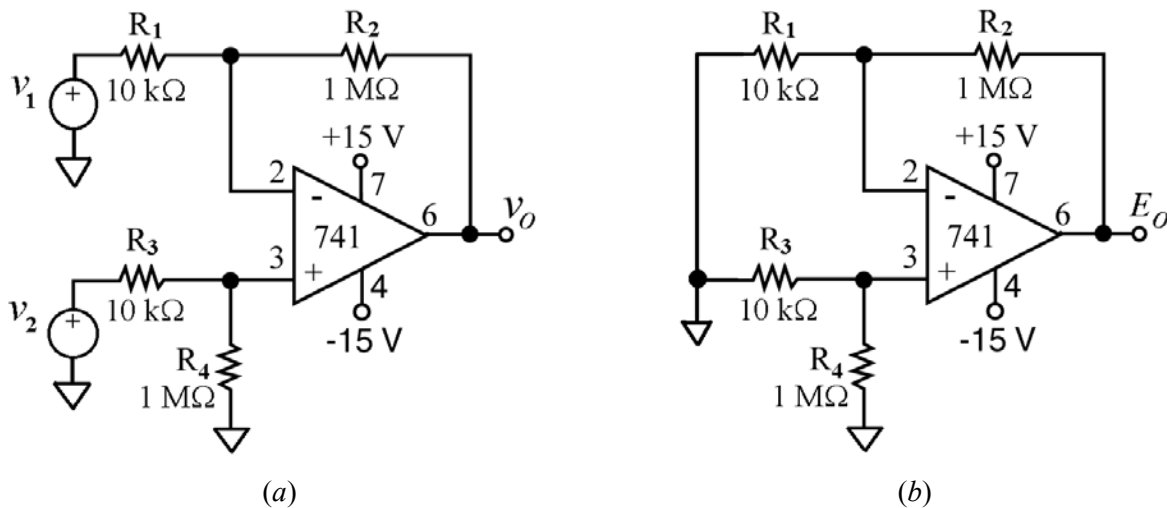


Fig. 8 – The difference amplifier .

$$v_o = \frac{R_2}{R_1}(v_2 - v_1) \quad (13)$$

With the component values shown, $v_o = 100(v_2 - v_1)$. Equation (13) indicates that v_o depends *exclusively* on the *difference* between the inputs, even if they happen to be different from zero. In particular, if the inputs are grounded ($v_1 = v_2 = 0$) as in Fig. 8b, the circuit ought to give 0 V also at the output. In practice, it yields an *output error* E_o generally different from zero.

C6: Show that the circuit of Fig. 8b gives

$$E_o = \frac{1}{\beta}[V_{os} - (R_1 // R_2)I_{os}] \quad (14)$$

where $1/\beta$ is aptly called the *noise gain*. Hence, use the experimental data gathered so far to predict the value of E_o .

M7: Pick a pair of 10-k Ω and a pair of 1-M Ω resistors from your kit and measure all four of them with the digital ohmmeter. Then, with power off, assemble the circuit of Fig. 8(b), using the *smaller* of the two 10-k Ω resistors as R_1 (and, of course, the *larger* one as R_3), and using the *larger* of the two 1-M Ω resistors as R_2 (and, of course, the *smaller* one as R_4). This arrangement results in the greatest degree of imbalance in the resistance ratios. Apply power, measure E_o , compare with the predicted value of Step C6, and account for possible differences.

Offset Error Nulling:

M8: The 741 op comes with provision for nulling the input offset error appearing inside brackets in Eq. (14). Nulling is accomplished by connecting an external 10-k Ω potentiometer as specified in the data sheets. The purpose of this pot is to *deliberately imbalance* the internal circuitry of the op amp so as to allow the user to drive E_o to zero. With power off, connect the pot between pins 1 and 5 as shown in Fig. 9. Reapply power, and vary the wiper until E_o comes as close as possible to 0 V, giving the appearance of an *offset-less* op amp! Once the pot has been adjusted, it should not be touched again, unless necessary because of thermal drift or other changes in the circuit.

Finding the CMRR:

If the left terminals of R_1 and R_3 are lifted off ground and driven with a common voltage v_{CM} as depicted

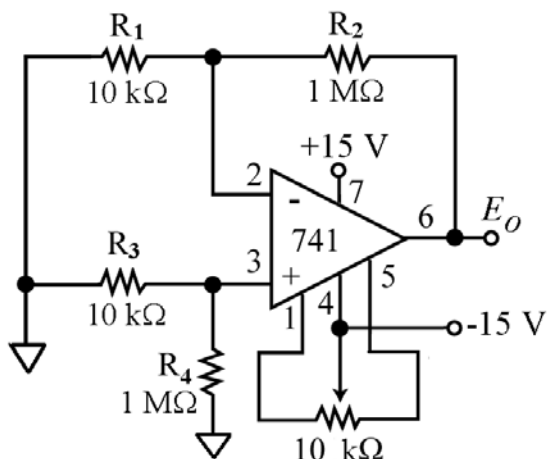


Fig. 9 – Difference amplifier with provision for *offset nulling*.

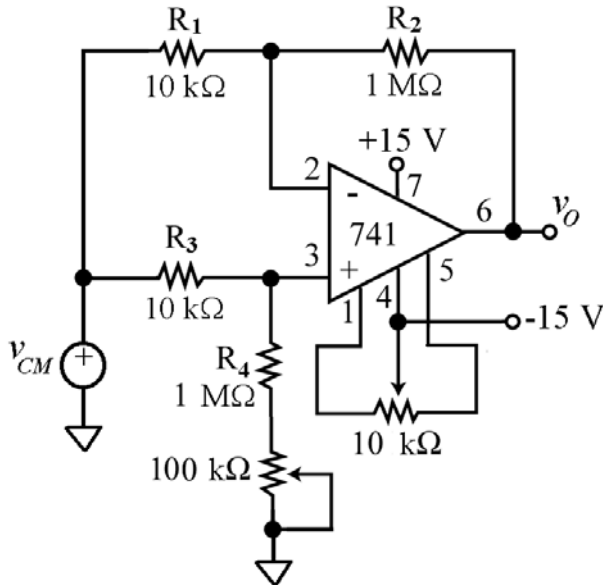


Fig. 10 – Circuit setup to optimize the *CMRR* of a difference amplifier.

in Fig. 10, we expect that a true difference amplifier will give $v_O = 0$ regardless of v_{CM} . In practice, v_O is likely to be different from zero because actual resistors will fail to satisfy Eq. (12) exactly, and also because of op amp nonidealities. The ratio v_O/v_{CM} is called the *common-mode gain*,

$$A_{cm} = \frac{v_O}{v_{CM}} \quad (15)$$

and our goal is to minimize it to approach the ideal condition $A_{cm} \rightarrow 0$. (As we shall see shortly, this is achieved via the 100-kΩ pot, as shown.) If we define $v_{DM} = v_2 - v_1$ in Fig. 8a, then the gain

$$A_{dm} = \frac{v_O}{v_{DM}} \quad (16)$$

is by contrast called the *differential-mode gain*. (The circuit of Fig. 8a has $A_{dm} = R_2/R_1 = 100$ V/V.) A very important *figure of merit* of a difference amplifier is its *common mode rejection ratio*, defined as

$$CMRR_{dB} = 20 \log \left| \frac{A_{dm}}{A_{cm}} \right| \quad (17)$$

Ideally, we'd want $A_{cm} \rightarrow 0$, and thus $CMRR \rightarrow \infty$. In practice, A_{cm} will be small but not zero, and clearly the smaller A_{cm} , the closer the amplifier will be to ideal.

MC9: With power off, add to your difference amplifier the 100-kΩ pot as indicated in Fig. 10. Initially, turn the wiper *all the way up* so as to short out the pot resistance and leave the resistance ratios as in Fig. 9. Next, apply power, and using Ch. 1 of the oscilloscope to monitor v_{CM} , adjust the waveform generator so that v_{CM} is a 100-Hz sine wave alternating between -5 V and $+5$ V. Observing v_O with Ch. 2 of the oscilloscope, measure the gain $A_{cm} = v_O/v_{CM}$, and insert it into Eq. (17), along with $A_{dm} \cong 100$ V/V, to find the value of $CMRR_{dB}$ for your difference amplifier.

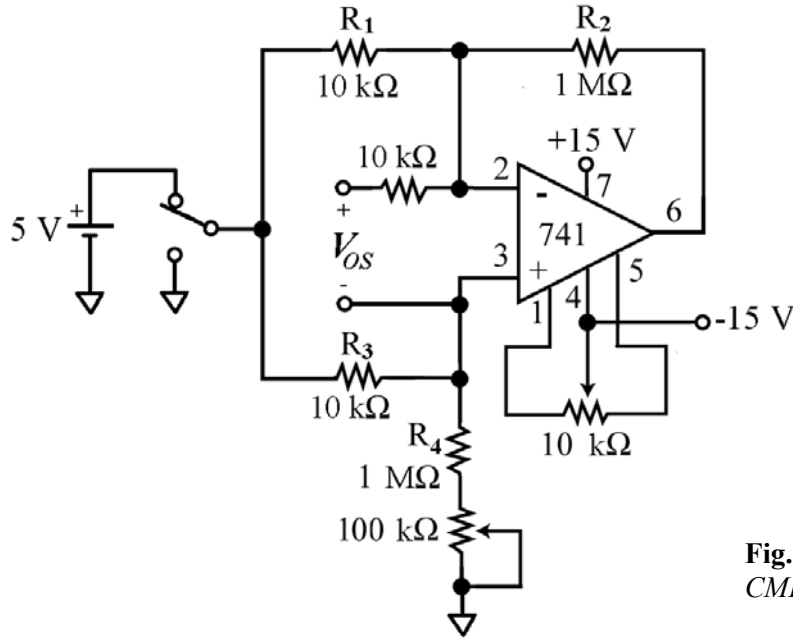


Fig. 11 – Test circuit to find the $CMRR$ of the basic op amp.

MC10: Now vary the wiper of the 100-k Ω pot in Fig. 10 until v_O is *minimized*. This, in turn, will maximize the $CMRR$ of your circuit. What is its new value, in dB?

Remark: If the resistance range provided by the pot is insufficient, insert a series resistance (~50 k Ω) between pot and ground.

MC11: Now let us take advantage of the calibrated circuit of Fig. 10 to find the $CMRR$ of the basic op amp via Eq. (3). With power off, insert the additional 10-k Ω resistor shown in Fig. 11 (the reason is given below). Then, apply power, and measure V_{OS} first with the switch to ground, then with the switch to +5 V (obtain 5 V from the third output available from your bench power supply). Next, calculate the difference ΔV_{OS} between the two readings. Note that flipping the switch from 0 V to 5 V causes the common-mode input to the basic op amp to change by $\Delta v_{CM} = 5R_4/(R_3 + R_4) \cong 5$ V, so apply Eq. (3) to estimate $CMRR \cong |\Delta v_{CM}/\Delta V_{OS}| \cong |(5 \text{ V})/\Delta V_{OS}|$. Give its value in dB, compare with the data sheets, and comment.

Remark: Never connect a cable directly to the inverting input of an op amp! The cable's stray capacitance – be it the cable of a voltmeter or the probe of an oscilloscope – tends to destabilize the op amp, possibly causing it to oscillate. *Always interpose an isolating resistor*, such as the 10-k Ω resistor shown.

Finding A_{OL0} and I_{SC} :

MC12: With power off, assemble the circuit of Fig. 12 (you can create the 15-k Ω resistor as 10 k Ω in series with the 10-k Ω pot with the wiper set in the middle). Then, apply power, and measure V_D and V_O with the switch first flipped to +15 V (positive supply), then flipped to -15 V (negative supply). (When measuring V_D , be sure to configure the voltmeter for its maximum sensitivity!) Next, calculate the differences ΔV_D and ΔV_O , and finally obtain $A_{OL0} = |\Delta V_O/\Delta V_D|$. Compare with the data sheets, comment.

Remark: Note again the use of the 10-k Ω isolating resistor!

MC13: In the circuit of Fig. 12, connect the *current meter* directly between the output node and ground, and measure current first with the switch to +15 V, then with the switch to -15 V. The two readings represent, respectively, the *maximum current* that the op amp is capable of *sinking* from and *sourcing* to

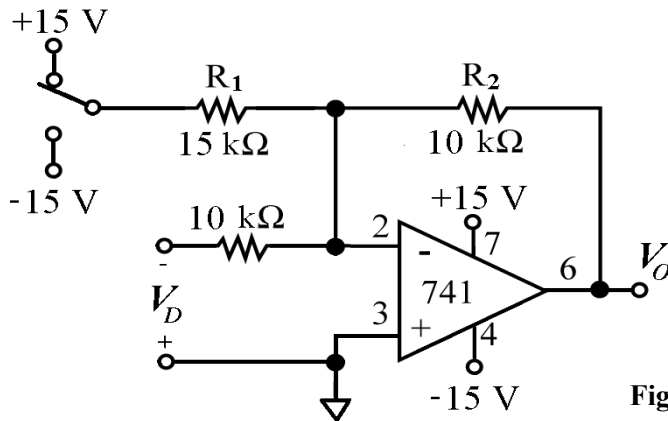


Fig. 12 – Test circuit to find A_{OL0} and I_{SC} .

an output load. Are your readings approximately similar? How do they compare with the value of I_{SC} given in the data sheets?

Finding f_b and f_i :

We now investigate the *frequency response* using the circuit of Fig. 13. Here, the op amp is configured to amplify the input v_i with the gain $A_{CL0} = 1/\beta = 1 + R_2/R_1 \cong 1000$ V/V. (Before assembling the circuit, you may want to measure R_1 and R_2 to find the actual value of β .) To prevent v_o from saturating, we must keep v_i suitably small, so we obtain it from the waveform generator v_s via a voltage divider such that $v_i = v_s R_4 / (R_3 + R_4) \cong v_s / 1000$. Moreover, since we have a new set of resistance values, the error term within brackets in Eq. (14) will also change, mandating that you *again offset null* your amplifier as in Step M8.

MC14: With power off, assemble the circuit of Fig. 13. Apply power, and null the offset as in Step M8. Next, while monitoring v_s with Ch. 1 of the oscilloscope, adjust the waveform generator so that v_s is a *sine wave* with an amplitude of 2.5 V (5-V peak-to-peak), 0-V DC, and frequency $f \sim 10$ Hz. Then, while monitoring v_o with Ch. 2 of the oscilloscope, gradually increase f while keeping the amplitude of v_s constant, until the amplitude of v_o drops to 0.707 (70.7%, or -3 dB) of its low-frequency value. Record this frequency, which is the *closed-loop bandwidth* f_B of your circuit. Finally, use Eq. (9b) to estimate f_i . How does it compare with the data sheets? Comment.

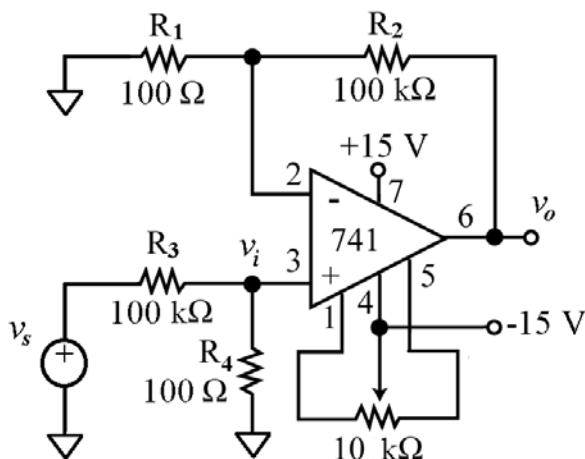


Fig. 13 – Test circuit to investigate the *frequency response*.

M15: In the circuit of Fig. 13 measure the amplitude V_{om} of v_o also at $f = 10f_B$ and at $f = 100f_B$, and find the corresponding values of the closed-loop gain $A_{CL} = |V_{om}/V_{im}|$, where V_{im} is the amplitude of v_i . Finally verify the *constancy* of the *GBP*, namely, $GBP = A_{CL} \times f = \text{constant}$.

C16: Using the value of A_{OL0} obtained in step MC12, estimate f_b . Hence, sketch the magnitude Bode plots of both the *open-loop* and *closed-loop* responses of your *particular* amplifier sample. How do they compare with the *typical* plots of Fig. 2? Comment.

M17: With power off, change R_4 to 10 k Ω in the circuit of Fig. 13, and connect a 2-k Ω *load* between the op amp output pin (pin #6) and ground. Moreover, adjust the waveform generator so that v_s is a 1-kHz sine wave with minimum amplitude and zero DC offset. Next, apply power, and while monitoring v_o with the oscilloscope, gradually increase the amplitude of v_s until v_o *clips*. Measure on the oscilloscope the *upper* and *lower saturation limits* V_{OH} and V_{OL} . Are they symmetric? Different? Justify. How do they compare with the data-sheet values?

Finding t_R :

To find this parameter, we use the inverting amplifier of Fig. 14, for which $A_{CL0} = -R_2/R_1 = -1V/V$, $\beta = 1/(1 + R_2/R_1) = 1/2$, and $f_B = (1/2)f_i$.

MC18: With power off, assemble the circuit of Fig.14. Then, while monitoring v_s with Ch. 1 of the oscilloscope, adjust the waveform generator so that v_s is a *square wave* alternating between 0 V and +50 mV with initial frequency $f \sim 250$ kHz. (If you have difficulty adjusting the waveform generator for this small an amplitude, you can interpose a suitable voltage divider between v_s and R_1). Next, apply power, observe v_o with Ch. 2 of the oscilloscope, and find the rise time t_R , that is, the amount of time it takes for the output to swing from 10% to 90% of its final value (for best visualization, you may need to vary f up or down from the suggested value.) How does the measured value compare with the expected value $t_R = 0.35/\beta f_i$? Comment.

S19: Run a PSpice simulation of the circuit of Step MC18 using the 741 macro-model available in PSpice's library. Plot the output waveform, and use the cursor to find t_R . Hence, compare with your measured value and account for possible differences based also on your conclusions of Step. MC18.

Finding SR and FPB :

To find these parameters we still use the circuit of Fig. 14, but with a *much greater* input amplitude.

MC20: In the circuit of Fig. 14, adjust the waveform generator so that v_s is a *square wave* now alternating between 0 V and +5 V with initial frequency $f \sim 25$ kHz. Hence, determine the slopes of the

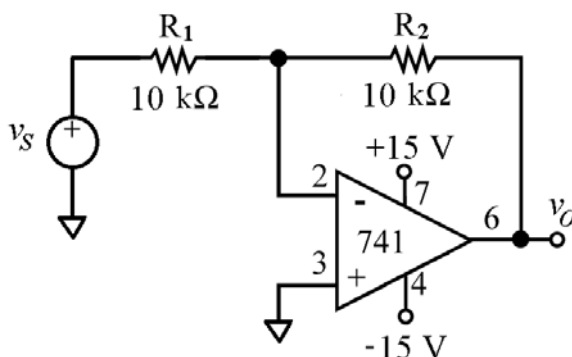


Fig. 14 – Test circuit to find t_R , SR , and the FPB .

two ramps, in V/ μ s. How do they compare with the data-sheet *SR* value for the 741C?

Note: For best visualization of the slopes, you may need to vary the frequency from the suggested initial value of 25 kHz.

MC21: Adjust the waveform generator so that v_S is now a 1-kHz *sine wave* alternating between -10 V and $+10$ V. Then, gradually increase its frequency while observing with the oscilloscope the *slope* of v_O near its zero crossings, where it is steepest. As you increase frequency, slope also increases, until a point is reached beyond which it won't increase any more due to slew-rate limiting, no matter how much you increase frequency. Record the frequency at which the slope *just begins* to saturate, and compare it with the frequency predicted by Eq. (11). Justify any differences.

Note: For best visualization of slope on the screen, you will find it necessary to keep increasing also the horizontal sensitivity of your oscilloscope as you increase frequency and thus slope. For best results, keep adjusting sensitivity so that slope is always in the vicinity of 45° on the screen.

MC22: Reduce v_S to half its magnitude of Step MC21, and find the new frequency at which the slope of v_O just begins to saturate near its zero crossings. Again, compare with Eq. (11), and comment.