

Course Outline for ENGR 453 Digital Integrated Circuit Design

Bulletin Description:

453 Digital Integrated Circuit Design (4)

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Prerequisite: grades of C or better in ENGR 301, 353, and 356. Integrated circuit technology, transistor characteristics and models. MOS and bipolar logic families, noise margins, speed, power, fanout, interfacing, PSpice simulation. Regenerative circuits and memories. Classwork, 3 units; laboratory, 1 unit. Extra fee required.

Textbooks:

1. Sedra, Adel S., and Smith, Kenneth C.: *Microelectronics*, 4th Ed, Oxford University Press, 1997
2. Franco, Sergio: *ENGR 453 Lab Manual*, downloadable from the Web.
3. Roberts, Gordon W., and Sedra, Adel S.: *SPICE*, 2nd Ed.; Oxford University Press, 1997.

References:

1. Databooks and application notes by major digital IC manufacturers.

Coordinator:

Sergio Franco, Professor of Electrical Engineering

Prerequisites by Topic:

1. Basic digital electronics concepts
2. Electronic circuit analysis, with emphasis on transient analysis
3. Basic semiconductor theory, *pn* junction, MOSFET, and BJT fundamentals
4. Ability to use PSpice for simple transistor circuit simulations

Course Objectives:

1. To study basic semiconductor principles and digital IC technology {A.1, B.1}*
2. To investigate the static and dynamic characteristics of popular MOS and bipolar logic families, with emphasis on CMOS and TTL technologies {B.1}
3. To study the design of common logic circuits, such as combinational circuits, regenerative circuits, and various types of memories {B.1}
4. To measure and verify the performance of digital circuits in the laboratory {B.2}
5. To perform the SPICE simulation of simple digital circuits {B.3}

**Refers to School of Engineering desired outcome*

Topics:

1. Review of basic concepts and terminology for digital ICs
2. MOSFETs: fabrication, electrical characteristics, models, SPICE simulation
3. MOS inverters and gates: static and dynamic characteristics of CMOS, pseudo-nMOS, pass-

- transistor, and dynamic logic circuits
4. Semiconductor memories: memory structures, ROMs, static and dynamic RAMs, sense amplifiers
 5. BJTs: fabrication, electrical characteristics, models and SPICE simulation.
 6. BJT inverters: static characteristics and switching times.
 7. BJT logic families: RTL, DTL, TTL, LSTTL, ECL, and BiCMOS
 8. Regenerative circuits: flip-flops and multivibrators

Professional Component:

1. Engineering Sciences: 50%
2. Engineering Design: 50%

Evaluation:

1. About a dozen homework assignments (about 8 problems each):10% overall
2. Three 1-hour midterm exams 4 problems each): 13% each
3. One 2.5-hour final exam (5 problems): 21%
4. Laboratory: 30%

Performance Criteria:

Objective 1

- 1.1 Students will demonstrate an understanding of MOSFET properties, characteristics, and models. [1, 2, 3, 4], {A.1, B.1}
- 1.2 Students will demonstrate an understanding of BJT properties, characteristics, and models. [1, 2, 3, 4], {A.1, B.1}
- 1.3 Students will become conversant with digital IC technology and fabrication techniques. [1], {A.1, B.1}

Objective 2

- 2.1 Students will develop an ability to calculate noise margins and propagation delays of basic MOS gates, including CMOS, pseudo-nMOS, pass-transistor, and dynamic logic circuits. [1, 2, 4], {B.1}
- 2.2 Students will demonstrate an ability to calculate the noise margins and fanout of basic resistive-load BJT inverters, and use charge-control analysis to predict their propagation delays. [1, 2, 4], {B.1}
- 2.3 Students will demonstrate an ability to interface between different logic families. [1, 3, 4], {B.1}

Objective 3

- 3.1 Students will demonstrate an ability to analyze and design basic combinational circuits in the most popular technologies, particularly CMOS and TTL technologies. [1, 2, 3, 4], {B.1}
- 3.2 Students will demonstrate an understanding of various types of regenerative circuits, such as bistable, monostable, and astable multivibrators. [1, 3, 4], {B.1}
- 3.3 Students will demonstrate an understanding of basic semiconductor memory concepts, such as organization and memory types (ROMs, PROMs, EPROMs, EEPROMs, static RAMs, and dynamic RAMs). [1, 3], {B.1}

Objective 4

- 4.1 Students will demonstrate an ability to characterize MOS and bipolar transistors

- experimentally. [4], {B.2}
- 4.2 Students will demonstrate an ability to characterize experimentally logic inverters representative of different technologies. [4], {B.2}
 - 4.3 Students will demonstrate an ability to design and characterize a variety of breadboarded logic circuits. [4], {B.2}

Objective 5

- 5.1 Students will demonstrate a skill in the SPICE simulation of simple transistor circuits. [1, 4], {B.3}
- 5.2 Students will demonstrate a skill in the SPICE simulation of basic logic gates using measured parameters. [4], {B.3}

*Numbers in brackets [] refer to evaluation method

**Related School outcomes { }

Class/Laboratory Schedule:

Three 50-minute lectures/week (or two 75-minute lectures/week, depending on scheduling needs)
One 3-hour lab/week

Scheduled Coverage:

1. Basic concepts: digital vs. analog; logic levels, voltage transfer characteristics, noise margins, fanout, rise and fall times, propagation delays (Ch. 1 and Ch. 13)
2. Physical structure of the enhancement MOSFET; threshold voltage, body effect; nMOSFETs and pMOSFETs; CMOS (Ch.5)
3. The $i-v$ characteristics of enhancement MOSFETs (Ch.5)
4. Depletion MOSFETs; threshold voltage as a function of channel implant; operating limits; parameter measurements (Ch.5)
5. The CMOS inverter: VTC and noise margins, dynamic operation (Ch.5)
6. CMOS transmission gates; internal capacitances; SPICE models (Ch.5)
7. The CMOS inverter revisited: static and dynamic properties, power dissipation, power-delay product (Ch. 13)
8. CMOS logic-gate circuits (Ch. 13)
9. Pseudo-nMOS logic circuits (Ch. 13)
10. Pass-transistor logic circuits (Ch. 13)
11. Dynamic logic circuits (Ch. 13)
12. Latches and flip flops (Ch. 13)
13. Multivibrator circuits (Ch. 13)
14. Semiconductor memories (Ch. 13)
15. Static cells (Ch. 13)
16. Dynamic cells and sense amplifiers (Ch. 13)
17. Row and column address decoders (Ch. 13)
18. ROMs, PROMs, EPROMs, Spice simulation (Ch. 13)
19. Physical structure of the BJT and modes of operation (Ch. 5)
20. Review of the BJT logic inverter; saturation and switching times (Ch. 5 and Ch. 14)
21. Early forms of BJT logic circuits: RTL and DTL (Ch. 14)
22. The basic TTL inverter (Ch. 14)
23. TTL inverter characteristics; TTL Gates (Ch. 14)

24. Schottky TTL and low-power Schottky TTL (Ch. 14)
25. The ECL principle (Ch. 14)
26. ECL gates and characteristics (Ch. 14)
27. BiCMOS digital circuits (Ch. 14)
28. Gallium-arsenide technology (Ch. 4)
29. Gallium-arsenide digital circuits (Ch. 14)
30. Interfacing between different logic families
31. SPICE simulation
32. VLSI fabrication technology

Notes on Evaluation:

1. No late homework accepted. Solutions to the homework assignments are posted in the solution window across Sci 144. For each assignment, two randomly selected problems are graded, each with a subjective grade of 0, 1, or 2 points.
2. All exams are closed book. One standard (8½" × 11") double-sized sheet of notes allowed.
3. *No make-up exams* and *no incomplete* grades without a serious and verifiable medical justification. *No changes* in the exam dates, *no exceptions*.
4. Grading criteria (Example: 55% to 60% results in a grade of C):

0<F<35<D-<40<D<45<D+<50<C-<55<C<60<C+<65<B-<70<B<75<B+<80<A-<85<A<100

Notes on Prerequisites:

Engineering students must have a copy of the course approval form on file. Non-engineering students must submit a copy of the grade report showing the appropriate course grade for ENGR 301, 353, and 356.

Relationship to Other Courses:

This course extends ENGR 353/356 and complements ENGR 378/456/478. While the latter focus on digital *systems design*, ENGR 453 concentrates on *device design* aspects. This correspondence in the digital realm mirrors the correspondence between ENGR 445 and ENGR 442 in the analog realm. Together, these courses provide students with a fairly comprehensive background in microelectronics with emphasis on design.