

San Francisco State University
Electrical Engineering

Course Outline for ENGR 445 Analog Integrated Circuit Design
Fall 2009

Bulletin Description:

445 Analog Integrated Circuit Design (4)

F

Prerequisite: grades of C or better in ENGR 301 and 353. Integrated circuit technology, transistor characteristics and models. Analysis and design of monolithic op amps. Frequency response, negative feedback, stability, PSpice simulation. Classwork, 3 units; laboratory, 1 unit. Extra fee required.

Textbooks:

1. S. Franco, *Introduction to Analog Integrated Circuit Design*, class notes distributed by the SFSU Student Chapter of the IEEE Society.
2. S. Franco, *ENGR 445 Lab Manual*, downloadable from <http://online.sfsu.edu/~sfranco>

References:

1. Sergio Franco, *An Introduction to Microelectronics*, University Readers, 2009.
2. Larry Klingenberg, *Introduction to PSpice – A quick Guide to Using PSpice 9.2*. Visit also <http://online.sfsu.edu/~larryk>
3. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5/E., Wiley & Sons, 2009.

Coordinator:

Sergio Franco, Professor of Electrical Engineering

Prerequisites by Topic:

- 1 Basic semiconductor theory, *pn* junction, MOSFET, and BJT fundamentals
- 2 Circuit analysis techniques with dependent sources, concept of equivalence
4. Basic systems theory, frequency and time responses, Bode Plots
5. Ability to use PSpice for simple transistor circuit simulations

Course Objectives¹:

1. To study basic semiconductor principles and analog IC technology. [A.1, B.1, B.4]
2. To study analog IC building blocks up to the complete 741 op amp. [B.1, B.4]
3. To investigate the frequency response of analog ICs. [B.1]
4. To study negative feedback, stability, and frequency compensation. [B.1]
5. To observe and measure the performance of analog ICs in the laboratory. [A.3, B.2]
6. To perform the SPICE simulation of simple digital circuits [B.3]

¹Indices in brackets refer to educational objectives and outcomes of the School of Engineering.

Topics:

1. Models for integrated-circuit active devices
2. Bipolar and MOS integrated-circuit technology
3. Single-transistor and two-transistor amplifiers

4. Current sources, active loads, and output stages
5. Large-signal and small-signal analysis of the 741 op amp
6. Frequency and time responses of integrated circuits
7. Negative feedback
8. Frequency response, stability, and frequency compensation of negative-feedback amplifiers.

Professional Component:

1. Engineering Sciences: 50%
2. Engineering Design: 50%

Evaluation:

1. Thirteen homework assignments: 10% overall
2. Three 1-hour midterm exams: 13% each
3. One 2.5-hour final exam: 21%
4. Laboratory: 30%

Performance Criteria²:

Objective 1

- 1.1 Students will demonstrate an understanding of *pn* junction properties and *i-v* characteristics. [1, 2, 3, 4]
- 1.2 Students will demonstrate an understanding of BJT properties, characteristics, and models. [1, 2, 3, 4]
- 1.3 Students will become conversant with analog IC technology and fabrication techniques. [1, 4]

Objective 2

- 2.1 Students will demonstrate an understanding of classical single-transistor and two-transistor configurations. [1, 2, 4]
- 2.2 Students will demonstrate an understanding of basic analog IC building blocks (current sources, active loads, and output stages). [1, 2, 4]
- 2.3 Students will demonstrate an ability to perform the DC and small-signal analysis of a complete IC op amp (741). [1, 2, 3, 4]

Objective 3

- 3.1 Students will demonstrate an ability investigate the frequency response of basic analog IC building blocks. [1, 2, 3, 4]
- 3.2 Students will demonstrate an ability to investigate the small- and large-signal transient response of an IC op amp. [1, 2, 3, 4]

Objective 4

- 5.1 Students will demonstrate an ability to identify and analyze classic negative-feedback topologies. [1, 2, 3]
- 5.2 Students will demonstrate an ability to assess the stability of a negative-feedback circuit. [1, 3, 4]
- 5.3 Students will become conversant with the most common frequency-compensation techniques. [1, 3, 4]

Objective 5

- 5.1 Students will demonstrate an ability to characterize electronic devices experimentally. [4]
- 5.2 Students will demonstrate an ability to characterize analog building blocks

experimentally. [4]

- 5.3 Students will demonstrate an ability to design and characterize a breadboard version of an IC op amp. [4]

Objective 6

- 6.1 Students will demonstrate a skill in the SPICE simulation simple analog circuits. [1, 4]
- 6.2 Students will demonstrate a skill in the SPICE simulation of basic analog building blocks using measured parameters. [4]

² Numbers in brackets refer to evaluation methods used to assess student performance.

Fall 09

Instructor: Sergio Franco, Ph.D.

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Class/Laboratory Schedule:

Two 75-minute lectures/week, one 3-hour lab/week

Scheduled Coverage (based on three 50-minute lectures/week):

1. Design considerations in monolithic circuits
2. Review of BJT characteristics
3. Basic BJT configurations
4. Review of MOSFET characteristics
5. Basic MOSFET configurations
6. Darlington configurations
7. Cascode configurations
8. Differential pairs – large-signal characteristics
9. Differential pairs – small-signal characteristics
10. Common-mode rejection ratio in differential pairs
11. Input offset voltage/current in differential pairs
12. Current Mirrors – basic concepts
13. Current Mirrors – advanced concepts
14. Differential pairs with active loads
15. CMRR and V_{OS} of differential pairs with active loads
16. Output stages – introduction
17. Output stages – advanced
18. Short-circuit protection and CMOS
19. The 741 Operational Amplifier – overview
20. The input and intermediate stages
21. The output stage and complete small-signal characteristics
22. High-frequency BJT model
23. High-frequency MOSFET model
24. The Miller approximation

25. Exact frequency analysis of the CE/CS configurations
26. Frequency response of differential amplifiers
27. Frequency response of voltage buffers
28. I/O impedances of voltage buffers, frequency characteristics of current buffers
29. The open-circuit time-constant analysis technique
30. Frequency response of cascode amplifiers
31. Negative feedback basics
32. Effect of feedback on distortion, noise, and bandwidth
33. Feedback topologies and closed-loop I/O resistances
34. Practical configurations and the effect of loading
35. Practical examples
36. Feedback Circuit Analysis Using the Return Ratio
37. Practical examples
38. Blackman's impedance formula
39. Injection methods

1. Notes on Evaluation:

2. No late homework accepted. Solutions to the homework assignments are posted in the solution window across Sci 144. For each assignment, two randomly selected problems are graded, each with a subjective grade of 0, 1, or 2 points.
3. All exams are closed book. One standard (8½" × 11") double-sized sheet of notes allowed.
4. **No make-up exams** and **no incomplete** grades without a serious and verifiable medical justification. **No changes** in the exam dates, **no exceptions**.
4. **Final exam:** Wed, Dec 16, 5:00-7:30 pm, in the lecture room.
5. Grading criteria (Example: 55% to 60% results in a grade of C):

0<F<35<D-<40<D<45<D+<50<C-<55<C<60<C+<65<B-<70<B<75<B+<80<A-<85<A<100

Notes on Prerequisites:

Engineering students must have a copy of the course approval form on file. Non-engineering students must submit a copy of the grade report showing the appropriate course grade for ENGR 301 and 353.

Relationship to Other Courses:

This course extends ENGR 353 and complements ENGR 442. While ENGR 442 focuses on analog *systems design*, ENGR 445 concentrates on *device design* aspects. This correspondence in the analog realm mirrors the correspondence between ENGR 453 and ENGR 478 in the digital realm. Together, these courses provide students with a fairly comprehensive background in microelectronics with emphasis on design.