San Francisco State University
Electrical Engineering

Course Outline for Engr 442 Operational Amplifier Network Design
Fall 2009

Bulletin Description:
442 Operational Amplifier Network Design (3) **F,S**
Prerequisite: grades of C or better in Engr 205, concurrent enrollment in Engr 305. Design of op-amp based amplifiers, signal converters, conditioners, filters. Negative feedback, practical op-amp limitations. Voltage comparators, Schmitt triggers, nonlinear signal processing. Sine-wave oscillators, multivibrators, function generators. Design project involving PSpice imulation.

Textbooks:
1. Sergio Franco, *Design with Operational Amplifiers and Analog ICs*, 3rd Ed., WCB/McGraw-Hill, 2002.
2. Larry Klingengberg, *Introduction to PSpice – A quick Guide to Using PSpice 9.2*, notes developed for the Engr 206 and Engr 301 labs. Visit also http://online.sfsu.edu/~larryk

Coordinator:
Sergio Franco, Professor of Electrical Engineering

Prerequisites by Topic:
1. Circuit analysis techniques with dependent sources, equivalence
2. Basic systems analysis concepts using Laplace techniques and Bode Plots
3. Transient and frequency response of 1st-order circuits
4. Ability to use PSpice for simple circuit simulations

Course Objectives[1]:
1. To investigate a variety of resistive op amp circuits with emphasis on feedback principles. [A,1, B.1, B.4]
2. To analyze and design active filters [A.1, B.1, B.4]
3. To investigate the effect of op amp nonidealities upon the DC as well as the AC and transient responses of popular op amp circuits [B.1]
4. To study the design of popular op amp and comparator applications in test, control, and instrumentation [B.1]
5. To perform SPICE simulation of common analog circuits [B.3]

[1]Indices in brackets refer to educational objectives and outcomes of the School of Engineering.

Topics:
1. Review; basic closed-loop configurations; negative feedback; op amp powering and saturation.
2. *I-V*, *V-I*, and *I-I* converters; difference and instrumentation amplifiers.
3. 1st-order filters. 2nd-order active filters: *KRC*, multiple feedback, state-variable and biquads.
4. Input-referred DC errors, drift, CMRR and PSRR; operating limits.
5. Frequency response, input /output impedances, small- and large-signal transient responses.
6. Voltage comparators and Schmitt triggers; precision rectifiers.

7. Sinusoidal oscillators, multivibrators, IC timers, waveform generators, VCOs.

Professional Component:
1. Engineering Sciences: 33%
2. Engineering Design: 67%

Evaluation:
1. Thirteen weekly homework assignments:10% overall
2. Three 1-hour midterm exams: 16% each
3. One 2.5-hour final exam: 22%
4. Design project: 20%

Performance Criteria[2]:

Objective 1

1.1 Students will demonstrate the ability to analyze and design a variety of popular op amp circuits, including signal converters and instrumentation blocks. [1, 2]

1.2 Students will demonstrate an understanding of the curative properties of negative feedback. [1, 2]

1.3 Students will demonstrate an ability to identify negative-feedback topologies and estimate the loop gain of a circuit. [1, 2]

Objective 2

2.1 Students will become conversant with systems poles, zeros, and Bode Plots as applied to op amp circuits. [1, 2, 3]

2.2 Students will demonstrate an ability to analyze and design first-order op amp filters. [1, 2]

2.3 Students will demonstrate an ability to analyze and design second-order active filters and compare different topologies. [1, 2]

Objective 3

3.1 Students will become conversant with the internal structure of a practical op amp and the origins of its non-idealities. [1, 2]

3.2 Students will demonstrate a skill in using data sheets to assess the limitations of practical analog ICs. [1,],

3.3 Students will demonstrate an ability to predict the effect of static op amp limitations upon DC circuit performance. [1, 2]

3.4 Students will demonstrate an ability to predict the effect of dynamic op amp limitations upon circuit performance in both the frequency and time domains. [1, 2]

Objective 4

4.1 Students will become conversant with a variety of popular test, control, and instrumentation blocks (comparators, Schmitt triggers, precision rectifiers, SHAs, timers, function generators, VCOs, and *V*-*F* and *F*-*V* converters). [1, 2, 3]

4.2 Students will be capable to assess the impact of component non-idealities upon circuit performance [1, 2,3]

Objective 5

5.1 Students will demonstrate a skill in the PSpice simulation of the circuits investigated in the course. [1]

[2] Numbers in brackets refer to evaluation methods used to assess student performance.

Fall 09

Instructor: Sergio Franco, Ph.D.
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Class/Laboratory Schedule:
Two 75-minute lectures/week

Scheduled Coverage (based on three 50-minute lectures/week)**:**

1. Review of op amp circuit analysis techniques
2. Summing and difference amplifiers
3. The differentiator, integrator, and the negative resistance converter
4. Negative feedback and its curative properties
5. Feedback in op amp circuits: the noninverting configuration
6. The inverting configuration
7. The loop gain
8. Op amp power dissipation and output saturation
9. *I-V* converters
10. *V-I* Converters
11. Difference amplifiers and the CMRR
12. Instrumentation amplifiers
13. Transfer functions and Bode Plots
14. First-order filters
15. *KRC* filters
16. Multiple-feedback filters
17. State-variable filters
18. Biquad filters
19. Input bias and offset currents
20. Input offset voltage
21. Drift, PSRR, CMRR
22. Input error compensation
23. Open-loop and closed-loop gains versus frequency
24. Examples
25. Input and output impedances
26. Transient response
27. Slew-rate limiting and PSpice simulations
28. Voltage comparators
29. Comparator applications
30. Schmitt Triggers
31. Precision rectifiers
32. Systems concepts and oscillations
33. Sinewave generators
34. Free-running multivibrators

35. Monostable multivibrators
36. IC timers
37. Triangular wave generators
38. Waveshapers and sawtooth wave generators
39. VCOs

Notes on Evaluation:

1. No late homework accepted. Solutions to the homework assignments are posted in the solution window across Sci 144. For each assignment, two randomly selected problems are graded, each with a subjective grade of 0, 1, or 2 points.
2. All exams are closed book. One standard (8½” × 11”) double-sized sheet of notes allowed. *No electronic devices* (cellular phones, PDAs, iPODs, etc.) allowed, except for a basic calculator.
3. ***No make-up exams*** and ***no incomplete*** grades without a serious and verifiable medical justification. ***No changes*** in the exam dates, ***no exceptions***.
4. **Final exam:** Mon, Dec 21, 1:30-4:00 pm, in the lecture room.
5. Grading criteria (Example: 55% to 60% results in a grade of C):
   0<**F**<35<**D-**<40<**D**<45<**D+**<50<**C-**<55<**C**<60<**C+**<65<**B-**<70<**B**<75<**B+**<80<**A-**<85<**A**<100

Notes on Prerequisites:

Engineering students must have a copy of the course approval form on file. Non-engineering students must submit a copy of the grade report showing the appropriate course grade for ENGR 205 and 305 (if already completed).

Relationship to Other Courses:

Engr 442 is a required course of all EE majors. It complements the analog design viewpoint of Engr 445. While Engr 445 focuses on device design aspects of analog ICs, Engr 442 concentrates on systems design aspects and applications. Together, these courses are designed to provide the student with a fairly comprehensive undergraduate background in analog electronics with emphasis on design.