

San Francisco State University
Electrical Engineering

Course Outline for Engr 353 Electronics
Fall 2009

Bulletin Description:

Engr 353 Electronics (3)

F,S

Prerequisite: grades of C or better in Engr 205 and 206. Concurrent enrollment in Engr 301. PN diodes, BJTs, and MOSFETs. Semiconductor device basics, characteristics, and models. Diode applications. Transistor biasing, basic amplifier configurations, and basic logic circuits. PSpice simulation.

Textbooks:

1. Sergio Franco, *An Introduction to Microelectronics*, University Readers, 2009.
2. Larry Klingenberg, *Introduction to PSpice – A quick Guide to Using PSpice 9.2*, notes developed for the Engr 206 and Engr 301 labs. Visit also <http://online.sfsu.edu/~larryk>

References:

Sergio Franco, *Electric Circuits Fundamentals*, Oxford University Press, 1995.

Coordinator:

Sergio Franco, Professor of Electrical Engineering

Prerequisites by Topic:

1. Circuit analysis techniques (Ohm's law, KVL, KCL, and the superposition principle)
2. Ideal op amp circuits and the Op Amp Rule
3. Circuit equivalence and modeling concepts
4. Basic physics and electricity.
5. Familiarity with the basics of PSpice simulation

Course Objectives¹:

1. To study *pn* junction diodes and basic applications thereof [A1, A.2, B.1, B.4]
2. To study transistors (BJTs and FETs), as well as their applications as single-stage amplifiers and logic inverters [A.1, A.2, B.1, B.4]
3. To expose students to SPICE simulation of basic op amp, diode, and transistor circuits [B.3]

¹Indices in brackets refer to educational objectives and outcomes of the School of Engineering.

Topics:

1. Diodes: ideal diode characteristics and applications, physical operation of *pn* junctions, circuit analysis, dc and ac diode models, voltage references and dc power supply design. SPICE simulation
2. Bipolar junction transistors: physical operation, characteristics, models, biasing, single-stage amplifier configurations, switch and logic applications, SPICE simulation.
3. Field-effect transistors: physical operation, characteristics, models, biasing, single-stage amplifier configurations, CMOS inverters and switches, SPICE simulation

Professional Component:

1. Engineering Sciences: 67%
2. Engineering Design: 33%

Evaluation:

1. Thirteen homework assignments 6 problems each: 10% of overall grade
2. Three 1-hour, 4-problems midterm exams, 20% each (60% of overall grade)
3. One 2.5-hour, 5-problems final exam, 5 problems: 30% of overall grade

Performance Criteria:Objective 1

- 1.1 Students will become conversant with *pn* junction behavior and characteristics. [1, 2]
- 1.2 Students will demonstrate an ability to analyze diode circuits using graphical and iterative techniques as well as large-signal and small-signal models. [1, 2]
- 1.3 Students will demonstrate a knowledge of popular diode applications such as rectification, regulation, limiting, and clamping. [1, 2]
- 1.4 Students will become conversant with SPICE diode models. [1]

Objective 2

- 2.1 Students will become conversant with the physical structures of BJTs, and MOSFETs, as well as their electrical characteristics. [1, 2]
- 2.2 Students will demonstrate an ability to use large-signal models for the DC analysis and design of simple transistor circuits. [1, 2, 3]
- 2.3 Students will demonstrate an ability to use small-signal models for the analysis and design of basic single-stage amplifiers. [1, 2, 3]
- 2.4 Students will demonstrate an ability to analyze simple logic inverters using transistors. [1, 2, 3]
- 2.5 Students will become conversant with SPICE transistor models. [1]

Objective 3

- 3.1 Students will demonstrate a skill in running successful computer simulations of simple electronic circuits and compare with hand calculations. [1]

² Numbers in brackets refer to evaluation methods used to assess student performance.

Fall 09

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Class/Laboratory Schedule:

Three 50-minute lectures/week

Scheduled Coverage:

1. The Ideal Diode
2. Basic Diode Applications
3. More Diode Applications
4. Semiconductors and the *pn* Junction

5. The Space-Charge Layer and its Characteristics.
6. The Diode Equation
7. Breakdown and forward Diode Characteristics
8. Dc Analysis of pn Diode Circuits
9. Ac Analysis of pn Diode Circuits
10. Breakdown-Region Operation
11. Voltage Regulation
12. Dc Power Supplies

1st Midterm exam: Mon, Sept 28

13. BJT Device Structure
14. Basic BJT Properties
15. The i - v Characteristics of BJTs
16. Operating regions and BJT Models
17. Circuit Examples
18. The BJT as an Amplifier/Switch
19. Small-Signal Operation of the BJT
20. The BJT as a Resistance-Transformation Device
21. BJT Biasing for Amplifier Design

2nd Midterm exam: Wed, Oct 21

22. Basic BJT Amplifiers and the Common-Emitter Configuration
23. The Common-Emitter with Emitter-Degeneration Configuration
24. The Common-Collector and Common-Base Configurations
25. MOSFET Device Structure and the Threshold Voltage
26. The Channel's Characteristics
27. The i - v Characteristics of n MOSFETs
28. p MOSFETS, and Large-Signal MOSFET Models
29. MOSFETs in Resistive Dc Circuits
30. Dc Biasing of MOSFETs

3rd Midterm exam: Mon, Nov 16

31. The MOSFET as an Amplifier/Switch
32. The Noise Margins
33. Small-Signal Operation of the MOSFET
34. A Generalized MOSFET Circuit
35. Basic MOSFET Amplifier Configurations
36. MOSFET Amplifier Examples
37. The CMOS Inverter/Amplifier
38. CMOS Gates and Noise Margins
39. CMOS Amplifiers and PSpice Simulation

Final exam: Wed, Dec 16, 10:45 am – 1:15 pm in the lecture room

Notes on Evaluation:

1. No late homework accepted. Solutions to the homework assignments are posted in the solution window across Sci 144. For each assignment, two randomly selected problems will be graded, each with a subjective grade of 0, 1, or 2 points.
2. All exams are closed book. One standard (8½" × 11") double-sized sheet of notes allowed. *No electronic devices* (cellular phones, PDAs, iPods, etc.) allowed, except for a basic calculator.
3. **No make-up exams** and **no incomplete grades** without a *serious and verifiable medical justification*. **No changes** in the exam dates. **No exceptions**.
4. **Final exam:** Wed, Dec. 16, 10:45 am – 1:15 pm, in the lecture room.
5. Grading criteria (Example: 55% to 60% results in a grade of C):

0<F<35<D-<40<D<45<D+<50<C-<55<C<60<C+<65<B-<70<B<75<B+<80<A-<85<A<100

Notes on Prerequisites:

Engineering students must have a copy of the course approval form on file. Non-engineering students must submit a copy of the grade report showing the appropriate course grade for ENGR 205 and 206.

Relationship to Other Courses:

This course extends the introductory circuit coverage of Engr 205 to electronic devices (diodes and transistors.) It prepares the student for Engr 301, 442, 445, 453, and 455. Most of the Engr 353 material is put to use in the Engr 301 lab, which is taken concurrently with (or after) Engr 353. **Important note:** *If you are taking Engr 353 and Engr 301 concurrently, and decide to withdraw from Engr 353, you will automatically be dropped also from Engr 301.*