

# EFFICIENT POWER CLOCK GENERATION FOR ADIABATIC LOGIC

Hamid Mahmoodi-Meimand<sup>1</sup> and Ali Afzali-Kusha<sup>2</sup>

Department of Electrical and Computer Engineering, University of Tehran, Tehran, Iran

<sup>1</sup>mahmoodi@iee.org <sup>2</sup>afzali@chamran.ut.ac.ir

## ABSTRACT

Practical issues in the design of power clock generators needed by adiabatic logic circuits are explained. Synchronous and asynchronous power clock generators are designed for an 8-bit adiabatic carry look-ahead adder and the more energy efficient circuit for the power clock generation is determined to be the 2N synchronous power clock generator that exhibits conversion efficiency of 77% at 10MHz operating frequency.

## 1. INTRODUCTION

The supply voltage in adiabatic circuits in addition to providing the power to the circuit behaves as the clock of the circuit and for this reason is called power clock. One of the main concerns in the adiabatic logic circuits is the power clock generation. In these circuits the supply voltage is desired to be a ramping voltage, although, it can be approximated by a sinusoidal voltage that can easily be generated using resonant circuits. Some adiabatic logic families need multiphase power clocks for their cascade [1-6]. The design of an efficient power clock generator is a challenging problem in this field. Although some possible power clock generators have been proposed [4,6-10], most attention in the earlier works has been given to logic operation and performance [1-2,11-12] while power clock generators consume a large fraction of the total energy consumption in adiabatic circuits and cause the energy savings to be greatly degraded. To the best of our knowledge no report on the efficiency comparison of different configurations of power clock generators has been published in the literature. Here, we present a quantitative efficiency comparisons of different configurations of power clock generators for adiabatic circuits. In this paper, we design and compare some synchronous and asynchronous power clock generators for an adiabatic adder and determine the more efficient power clock generator. The paper is organized as follows: In Section 2 the adiabatic adder design is described. The design and comparison of synchronous and asynchronous power clock generator schemes are presented in Section 3 and, finally, Section 4 contains the summary and conclusions of the paper.

## 2. ADIABATIC ADDER DESIGN

The schematic diagram of the 8-bit Carry Look-ahead Adder (CLA) used for our adiabatic design is shown in Fig. 1. We have designed this adder based on Pass-transistor Adiabatic Logic (PAL) [1,13], which is a dual-rail adiabatic logic with a relatively low gate complexity that operates with a two-phase power clock. We have generated the layout of this design in a 0.6 $\mu$ m CMOS technology and extracted its netlist for simulation and power clock generator design. Each primary output was connected to a 50fF load.

## 3. POWER CLOCK GENERATION

In conventional dynamic digital circuits, power and clock lines are separate. The power is supplied through a DC supply voltage and

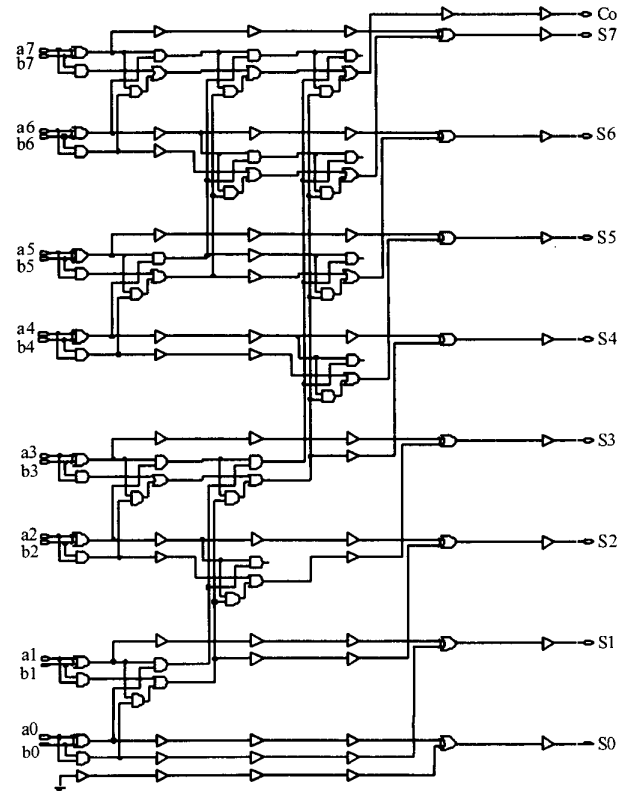


Figure 1. Schematic diagram of the 8-bit CLA

the clock is generated by a separate circuit and is usually a square waveform. In adiabatic circuits power and clock lines are mixed into a single power clock line, which has both the functions of powering and timing the circuit. Adiabatic logic circuits, therefore inherently operate in a pipelined and dynamic fashion. A DC to AC converter named power clock generator is needed for the generation of the power clock signal. Power clock generators usually consume the main fraction of the total energy consumed by the adiabatic system and degrades the energy savings obtained due to the energy recovery property of the adiabatic logic. The design of power clock generator, therefore, is an important part of the whole adiabatic system design. Inefficient power clock generations have become an obstacle to the adiabatic module integration into a VLSI system and, hence, power clock generators with high conversion efficiency are strongly desired. In order to evaluate the performance of a power clock generator, the conversion efficiency is defined as the ratio of the dissipated energy in the adiabatic core and the total delivered energy from the DC supply. Previous record showed a conversion efficiency of 41% in a relatively complex design [3].

Two methods have been developed for power clock generation: stepwise charging [14] and resonant charging [7] where the latter is simpler, more efficient, and commonly used and thus we use this approach. The LC resonant circuit, which performs like a colpitts-type oscillator, is suitable for a power clock generator. Since the on-chip inductors do not lead to a high  $Q$  inductor, on-chip inductors may not be used for power clock generation. An external high  $Q$  inductor is therefore used for energy recovery. The  $C$  component is the distributed capacitance of the power clock line and its connected logic circuits all over the chip. The LC product determines the oscillation frequency of the power clock generator. In order to have a stable frequency of oscillation, the equivalent on chip capacitance should be constant and data independent which is achieved in the adiabatic logic circuits due to their differential nature. The first step in designing the power clock generator for an adiabatic circuit is circuit modeling to determine the equivalent capacitance. This concept is described in the following section and illustrated by the example of our adiabatic CLA.

### 3.1 Adiabatic Logic Model

Adiabatic logic presents a capacitive load to the power clock generator. For each phase, an approximate lumped-element model of the logic includes an equivalent capacitor  $C$  to model energy storage, in series with a resistor  $R$  to model the losses. By using the differential logic, as in the case of PAL, the equivalent capacitance becomes approximately independent of the logic states or the logic activity. This simplifies the design of power clock generators based on resonant power conversion technique. The values of the model parameters,  $R$  and  $C$ , can be extracted from the simulation tests where an external ideal sinusoidal voltage source is applied as the power clock. For a given clock frequency,  $f_c$ , and a logic activity, the power loss,  $P_L$ , in the logic, and the rms current  $I_L$  supplied to the logic by the power clock can be found from the test. For the purpose of power clock design, the test should be performed for the logic activity that corresponds to the worst-case losses. Given  $P_L$  and  $I_L$ , the model parameters can be found as [9]:

$$R = \frac{P_L}{I_L^2} \quad (1)$$

$$C = \frac{\sqrt{2}I_L}{\pi V_{DD}f_c} \quad (2)$$

where  $V_{DD}$  is the peak value of the applied power clock. We have performed this test for our adiabatic CLA and extracted the

equivalent  $R$  and  $C$  for each power clock phase in the frequency range of 10 MHz to 100MHz. The results have been summarized in Table 1 where the tests were performed for the maximum logic activity of the circuit. As expected the equivalent capacitance is relatively independent of the clock frequency ( $\approx 5$ pF), while the resistive component decreases with increasing the clock frequency.

### 3.2 Integrated Resonant Power Clock Generators

Various circuit topologies for resonant energy recovery have been proposed for different adiabatic logic styles and for different applications [4,6-10]. They can be classified into two main groups: asynchronous and synchronous power clock generators. Asynchronous power clock generators are free running circuits that use feedback loops to self-oscillate without any external timing signals. Fig. 2 illustrates two commonly used asynchronous power clock generators: 2N and 2N2P power clock generators [4,7]. They are simple dual-rail LC oscillators whose active elements are cross-coupled pairs of NMOS and PMOS transistors. Many problems are associated with asynchronous structures. Their oscillation frequencies are sensitive to their capacitive load variations in different cycles of the system operation resulting in unstable frequency problems. In addition, they can not be used for the generation of 4, 8 and more phase shifted power clocks needed in some adiabatic circuits [3-6]. Finally, in large systems, inputs and outputs of each module must be in synchronization with other modules prohibiting the integration of the adiabatic module driven by asynchronous power clock generators into a larger non-adiabatic system. Using phase-locked loops or synchronizers such as self-timed first-in-first-out (FIFO) memories, would not be energy and area efficient solutions to this problem. In these cases, the synchronous power clock generators can be utilized as an efficient solution without having any of the above problems. Synchronous power clock generators are synchronized to external timebase signals usually available in large systems. Fig. 3 illustrates two synchronous power clock generators similar to the asynchronous counterparts except that the gate control signals are derived externally. The capacitors  $CE1$  and  $CE2$  in Fig. 2 and 3, are external balancing capacitors to achieve more conversion efficiency. The adiabatic module can be easily synchronized to a larger conventional non-adiabatic system by using synchronous power clock generators. Level to pulse and pulse to level converters which are simple latch structures, can be used for interfacing between adiabatic and conventional circuits [15]. We will also show that the synchronous power clock generators are more energy efficient than the asynchronous ones.

**Table 1.** Results of modeling the adiabatic CLA for  $V_{DD}=3.3V$

$f_c$ [MHz]	Phase#1				Phase#2			
	$P_L$ [ $\mu$ w]	$I_L$ [ $\mu$ A]	$R_L$ [ $\Omega$ ]	$C_L$ [pF]	$P_L$ [ $\mu$ w]	$I_L$ [ $\mu$ A]	$R_L$ [ $\Omega$ ]	$C_L$ [pF]
10	20.9	355.3	166	4.85	34.23	385	231	5.25
20	57.4	704	116	4.8	91.67	761	158	5.19
30	104.9	1050	95	4.77	164.7	1126	130	5.12
40	163	1377	86	4.7	250.9	1489	113	5.08
50	229.8	1715	78	4.68	348.8	1834	104	5
60	364.2	2092	83	4.75	453.6	2222	92	5
70	390.5	2413	67	4.7	537.9	2561	82	5
80	478.6	2758	62.9	4.7	645.8	2911	76	4.96
90	585.3	3123	60	4.7	763.5	3280	70	4.97
100	701.4	3415	60	4.66	821	3598	63	4.91

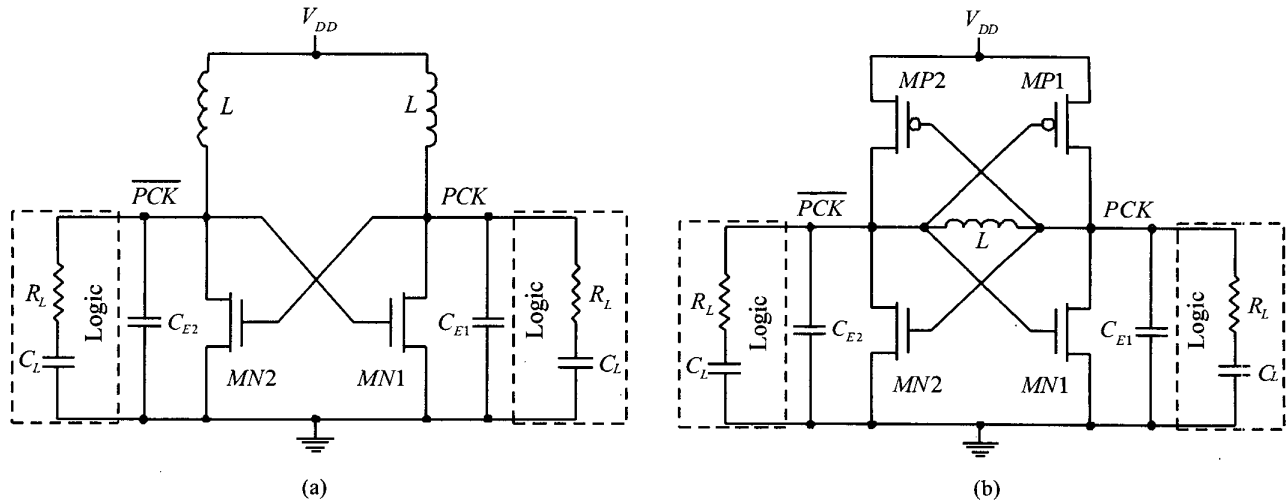


Figure 2. Asynchronous two phase power clock generators: (a) 2N (b) 2N2P

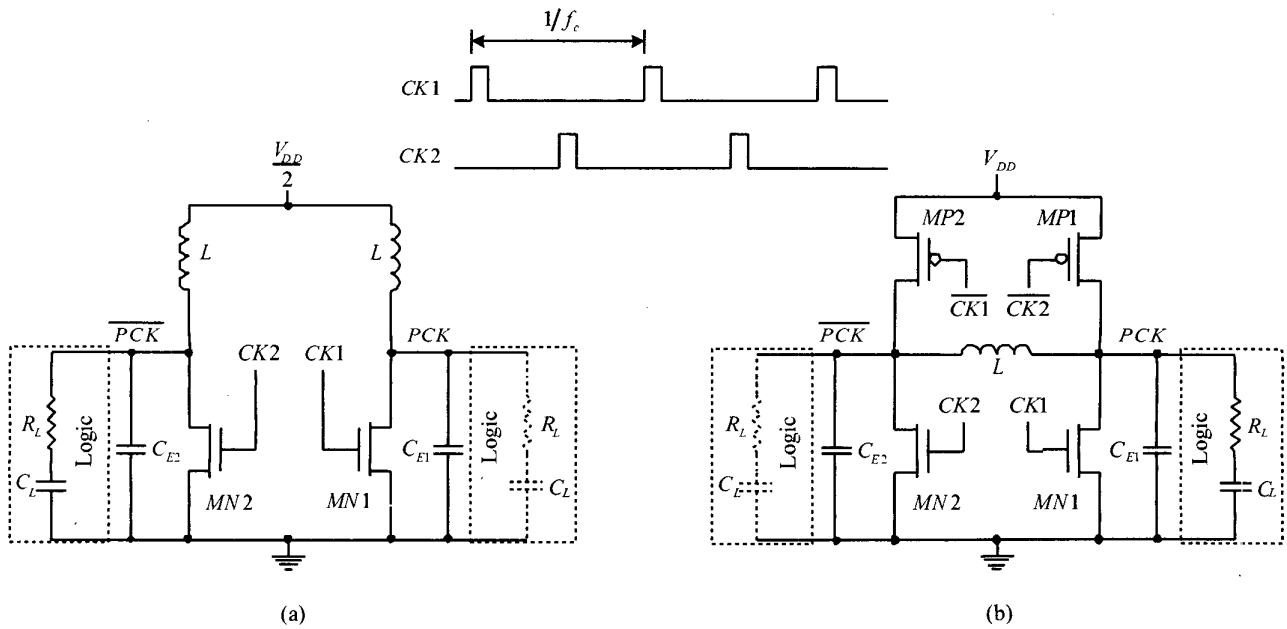


Figure 3. Synchronous two phase power clock generators: (a) 2N (b) 2N2P

Table 2. Power dissipation summary of the adiabatic CLA with different power clock generators at 10MHz operating frequency and 3.3V supply voltage

Power Clock Generator	Asynchronous		Synchronous	
	2N	2N2P	2N	2N2P
Power Dissipation of ACLA Core	62 $\mu$ w	61 $\mu$ w	58 $\mu$ w	57 $\mu$ w
Power Dissipation of DC-to-AC Converter	66 $\mu$ w	77 $\mu$ w	17 $\mu$ w	26 $\mu$ w
<b>Total Delivered Power</b>	<b>128<math>\mu</math>w</b>	<b>138<math>\mu</math>w</b>	<b>75<math>\mu</math>w</b>	<b>83<math>\mu</math>w</b>
<b>Conversion Efficiency</b>	<b>48%</b>	<b>44%</b>	<b>77%</b>	<b>69%</b>

### 3.3 Power Clock Design

We design all four power clock generators for the adiabatic CLA, at 10MHz operating frequency and 3.3V supply voltage, and compare the power dissipation and conversion efficiency. We first model the adiabatic circuit for which the power clock generator should be designed. The adiabatic logic modeling was described in section 3.1 and the results were summarized in Table 1 for the adiabatic adder. Using these results, we design each of the power clock generators by placing simple resistors and capacitors equal to the extracted values instead of the adiabatic adder. Then this simple circuit can be quickly designed and simulated to find the optimum design. The value of  $L$  is determined by the required frequency and the extracted capacitance. The oscillating frequency for the 2N power clock generators is determined by [16]:

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (3)$$

and for the 2N2P power clock generators is determined by:

$$f = \frac{1}{2\pi\sqrt{L\left(\frac{C}{2}\right)}} \quad (4)$$

where  $C$  is the equivalent capacitance of each phase. The slight differences in the equivalent capacitance of the phases are due to the large capacitors of 50fF placed on each output bit line derived by the /PC resulting in greater equivalent capacitance on this phase. The slight difference should be compensated by the balancing capacitors  $C_{E1}$  and  $C_{E2}$  to achieve higher conversion efficiency. In our simulation, we place small resistors in series with the inductors to model the limited  $Q$  of the inductors, which was assumed to be 100. After simulating and optimizing the power clock generator with the simple RC model, the designed power clock generator is connected to the adiabatic CLA and simulated again. In this stage, slight modifications may be needed to optimize the design for the highest achievable conversion efficiency. The results, summarized in Table 2, indicate that with synchronous power clock generators larger conversion efficiencies can be achieved. Between the two synchronous schemes, the 2N power clock generator is simpler, more energy efficient, and resulting in the higher conversion efficiency of 77%.

### 4. SUMMARY AND CONCLUSION

Many problems are associated with asynchronous power clock generators such as unstable frequency problems due to the sensitivity of their oscillation frequencies to their capacitive load variations in different cycles of the system operation, and their disability for the generation of 4, 8 and more phase shifted power clocks needed in some adiabatic logic circuits. The synchronous power clock generators can be utilized as an efficient solution without having any of the above problems. Synchronous power clock generators are synchronized to external timebase signals usually available in large systems. Moreover, we also showed that the synchronous power clock generators are more energy efficient than the asynchronous ones. Different asynchronous and synchronous power clock generators were designed for an adiabatic carry look-ahead adder and the results concluded that the synchronous 2N power clock generator was the more efficient

power clock generator that showed the conversion efficiency of 77% at 10MHz operating frequency.

### 5. REFERENCES

- [1] V. G. Oklobdzija, D. Maksimovic, and F. Lin, "Pass-transistor adiabatic logic using single power clock supply," *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 44, no. 10, pp. 842-846, Oct. 1997.
- [2] C.K. Lo and P. C. H. Chan, "An adiabatic logic for low-power digital systems," *IEEE Tr. on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 46, no. 9, pp. 1245-1250, Sep. 1999.
- [3] Y. Moon and D. K. Jeong, "An efficient charge recovery logic circuit," *IEEE J. Solid-State Circuits*, vol. 31, no. 4, pp. 514-522, Apr. 1996.
- [4] A. G. Dickinson and J. S. Denker, "Adiabatic Dynamic Logic," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 311-315, Mar. 1995.
- [5] S. G. Younis and T. F. Knight, "Asymptotically zero energy split-level charge recovery logic," in *Proc. Int. Workshop on Low Power Design*, Napa Valley, California, pp. 177-182, 1994.
- [6] J. Lim, D. G. Kim, and S. I. Chae, "A 16-bit carry-lookahead adder using reversible energy recovery logic for ultra-low-energy systems," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 898-903, Jun 1999.
- [7] W. C. Athas, L. J. Svensson, and N. Tzartzanis, "A resonant signal driver for two-phase, almost-non-overlapping clocks," *IEEE Symp. Circuits and Systems*, vol. 4, pp. 129-132, 1996.
- [8] Y. Moon and D. K. Jeong, "A  $32 \times 32$ -b adiabatic register file with supply clock generator," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 696-701, May 1998.
- [9] D. Maksimovic and V. G. Oklobdzija, "Integrated power clock generators for low energy logic," *IEEE Power Electronics Specialists Conf.*, vol. 1, pp. 61-67, 1995.
- [10] S. G. Younis and T. F. Knight, "Non-dissipative rail drivers for adiabatic circuits," in *Proc. of Conf. on Advanced Research in VLSI*, pp. 404-414, 1995.
- [11] S. Kim and M. C. Papaefthymiou, "True single-phase energy-recovering logic for low-power, high-speed VLSI," *Proc. of International Symp. on Low-Power Electronics and Design*, pp. 167-172, Aug. 1998.
- [12] S. Kim and M. C. Papaefthymiou, "Single-phase source-coupled adiabatic logic," *Proc. of International Symp. on Low-Power Electronics and Design*, pp. 97-99, Aug. 1999.
- [13] H. Mahmoodi-Meimand, A. Afzali-Kusha, and Mehrdad Nourani, "Efficiency of adiabatic logic for low-power, low-noise VLSI," To be presented in *IEEE Midwest Symp. on Circuits and Systems*, Aug. 2000.
- [14] L. J. Svensson and J. G. Koller, "Driving a capacitive load without dissipating  $fCV^2$ ," *IEEE Symp. Low Power Electronics*, pp. 100-101, 1994.
- [15] N. Tzartzanis and W. C. Athas, "Clocked-powered CMOS: a hybrid adiabatic logic style for energy-efficient computing," in *Proc. 20<sup>th</sup> anniversary conf. on advanced research in VLSI*, pp. 137-151, 1999.
- [16] N. Tzartzanis and W. C. Athas, "Energy recovery for the design of high-speed, low-power static RAMs," *Int. Symp. on Low Power Electronics and Design*, pp. 55-60, 1996.