Low-Power Scan Design Using First-Level Supply Gating

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***Abstract*—Reduction in test power is important to improve battery lifetime in portable electronic devices employing periodic self-test, to increase reliability of testing, and to reduce test cost. In scan-based testing, a significant fraction of total test power is dissipated in the combinational block. In this paper, we present a novel circuit technique to virtually eliminate test power dissipation in combinational logic by masking signal transitions at the logic inputs during scan shifting. We implement the masking effect by inserting an extra supply gating transistor in the supply to ground path for the first-level gates at the outputs of the scan flip-flops. The supply gating transistor is turned off in the scan-in mode, essentially gating the supply. Adding an extra transistor in only one logic level renders significant advantages with respect to area, delay, and power overhead compared to existing methods, which use gating logic at the output of scan flip-flops. Moreover, the proposed gating technique allows a reduction in leakage power by input vector control during scan shifting. Simulation results on ISCAS89 benchmarks show an average improvement of 62% in area overhead, 101% in power overhead (in normal mode), and 94% in delay overhead, compared to the lowest cost existing method.**

***Index Terms*—Low power test, scan design, supply gating.**

I. Introduction

POWER dissipation during test mode can be significantly higher than that during functional mode, since the input vectors during functional mode are usually strongly correlated compared to statistically independent consecutive input vectors during testing. Zorian [1] showed that the test power could be twice as high as the power consumed during the normal mode. Test power is an important design concern to increase battery lifetime in hand-held electronic devices that incorporate built-in self test (BIST) circuitry for periodic self-test. It is also important to improve test cost, since reduced test power of a module allows parallel testing of multiple embedded cores in an IC [7]. Increased peak power is likely to create noise problems in a chip by causing a drop in the supply voltage [9]. Peak and average power reduction during test contributes to enhanced reliability of the test and improvement of yield [11]. It is, therefore, important to ensure reduction in power dissipation during the test mode.

Scan architectures represent the prevalent Design for Testability (DFT) approach to test digital circuits [9]. During test application in a scan-based circuit, power is dissipated in both the sequential scan elements and in the combinational logic. While scan values are loaded into a scan chain, the effect of scan-ripple propagates to the combinational block and redundant switching occurs in the combinational gates during the entire scan-in/out period. It is observed that about 78% of total test energy is dissipated in the combinational block alone [10]. Hence, a low-power scan design should address techniques to reduce power dissipation in the combinational block.

There has been multitude of research exploring efficient techniques to reduce test power in scan-based circuits. Wang *et al.* proposed automatic test pattern generation technique to redesign test vectors for reducing power dissipation during scan testing [4]. With their automatic test pattern generation (ATPG), redundant transitions in combinational logic can be reduced but not completely eliminated. Moreover, test application time may increase to trade off power. Scan-latch reordering [5] or input vector reordering [6] techniques have been proposed for reduction in test power. However, these techniques target reduction of transitions at the output of scan flip-flops and cannot eliminate redundant switching in combinational block. In [7], Whetsel provided a solution for reduction in average and peak power dissipation by transforming conventional scan architecture into desired number of selectable, separate scan paths. Each scan path is in turn filled with stimulus and emptied of response. Sankaralingam *et al.* [8] proposed a solution to the peak power problem during external testing by selectively disabling the scan chain. In this scheme, the test-set is generated and ordered in such a way that only changing portions of consecutive tests are shifted into the scan chains. In [11] and [12], the authors provide a solution to prevent peak power violation during both shift and capture cycle using scan chain partitioning. However, the modification of the scan flip-flop in [12] results in a substantial increase in area and degradation in performance. Redundant power loss in combinational logic is not completely prevented in the above cases, since part of the scan chain is always active during shifting.

Inserting blocking logic into the stimulus path of the scan flip-flops [as shown in Fig. 1(a)] to prevent propagation of scan-ripple effect to logic gates offers a simple and effective solution to significantly reduce test power, independent of test set. Werstendorfer *et al.* have proposed NOR or NAND gate-based blocking method in [10]. Blocking gates (of type NOR or NAND) are controlled by the test enable signal [as in Fig. 1(b)], and the stimulus paths remain fixed at either logic “0” or logic “1” during the entire scan shift operation. Zhang *et al.* [14] have used multiplexers at the output of the scan cells [Fig. 1(b)], which hold

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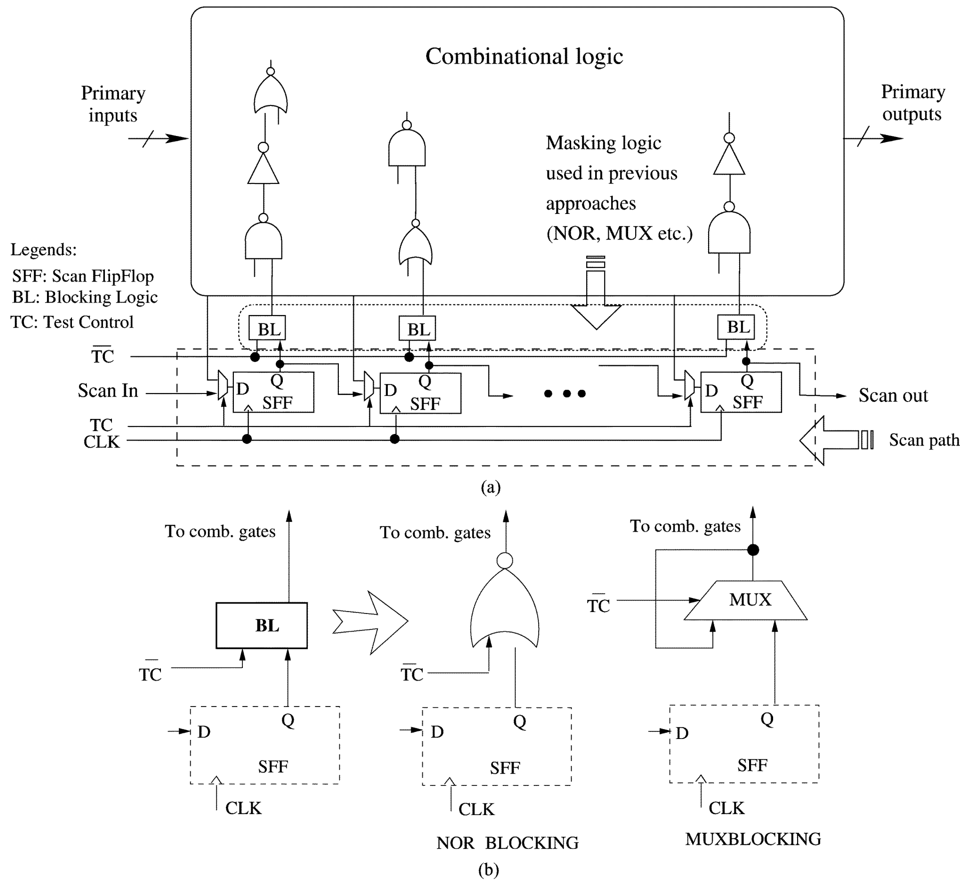

Fig. 1. (a) Scan architecture with existing blocking circuitry to reduce power during scan operation. (b) Blocking logic.

the previous states of the scan register during shifting and, thus, prevent activity in combinational logic. Another method for reduction in combinational power using blocking is to use a scan-hold circuit as a sequential element. This technique is called enhanced scan [9], which also helps in delay fault testing by allowing application of arbitrary two-pattern test. In a scan-hold design, each sequential element contains an additional storage cell called the hold latch, and the stimulus path for the combinational part is connected to the output of the hold latch, which is not used in scan shifting. Therefore, it also prevents redundant switching in combinational logic.

The problem with the blocking logic is that it adds significant delay in the signal propagation path from the scan flip-flop to logic [10]. Moreover, they have large overhead in terms of area and switching power in normal operation of the circuit. In this paper, we present an elegant signal blocking technique, which is referred as **First-Level Supply (FLS) gating**, to reduce power dissipation in the combinational logic during scan shifting. This is achieved by inserting a supply gating transistor in the first level of logic connected to the scan cell outputs, which essentially "gates" the VDD or GND line. The proposed method is as effective as the other blocking methods in terms of reducing peak power and total energy dissipation during scan testing. However, since we introduce just one transistor in the charge/discharge path of the first level logic, the delay penalty is significantly reduced compared to other blocking methods, which insert additional level of logic into signal propagation path. The overhead incurred in die-area and switching power in normal mode due to extra discrete Fourier transform (DFT) logic is also significantly lower than the existing methods using NOR [10], MUX [14], and Hold-latch [9]. The area overhead for FLS, however, depends on number of unique first-level fanout gates. We have also presented a low-complexity algorithm to reduce fanouts of the scan flip-flops under delay constraint, which helps to further reduce the area overhead in FLS.

Besides saving dynamic power in the combinational logic during test application, FLS can also be used to reduce leakage power by input vector control (IVC) mechanism [16]. With technology scaling, leakage power is becoming a notable source of power dissipation. We have demonstrated that FLS can be easily adapted to reduce leakage power in the combinational part during scan testing without any extra hardware or control signal. Based on the advantage of leakage reduction, we have shown that FLS even achieves improvement in total test power compared to other blocking methods. Since leakage increases exponentially with technology scaling, we can obtain about 25% improvement in total test power in a 45-nm technology node compared to a NOR-based blocking scheme.

The rest of the paper is organized as follows: Section II illustrates the proposed gating technique for saving energy in the combinational block during scan shifting. Section III presents experimental results in terms of area, delay, and power for a set of ISCAS89 benchmark circuits. Section IV explains power dissipation in test mode and presents a technique to reduce leakage

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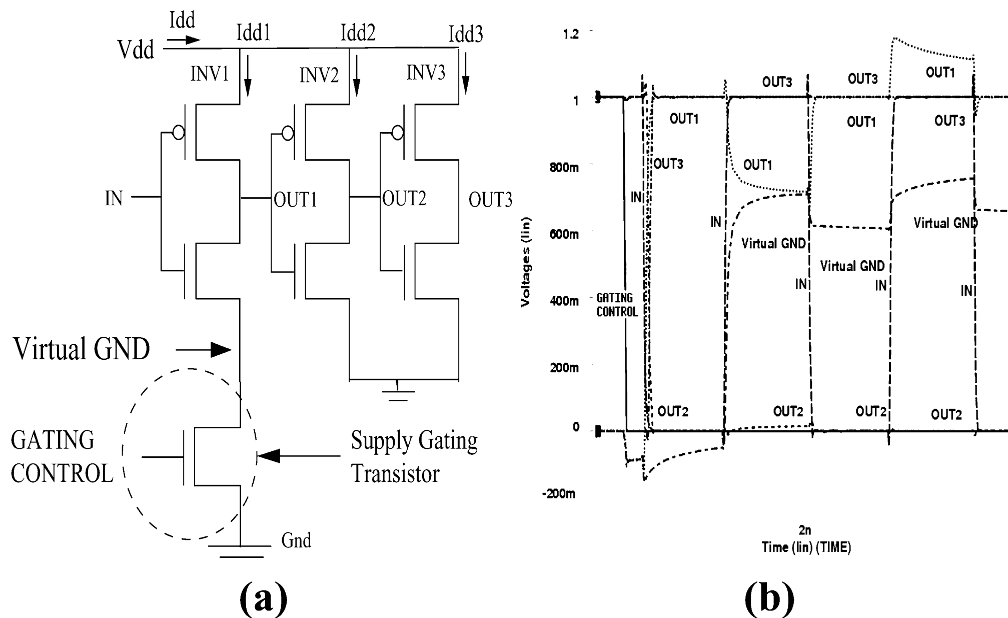

Fig. 2. (a) Use of FLS gating transistor in combinational part. (b) Transient response in 70 nm.

power using FLS. Section V discusses further scope for optimizing DFT overhead and test power, and Section VI discusses important test issues associated with the proposed technique. Section VII concludes the paper.

II. FLS Gating for Power Reduction in Scan Mode

The dynamic power dissipation in the combinational circuit can be reduced by lowering the activity of the circuit. Previous works on low power scan design target reducing the activity of the circuit by gating the inputs of the combinational block with the use of extra logic gates (latch [9], multiplexer [14], NOR [10], etc.). However, these techniques have a negative impact on circuit performance and considerably add to the total area. Moreover, they impose significant power overhead during the normal mode of operation of the circuit. In this section, we have described a novel methodology based on supply gating to reduce power dissipation in the combinational circuit during the scan shift cycles.

A. Supply Gating Transistor for Reducing Active Power in Scan Mode

Although global supply gating transistor prevents propagation of switching activity in the combinational block, it results in considerable area and delay overhead. To overcome the overhead associated with the global supply gating transistor, we have proposed a novel FLS gating technique, where only the first-level logic gates connected to the scan flip-flops are gated using supply gating transistors [Fig. 2(a)]. Insertion of the supply gating transistor in the first level logic will screen the rest of the combinational logic from the state-input (scan-input) transitions (except only one transition—a "1" to "0" if NMOS supply gating and "0" to "1" in PMOS supply gating). This can be observed in Fig. 2(b) from which it can be understood that the first transition at the input IN from "1" to "0" will charge the OUT1 to VDD. This transition will propagate throughout the inverter chain. However, any further transition in the input (i.e., from "0" to "1") will not propagate, as the OUT1 cannot be discharged [Fig. 2(b)]. This significantly reduces the redundant activity of the circuit during the scan-shift operation.

The principal issue associated with FLS scheme shown in Fig. 2 is that the outputs of the first level gates are floating if they are at logic "0" (connected to the virtual ground). The voltage of a floated output is determined by the leakage balance between the pull-up PMOS and pull-down NMOS network of the gate. Moreover, crosstalk noise or transient effect due to soft error can easily change the voltage of a floated output. If the voltage of the output of a first-level gate is not exactly at VDD or GND, this could cause static short circuit current on the following logic gates being driven by the first level gate. This particularly becomes more of an issue in deep submicron technologies due to increased leakage and noise.

In order to avoid such an issue, the outputs of the first-level gates need to be forced at VDD or zero in the supply gating mode. If the GND is gated as in Fig. 2, then the outputs of the first-level gates can be forced to VDD by a pull-up PMOS driven by the Gating Control (GC) signal. If the VDD is gated, then the outputs of the first level gates can be forced to ground using NMOS pull-down transistors driven by the GC signal. The general schemes of the proposed supply gating are shown in Fig. 3. In order to evaluate and compare these two schemes [Fig. 3(a) and (b)], they are applied to NAND and NOR gates. The pull-up (pull-down) transistor is kept at minimum size to optimize its impact on circuit delay and power during normal mode of operation. Fig. 4 shows the delay comparisons of the gated-VDD and gated-GND circuits. As expected, for the same size of the supply gating transistor, the gated-GND circuit is faster than the gated-VDD circuit for both NOR and NAND gates. This is because NMOS transistors are faster than PMOS transistors of the same size. It is also observed that as the size of the supply gating transistor is increased, the delay of the circuit is reduced and gets closer to the delay of the circuit without any gating. However,

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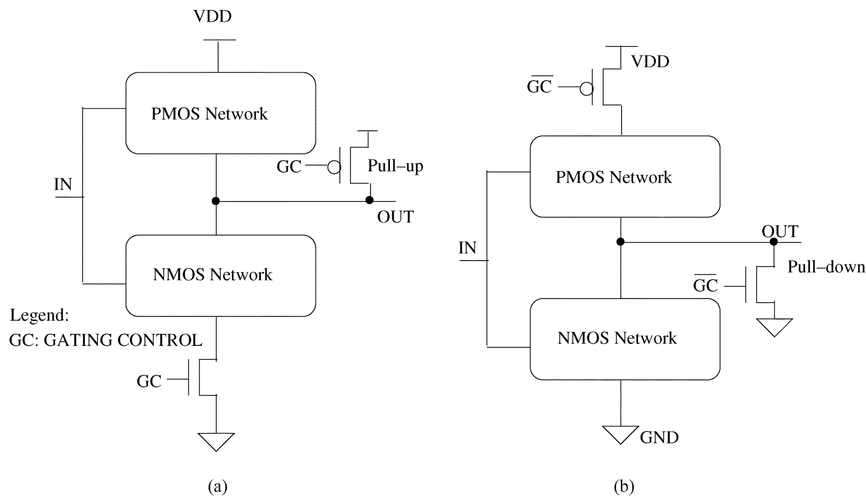

Fig. 3. Proposed supply gating schemes. (a) GND-gating. (b) VDD-gating.

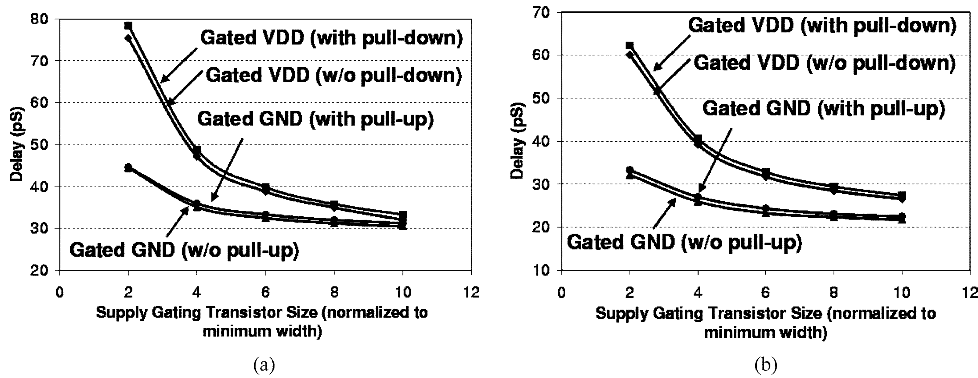

Fig. 4. Delay comparison of gated-VDD and gated-GND for (a) NOR gate and (b) NAND gate.

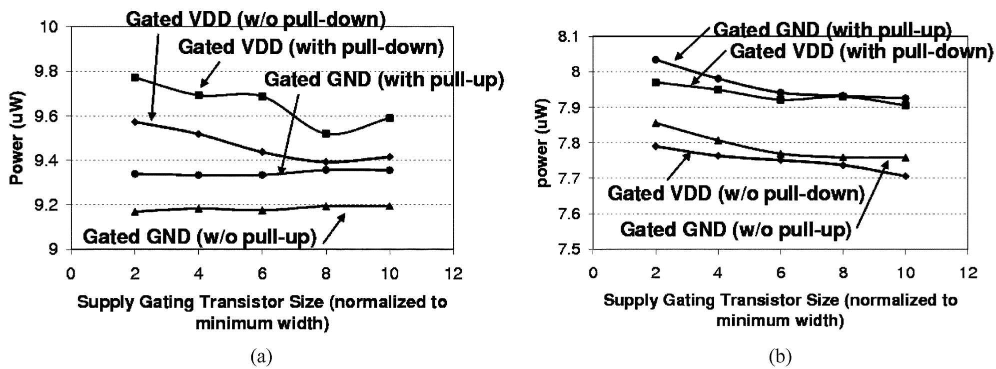

Fig. 5. Power comparison of gated-VDD and gated-GND for (a) NOR gate and (b) NAND gate.

increasing the transistor width for the supply gating transistor does not help much for delay improvement beyond some point. As observed from the plots in Fig. 4, for 2-input NAND and NOR gates, a supply gating transistor of six times the minimum size is a reasonable choice for minimal delay impact and small area overhead. Another point observed from Fig. 4 is that the impact of pull-up (pull-down) transistor on delay is negligible. Fig. 5 shows the power comparisons in the active mode for both the NAND and NOR gates. For the NAND gate, there is not much difference in the power of the gated-VDD and gated-GND cases. However, for the NOR gate, the gated-GND circuit shows less power consumption due to fewer transistors in the stack, 'and, therefore, fewer intermediate node capacitances. From these results, it can be inferred that the gated-GND is more suitable for gating due to smaller area overhead and less delay and power penalties. Table I compares the area, delay, and power overhead among several gating techniques, including FLS. We can observe from Table I that compared to latch and MUX-based gating, FLS is superior with respect to all three design parameters (area, delay, and power).

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TABLE I
COMPARISON OF AREA, DELAY, AND POWER AMONG ALTERNATIVE GATING TECHNIQUES APPLIED TO A SINGLE INVERTER

	Latch	MUX	NOR	**FLS**
Area (um^2)	00.49	00.31	00.27	**00.19**
Delay (pS)	59.91	90.38	42.56	**22.47**
Power (uW)	22.23	19.37	12.40	**07.93**

B. Scan Design Using FLS

Fig. 6 shows the proposed FLS gating techniques applied to a general circuit. This scheme completely eliminates switching activity in the combinational circuit during scan shifting. To implement the proposed supply gating scheme in a scan architecture, two approaches can be taken: In one case, the first-level gates have separate supply gating transistors [Unshared FLS; see Fig. 6(a)], and in the other case, all the first-level gates share a single supply gating transistor [Shared FLS; see Fig. 6(b)]. The area overhead is mostly due to the active area taken by supply gating transistors. By sharing the supply gating transistors, area overhead can be reduced because a shared supply gating transistor can have less size than the sum of the sizes of all supply gating transistors in the unshared case. In the Unshared FLS, the size of the supply gating transistor is chosen to be ten times the minimum transistor size, regardless of the type of the gate ($W_{\rm supplygating} = 10 * W_{\rm min}$). Statistically speaking, for random input data patterns, we can assume that approximately half of the first-level gates are switching at a time, while the rest do not experience any switching. Therefore, the supply gating transistors of the idle gates are not actually used, and the size of the supply gating transistor in case of Shared FLS can be half the sum of the sizes of all supply gating transistors in the Unshared FLS. Based on this argument, the size of the supply gating transistor in the Shared FLS case is given by

$$W_{\rm gating} = 0.5 * FO * (10 * W_{\rm min}) = 5 * FO * W_{\rm min} \quad (1)$$

where FO is the number of first-level gates in the combinational circuit. Therefore, by sharing the supply gating transistor, the area overhead due to supply gating transistor is reduced by half.

III. EXPERIMENTAL RESULTS AND COMPARISONS

To estimate the effectiveness of the FLS scheme, we simulated a set of ISCAS89 benchmark circuits and obtained power and performance in normal mode of operations and area overhead due to additional DFT logic in case of FLS, NOR-based, MUX-based, and latch-based gating. The simulation was performed in the 70-nm Berkeley Predictive Technology Model (BPTM) [15] to observe the effect of gating in a sub-100-nm scaled technology. The gate-level netlists were first technology-mapped to a *LEDA* 0.25-μ standard cell library [21] using a Synopsys design compiler with the mapping effort at medium [19]. The library contains complex gate types, e.g., "aoi" (and-or-invert) and "mux." and hence, the total number of logic gates is reduced from that in the original benchmark. The benchmark circuits are then translated to *Hspice* and scaled to 70 nm. Power is measured in *NanoSim* [20] by applying 100 random vectors to the inputs, and delay is measured by *Hspice* simulation of the critical paths of a circuit. Tables II–IV show comparisons of the proposed gating techniques with the existing techniques. In these tables, the advantage of our technique is shown in terms of percentages of improvement over the NOR-based gating. The percentage of improvement is calculated as the percentage of reduction in overhead from the NOR-based technique ($ov_{\rm NOR}$) to our technique ($ov_{\rm FLS}$) [see (2)].

$$\text{percent improvement} = 100 * \frac{(ov_{\rm NOR} - ov_{\rm FLS})}{ov_{\rm NOR}}. \quad (2)$$

Table II shows comparisons of these techniques in terms of area overhead. Since the layout rules for the 70-nm node are not available, the measure used for area is the total transistor active area ($W * L$ for a transistor). As explained earlier, by sharing the gating transistors in the Shared FLS case, the area overhead can be reduced by nearly half compared to the Unshared FLS, since pull-up PMOS transistors are minimum sized. The latch is the largest gating circuit, and therefore, the latch-based gating circuit has the largest area overhead followed by the MUX-based gating technique. The NOR-based gating has the least area penalty among the existing gating techniques. The proposed Shared FLS gating technique exhibits the smallest area overhead for all benchmark circuits (2.7% on an average). It shows 48% to 80% reduction in area overhead (with an average of 62%) as compared to the existing NOR-based gating technique, which has the least area penalty among the alternative techniques. It can be noted that for the NOR, MUX, or Latch-based method, area overhead is proportional to the number of scan flip-flops, since blocking logic is introduced at the output of each scan flip-flop [Fig. 1(a)]. However, in FLS, gating logic is inserted in all first-level gates [Fig. 6(a)], the number of which depends on the number of unique fanout gates of the scan flip-flops. Therefore, for a circuit with large number of fanouts for the scan flip-flops, such as s838, improvement in area overhead may not be significant (Table II). However, the number of fanouts of a scan flip-flop is usually not high (2.3 on average as can be obtained from column 2 and 3) to satisfy delay constraint of a circuit (since higher fanout means higher load at the output of a gate and, hence, higher delay). Due to overlapping of fanout cones, the number of unique fanouts of the scan flip-flops, i.e., the number of first-level gates (as shown in column 4), is further less (1.8 on average per scan flip-flop compared to 2.3 of total fan-out).

Table III shows comparative impact of the existing and proposed gating techniques on circuit delay for different benchmark circuits. As observed from Table III, the proposed technique has the least impact (minimal increase) on circuit delay. The MUX-based gating has the largest increase in delay. The latch-based gating shows the second largest increase in delay, and the NOR-based gating has the least delay penalty among existing techniques. Compared to the NOR-based gating, which has the least delay penalty among existing techniques, FLS exhibits circuit delay reduction of up to 8%. In fact, as observed from Table III, the delay overhead of the FLS technique is less than 1.3% for all the benchmark circuits. Another point to notice is that the delay of the NOR-based gating would be more if the logic polarity at the input of combinational block needs to be preserved. Since introduction of a NOR gate inverts the logic

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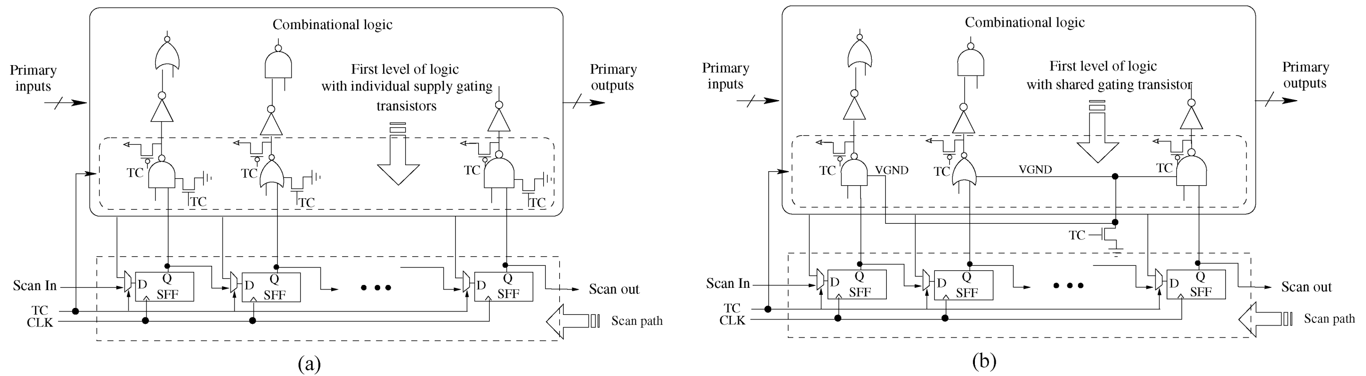

Fig. 6. Low-power scan architecture using FLS. (a) Unshared supply gating transistor. (b) Shared supply gating transistor.

TABLE II
COMPARISON OF PERCENTAGE AREA INCREASE

Ckt.	# of Flip-flops	# of first-level fanouts: Total fanouts	unique fanouts (Ratio*)	% of area increase with: Latch gating	MUX gating	NOR gating	FLS (Unshared)	FLS (Shared)	Improvement over NOR (%)
S298	14	46	35 (2.5)	15.10	13.74	6.86	6.55	3.57	47.91
S344	15	36	32 (2.1)	14.83	13.49	6.74	5.49	3.00	55.55
S641	19	19	19 (1.0)	14.24	12.95	6.47	2.47	1.35	79.17
S838	32	128	96 (3.0)	14.35	13.05	6.52	7.47	4.08	37.50
S1196	18	24	23 (1.3)	8.17	7.43	3.71	1.81	0.99	73.38
S1423	74	185	160 (2.2)	15.07	13.71	6.85	5.66	3.08	54.95
S5378	179	410	280 (1.6)	15.67	14.25	7.12	4.26	2.32	67.41
S9234	211	635	445 (2.1)	14.98	13.62	6.81	5.48	2.99	56.06
s13207	638	1166	729 (2.1)	26.75	24.33	12.16	5.31	2.89	76.19
s15850	534	1152	837 (1.1)	22.65	20.61	10.30	6.16	3.36	67.34
s35932	1728	4272	2692 (1.6)	16.80	15.28	7.64	4.54	2.48	67.54

*Ratio = Ratio of the unique fanouts to number of flip-flops

TABLE III
COMPARISON OF PERCENTAGE INCREASE IN DELAY

Ckt.	Crit. path logic gates	% of delay increase with: Latch	MUX	NOR	FLS Un-shared	FLS Sha-red	Imp. over NOR (%)
s298	8	15.11	21.99	7.50	1.30	1.30	82.73
s344	11	10.63	14.43	4.75	0.00	0.00	100.00
s641	22	5.88	9.17	3.94	0.87	0.87	77.81
s838	20	4.62	5.86	1.74	0.40	0.40	77.15
s1196	16	7.60	11.96	3.34	0.45	0.45	86.49
s1423	46	2.90	4.70	1.61	0.45	0.45	72.20
s5378	13	8.66	11.44	3.54	0.00	0.00	100.00
s9234	16	4.95	9.05	2.51	0.00	0.00	100.00
s13207	21	5.12	8.13	3.31	0.00	0.00	100.00
s15850	28	4.04	4.90	1.28	0.00	0.00	100.00
s35932	14	15.85	24.03	8.91	1.31	1.31	85.28

TABLE IV
COMPARISON OF POWER OVERHEAD

Ckt.	% of power increase with: Latch gating	MUX gating	NOR gating	FLS un-shared	FLS shared	Imp. over NOR (%)
s298	92.23	68.00	34.48	3.40	1.14	96.68
s344	81.52	56.58	6.18	2.35	1.88	69.53
s641	136.36	100.83	20.81	3.58	2.50	87.96
s838	152.56	111.55	75.28	27.37	33.00	56.16
s1196	31.37	24.24	2.96	0.13	0.51	82.72
s1423	80.47	64.19	47.22	-7.87	0.37	99.22
s5378	91.60	65.43	12.05	-2.97	1.30	89.20
s9234	111.18	75.26	32.96	0.11	-7.79	123.63
s13207	120.72	86.75	22.88	-1.93	-13.79	160.26
s15850	110.44	81.41	27.36	1.55	-4.03	114.74
s35932	98.61	66.49	15.71	-7.21	-4.69	129.86

value, an extra inverter needs to be added to the inputs of combinational block to keep the logic value unchanged. This further adds to the delay overhead of the NOR-based gating technique. Moreover, as the logic depth decreases to meet higher performance in sequential circuit, the proposed FLS scheme shows much less delay overhead as compared to the NOR-based gating. For example, assuming a logic depth of six, composed of simple 2-input NAND and NOR gates, the delay overhead with the NOR-based technique is 19.6%, whereas the overhead in the FLS scheme is only 2.4%. Comparing the overhead in delay between NOR-based gating and FLS, FLS shows an average reduction of 94% in delay overhead compared to the NOR-based gating.

Table IV shows comparisons of power in normal mode of operation. Significant power savings are observed for all the benchmark circuits. In fact, the power dissipation of the FLS circuits are very close to the power dissipation of the original combinational circuit with no gating technique. This is because, in the proposed technique, the gating transistor and the pull-up PMOS do not switch in the active mode. The only source of power overhead is due to the diffusion capacitance added to the outputs of the first-level gates by the PMOS pull-up. However, this capacitance is negligible compared to the gate capacitance of the second level gates. It is interesting to notice that for large benchmark circuits such as s1423, s5378, and s35932,

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TABLE V
COMPARISON OF POWER CONSUMPTION DURING TEST MODE

Ckt.	# Flip-flops	Power in scan chain				% of comb. leakage power in total test power (NOR-gating)	% Improvement in total test power over NOR gating
		Latch/MUX based method	NOR-based method	FLS method	% increase over NOR		
S298	14	17.44	17.95	19.21	7.03	20.50	4.83
S344	15	18.69	19.23	19.76	2.72	19.54	3.22
S641	19	23.67	24.36	24.07	-1.20	18.53	7.63
S838	32	39.87	41.03	43.22	5.33	24.10	9.43
S1196	18	22.43	23.08	23.15	0.29	44.28	4.66
S1423	74	92.20	94.88	96.47	1.67	18.40	5.91
S5378	179	223.02	229.52	233.21	1.61	13.49	6.01
S9234	211	262.89	270.55	280.29	3.60	19.59	3.79
s13207	638	794.89	818.05	825.25	0.88	11.62	0.64
s15850	534	665.31	684.70	694.65	1.45	15.87	4.24
S35932	1728	2152.92	2215.66	2212.62	-0.14	15.11	8.25

the power of the FLS circuit is even less than the power of the original circuit. This is due to the fact that the gating transistor results in leakage reduction (due to the stacking effect [2], [3]) for the idle gates. For the large circuits, there are many idle first-level gates for any random pattern. The gating transistors reduce the leakage on the idle gates. This leakage is called active leakage because it occurs in the active mode on the idle gates. In the 70-nm technology node, the active leakage is a significant part of the overall active power. Reducing the active leakage on the first-level gates can result in overall power reduction for large circuits. Results for all the circuits show that the latch-based gating imposes the largest power overhead. The MUX-based gating has the second largest power overhead for all the circuits, whereas NOR-based gating shows the least overhead among the existing techniques. FLS shows overall power reduction of up to 33% compared to the NOR-based technique. However, the improvement in power overhead compared to the NOR-based method is as high as 160% and is 101% on an average for the circuits under consideration.

Larger sized gating transistors for gates in the critical path can be used to further reduce the delay penalty. It increases the area overhead but does not affect the switching power of the gates. However, upsizing the NOR, MUX, or latch does not help much to improve delay since it increases load on the scan flip-flop. Moreover, it comes at the cost of an increase in both area and power overhead. As in NOR-based gating [10], FLS allows at most two signal changes at a gated input for application of one test vector. Hence, we virtually eliminate switching power in the combinational logic during scan-shift operation. Area and power overhead can be further reduced by local fanout optimization under delay constraint, as discussed in Section V. The routing overhead associated with the proposed FLS technique should not be very high. This is because FLS requires no additional control signal. The TC signal needs to be routed to the scan flip-flops in a standard scan-based design, while in the proposed technique, the gating control signal needs to be routed only to the first level of logic.

IV. POWER IN TEST MODE

As we have seen in Section III, FLS induces some penalty in terms of power dissipation in normal mode of circuit operation due to the extra DFT logic, although it is significantly less compared to other methods. Although FLS saves most part of the energy spent during test application by eliminating switching activity in combinational block, it is not effective in saving power dissipated in scan chain due to rippling of scan values similar to the other gating methods. The scan partitioning technique presented in [7] is an effective solution for significantly reducing power in the scan chain during testing. There are two components of power dissipated in scan chain: switching power in the scan element and power in the clock line due to transition of clock. While clock power is independent of the load capacitance at the output of the scan element, the switching power of the scan element is almost linearly dependent on the output load. In the case of NOR-based gating, the output load of the scan flip-flop is a NOR gate, but, for FLS, the load varies, depending on fanout of a scan flip-flop. Hence, FLS can consume more power in the scan chain during test mode, depending on the average load on the outputs of the scan flip-flops. As described in Table V, FLS suffers an average increase of about 2% in scan power during scan in/out operation. However, the energy savings in the combinational part far outweighs the small energy overhead in the scan chain. It can be noted that both the latch-based and MUX-based methods have about the same power (Table V) in the scan chain since the multiplexer and latch circuit imposes almost the same load on their driver. We will present a fanout reduction algorithm for the FLS technique in Section V that can reduce the power overhead in the scan chain in test mode.

Another component of test power is the leakage power in the combinational block. Since the whole combinational block remains idle during scan shifting, it dissipates a considerable amount of power due to leakage current. In our experiment, average power dissipation due to leakage was 20% and 17% of the total test power in the case of the NOR-based gating and FLS, respectively (higher for MUX and latch gating) at a 100-MHz test clock. Column 7 in Table V lists the percentage of leakage power in the total test power for the NOR-based gating. The leakage power is expected to rise significantly with technology scaling and temperature, as explained in [2] and [3]. For a given scan chain and combinational block, the switching power in the scan chain reduces by technology scaling due to reduced capacitances and supply voltage. However, the leakage power in the combinational block increases due to an exponential increase in

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the subthreshold leakage and new mechanisms of leakage such as gate leakage and band-to-band-tunneling junction leakage [2]. Therefore, the leakage power becomes a larger fraction of the total test power during scan shifting. In terms of supply noise, leakage power on the combinational block adds as a constant dc component to the supply current during scan shifting. Such a dc component in the supply current results in IR-drop noise. This noise added to the switching noise due to switching of flip-flops can affect the reliability of the scan test. The FLS technique holds an important advantage over the alternative implementations in terms of reduction in leakage power, as described in Section IV-A. We will describe how the FLS scheme can be easily adapted to save leakage during scan shifting. It is interesting to observe that although the power in the scan chain is about 2% higher in FLS compared to the NOR-based method, significant reduction in leakage results in about a 5.3% average improvement in overall test power (see column 8 of Table V).

A. Leakage Reduction in Test Mode by Input Vector Control

Test vector bits are often scanned in using a slow clock to reduce switching power consumption and the chance of errors occurring due to scan chain delays. This increases the scan shifting time and, therefore, the leakage component of energy dissipation during testing. Therefore, it is important to address the leakage power issue even in the test mode.

Leakage of a combinational circuit is a strong function of the state of its inputs [16], [17]. Therefore, by selecting the best input vector for a combinational circuit during the standby mode, its leakage power dissipation can be minimized. There are algorithms proposed in the literature for finding the best input vector [16], [17]. The existing gating techniques fix the state of the inputs during shift operation. However, this input state may not correspond to the best input vector that minimizes overall leakage power on the combinational block. In the latch and MUX-based gating techniques, the states of inputs are fixed at the state of scan flip-flops before scan shifting starts. Therefore, the state of the inputs cannot be set to the best vector in the MUX and latch-based gating techniques. In the NOR and NAND-based gating techniques, the state of all inputs are forced to logical "0" and "1," respectively. However, state of all "0" or all "1" may not correspond to the best input vector. Interestingly, we have observed that the NAND and NOR gating can be used together to provide best input vector for the combinational block during scan shifting. In this case, the NOR masking is used at the inputs that are to be at the logic state of "0," and NAND masking is used at the inputs that are to be at the logic state of "1" to generate the best input vector. It can be noted that inverted masking signals are required to gate the NOR and NAND gates. Although this mixed use of NOR and NAND gating can induce the minimum leakage state in the combinational block, the blocking gates (NAND and NOR) themselves consume leakage power. The application of the best vector by the FLS can result in more leakage savings, because FLS does not introduce extra gates to mask the input switching.

In the proposed FLS scheme of Fig. 3(a) or (b), the outputs of the all first-level gates are forced to logic level "1" or "0," respectively. However, this state of inputs may not correspond to the best input vector for minimum leakage. By selective use of gated-GND [Fig. 3(a)] or gated-VDD [Fig. 3(b)]

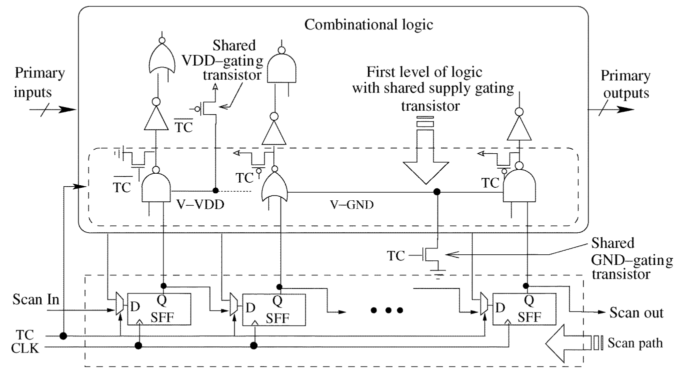

Fig. 7. Leakage reduction with supply gating and input vector control. Gating transistors are shared among gating of the same type (i.e., with gated-VDD or gated-GND).

for individual inputs, the state of the circuit can be assigned to the best input vector during the scan test in order to minimize leakage power dissipation on the combinational circuit. Fig. 7 shows the scan architecture with input vector control using FLS. It is worth noting that sharing of the gating transistors is still possible. However, to avoid a possible short-circuit condition, sharing has to be limited between logic gates with similar gating, i.e., all the NMOS GND-gating transistors can be shared among the GND-gated first-level gates, and all the PMOS VDD-gating transistors can be shared among the VDD-gated first-level gates (see Fig. 7). In this case, an inverted gating control signal is required to control the PMOS VDD-gating transistors.

The results of leakage savings by input vector control using mixed NOR/NAND and mixed gated GND/VDD FLS for different benchmark circuits are shown in Table VI. The best input vectors are found using the algorithms described in [16]. As observed, depending on the benchmark, significant savings can be achieved by applying the best input vector using selective use of gated-GND or gated-VDD FLS schemes for individual inputs. The mixed FLS gating techniques show improvements of 37%, 36%, and 29% in leakage power on an average compared to the NOR, NAND, and mixed NOR/NAND masking techniques. These improvements are attributed to two facts: a) FLS eliminates the extra gating logic circuits (NOR/NAND), which are also leaking, and b) FLS reduces the leakage of first-level gates due to the stacking effect. Since the leakage for a multiplexer and latch are more than $10\times$ higher than the NOR gate, we get more improvement in leakage with FLS compared to the MUX or latch-based methods. The leakage reduction is an additional advantage of the mixed FLS techniques on top of the benefits in terms of area, delay, and power in the normal mode.

Due to the exponential increase of leakage with technology scaling and temperature increase, the leakage reduction of the mixed FLS becomes more effective as the technology scales or the temperature increases. Table VII shows the improvement in the effectiveness of this technique in the reduction of the overall test power with technology scaling. As the technology scales to smaller feature sizes, the leakage power on the combination block becomes a larger fraction of the total test power. Therefore, leakage reduction by mixed FLS gating can result in a more dramatic saving in the total test power. As observed from Table VII, compared to the NOR-based gating, the mixed FLS gating results in an average reduction of 5.3% in the overall

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TABLE VI
LEAKAGE POWER (μW) OF COMBINATIONAL BLOCK IN THE TEST MODE FOR DIFFERENT GATING TECHNIQUES (70-nm CMOS, Supply = 1 V, T = 25°C)

Ckt.	Leakage in combinational circuit with					% improvement with mixed FLS		
	NOR gating	NAND gating	Gated-GND FLS	IVC by mixed NAND/NOR	IVC by mixed FLS	over NOR gating	over NAND gating	over mixed NAND/NOR
s298	4.63	3.70	3.36	3.54	2.28	50.75	38.37	35.65
s344	4.67	5.03	3.66	4.49	3.37	27.97	33.06	24.97
s641	5.54	5.50	4.90	4.77	3.55	35.90	35.37	25.56
s838	13.03	12.83	9.15	9.98	5.74	55.96	55.26	42.52
s1196	18.34	19.29	17.45	17.39	16.34	10.89	15.29	6.06
s1423	21.40	20.93	16.09	18.34	12.94	39.54	38.18	29.44
s5378	35.80	30.82	21.29	30.55	16.17	54.83	47.53	47.07
s9234	65.92	66.02	48.35	61.05	43.43	34.12	34.21	28.86
s13207	107.53	103.33	95.38	105.53	94.39	12.23	8.66	10.56
s15850	129.17	131.52	96.50	117.54	84.71	34.42	35.59	27.93
s35932	394.33	383.52	258.04	316.58	182.14	53.81	52.51	42.47

TABLE VII
LEAKAGE REDUCTION BY MIXED FLS GATING IN SCALED TECHNOLOGIES

Ckt.	% reduction in total test power compared to NOR-based gating	
	70nm tech.	45nm tech.
s298	4.81	37.02
s344	3.28	11.68
s641	7.63	27.11
s838	9.44	40.72
s1196	4.66	10.31
s1423	5.92	26.29
s5378	6.01	36.06
s9234	3.79	22.82
s13207	0.64	7.48
s15850	4.24	22.20
s35932	8.25	33.26

test power in the 70-nm technology. This reduction, however, improves to 25% in a more scaled technology of 45 nm. Hence, FLS outperforms alternative gating techniques in terms of total test power as well. Moreover, these results manifest the scalability of the proposed gating techniques across technology generations.

The input vector control using the FLS scheme can also be dynamically employed during the normal mode of operations when the combinational block is idle. In this way, the active leakage component of power dissipation can be reduced. In this case, an extra control signal needs to be generated to dynamically gate the first-level gates during normal mode of operation.

V. FURTHER REDUCTION OF AREA/POWER OVERHEAD

In FLS, the overhead in terms of die-area and power during normal operation is less than in earlier methods. Transistor downsizing can be applied in all the methods, including FLS, to reduce the area and power overhead, but narrowing transistor width usually trades off circuit performance by affecting critical path delay. FLS, however, has the potential to reduce the area penalty further without compromising delay.

Since the overhead in area and power in FLS is proportional to the number of unique fanout cells, we can reduce the overhead by optimizing the number of direct fanouts of the scan flip-flops. The number of fanout cells in a circuit is not generally allowed to be large, since it affects capacitive load at the output of a cell and, hence, increases propagation delay. It can be noted that when a netlist is mapped to a standard cell library, fanouts of the cells may change, depending on the gate types available in the library. Existence of complex gate types like "aoi" or "mux" tends to reduce number of fanouts. As an example, for the benchmark s838, the number of unique fanouts is 118 for a cell library containing only inverter and 2-input NOR/NANDs, whereas this number reduces to 96 (19% improvement) when the netlist is technology-mapped to the complete the *LEDA* library consisting of multi-input complex gates.

We designed a low-complexity local fanout reduction algorithm which targets minimization of first-level gates under constraint on critical path delay. The algorithm is based on finding a minimal vertex cover [18] of a bi-partitite graph and then adding two inverters in series at the output of selected scan flip-flops. First, we create a undirected bi-partite graph $G = \{SO, FL\}$ with the scan flip-flop outputs (*SO*) and the first-level gates (*FL*) as vertices. Edges in G correspond to logic path from scan flip-flops to first-level gates in the netlist. Critical path edges are marked G. Then, we determine an approximate solution of the vertex cover problem ($VC = \{\{SO_i\}, \{FL_j\}\}$) for the graph G using a greedy heuristic-based solution of linear complexity. Note that the vertex cover problem, i.e., finding an optimal vertex set that covers all the edges in a graph is NP-Hard [18]. We, however, use an approximate solution for the vertex cover problem using heuristics. First, we identify the *SO* vertices that have a single fanout and select the incident *FL* vertex for them. We choose these *FL* vertices into *VC* one at a time in decreasing order of degree of the vertices and remove all their incident edges from G. Next, we choose those *FL* nodes with high degree (i.e., large number of incident edges, say three or more) and the ones corresponding to critical path edges. As before, the incident edges of all *FL* nodes selected in *VC* are removed from G. Finally, the *SO* vertices with remaining degree greater than 0 are selected into *VC*.

Two inverters (*INV*1, *INV*2) of appropriate sizes are added to all the SO_is in *VC*, and the output of INV2 is connected to all *FL*s adjacent to SO_i and not in *VC*. We then try to resynthesize the second inverter and the following first-level gates to reduce the area/delay penalty. For example, if SO_1 and SO_2 are connected to an OR gate, and both are in *VC*, then the second inverters can be resynthesized with the OR gate to generate a NAND gate with about one third the delay/area of *INV*2 and the OR gate.

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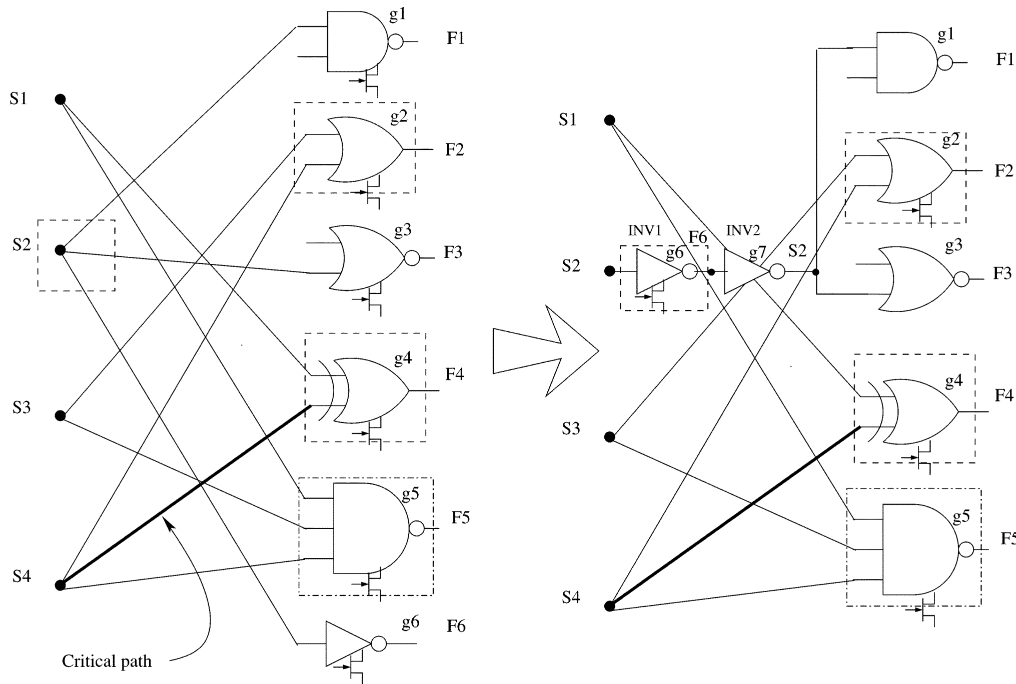

Fig. 8. Example of fanout reduction with the proposed algorithm.

TABLE VIII
COMPARISON OF AREA AND POWER IN NORMAL MODE AND POWER IN TEST MODE BEFORE AND AFTER FANOUT OPTIMIZATION

Ckt.	# FFs	Fanout (before)	Fanout (after)	% improvement in area	% Comb. power increase	% Seq. power increase (before)	% Seq. power increase (after)	% improvement in total power
s298	14	35	18	89.75	-2.21	7.03	0.64	9.90
s344	15	32	15	6.19	3.69	2.72	-1.75	6.83
s641	19	19	19	0.00	0.00	-1.20	-1.20	7.62
s838	32	96	36	22.07	2.45	5.33	-1.37	14.52
s1196	18	23	18	9.34	0.60	0.29	-1.19	5.49
s1423	74	160	86	-13.58	1.98	1.67	-1.31	8.34
s5378	179	280	163	-5.78	-7.64	1.61	-1.43	8.64
s9234	211	445	199	22.18	-6.51	3.60	-1.92	8.23
s13207	638	729	589	17.49	4.19	0.88	-1.14	2.43
s15850	534	837	519	25.07	-3.11	1.45	-1.77	6.95
s35932	1728	2692	1728	36.20	-2.26	-0.14	-1.90	9.74

However, delay or area improvement with resynthesis largely depend on the circuit topology. We have used a Synopsys-design compiler to locally synthesize the first level of the gate with *INV*2 to improve area overhead with a time constraint. We keep *INV*1 unaffected. If a scan flip-flop is already connected to an inverter, we can use it as *INV*1. It can be noted that although additional inverters may introduce extra delay, reduction of the output load of the scan flip-flop due to lesser fanouts induces a positive impact on the delay. To ensure that the delay constraint is met, we remove inverters from those paths that violate the delay constraint and add their incident *FL* nodes directly to *VC*. Finally, gating logic is added to all FL_j in *VC* and to all *INV*1, which become the new first-level gates.

The flow of the algorithm is explained in Fig. 8 with an example. We start with four scan flip-flop outputs ($s1$, $s2$, $s3$, and $s4$) and six first-level gates ($g1, \ldots, g6$). The critical path edge is marked in bold. Before fanout reduction, gating logic needs to be applied to all six fanout gates. First, we create a bi-partite graph and determine the vertex cover as marked by dashed boxes (the left side of the schematic in Fig. 8). We add two inverters in series to scan the flip-flop outputs in *VC* in such a way that the timing constraint is not violated. Gating logic is added to the new first-level gates (the right side of the schematic in Fig. 8), the number of which is reduced to four.

We implemented the algorithm in C programming language and observed its impact on some benchmark circuits for the case of Shared FLS. The result is shown in Table VIII. It can be noted that we get significant improvement in fanouts (with an average reduction of 38%) for the set of ISCAS circuits under consideration. Although the power in combinational logic remains comparable, area overhead improves significantly (by 19% on an average). Since the area overhead in Unshared FLS is higher than Shared FLS, we get higher improvement (of 23.5% on an average) when the gating transistor is not shared. Power reduction due to a reduction in gating logic is balanced out by a possible increase in the amount of switching at the outputs of the extra inverters. Power during test application in the scan chain improves consistently, as shown in the last two columns,

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since the load at the outputs of the scan flip-flops reduces with fanout reduction. The test-mode power in the scan chain becomes better than NOR-based gating for all test circuits except s298. The complexity of the algorithm is determined by the sorting algorithm required to find the vertex cover and, hence, is $O(n \log n)$, where n is the number of vertices in graph G. The algorithm took only 59.27 s to run in a GNU/LINUX machine with an i686 processor for the benchmark s35932.

VI. Test Considerations

Fault coverage and fault models remain unaffected with the insertion of FLS. During normal mode of operation, the gating transistors are turned ON; hence, the conventional stuck-at fault models (the transition and path delay fault models) still remain valid. We can directly apply the stimulus and response patterns (for a particular fault model) generated by conventional ATPG tools for standard scan-based testing to a scan architecture using FLS. Besides, FLS maintains the fault coverage. However, the insertion of extra transistors brings in the possibility of extra faults. Any additional DFT logic is likely to increase the fault set. Since the DFT overhead in FLS is significantly lower than the MUX-based, NOR-based, or enhanced scan-based methods, gating logic in FLS causes much lower impact on the total fault set. Since the proposed method can save a large part of the test power, irrespective of test patterns, low-power ATPG tools [4], [13] need to address power dissipation in the scan chain only and can, thus, generate a more efficient test set in terms of test application time and/or coverage.

The proposed FLS technique can be easily integrated into the automatic scan synthesis tools. For automated scan design flow, the scan synthesis tool first identifies the flip-flops that need to be placed in the scan chain. The synthesis tool then identifies all the first-level logic gates in the fan-out cones of the scan flip-flops. Next, it adds PMOS pull-up transistors to the outputs of the identified first-level logic gates. In the placement and routing (PR) phase, the PR tool connects virtual ground ports of the first-level logic gates together and inserts an NMOS ground gating transistor between the virtual ground line and the real ground. Logic cells with virtual ground ports, the PMOS pull-up, and the NMOS GND-gating transistors can be added to the standard cell library. There is no special routing constraint on the GC (TC) signal because it is a low-frequency control signal. Since the gating control signal is not time-critical, unlike clock, FLS does not require special considerations (e.g., skew, jitter etc.) in distributing it.

The proposed technique can be easily applied to scan-based test-per-scan BIST [9], [13] circuits. A circuit designed with BIST has a weighted random pattern generator and an output response analyzer built into the circuit. Random test patterns are generated by a Linear Feedback Shift Register (LFSR). The patterns are applied to both primary inputs and scan cells. Depending on how the test patterns are applied to the primary inputs (sequential as in the scan chain or parallel), the combinational logic may suffer from redundant switching when the patterns are applied to primary inputs. If patterns are applied sequentially, we need to incorporate gating logic for the primary inputs as well. The FLS technique proposed for the scan path can be equally used on the fanout logic gates for the primary inputs. It may help to further amortize the overhead of the FLS, since the first-level fanout cells for the primary input and scan outputs can overlap significantly. For example, in the case of benchmark s838, the average number of unique fanouts reduces from 3 to 2.8 after primary inputs are considered for gating.

FLS does not affect scan-based structural delay fault testing. A test circuit with regular scan cells (not enhanced scan) is capable of performing delay tests where the second pattern is applied by switching only the primary inputs (broadside delay testing) or by shifting the scan cells by one bit (skewed-load delay testing) [9]. In both cases, once the scan chain is loaded, we need to make the gating control signal *high* to enable signal propagation and keep it at that level throughout the capture cycle. In this case, the TC signal can be applied well ahead of time (at least one cycle ahead) to let the state of the combinational block become stable to the first test pattern before shift/launch of the second test pattern. For enhanced scan-based delay testing, selected scan elements are morphed to enhanced scan cells by adding a hold latch [9], which automatically blocks switching in scan cells to propagate into combinational logic. In that case, the proposed first-level gating can be used in those scan cells, which are not modified with a hold latch to completely eliminate switching in the combinational block during scan shifting.

VII. Conclusions

We proposed a novel low-cost solution (FLS) for preventing redundant switching in combinational logic during scan testing. Compared to existing methods using NOR or MUX-based output gating, the proposed technique can achieve similar savings in average and peak power during test with significantly lower DFT overhead with respect to die-area, circuit performance, and power. FLS gating can also help to reduce leakage power considerably during scan-in/out operation by setting the best vector at the input of combinational logic. The technique maintains fault coverage and does not impact the test generation or test application process. It can be easily extended to test-per-scan BIST and can be coupled with other scan-power reduction techniques like scan reordering or scan partitioning to produce additional savings in test power.

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