

An analytical model for read static noise margin including soft oxide breakdown, negative and positive bias temperature instabilities

Behrouz Afzal^a, Behzad Ebrahimi^a, Ali Afzali-Kusha^{a,*}, Hamid Mahmoodi^b

^a Nanoelectronics Center of Excellence, School of Electrical and Computer Engineering, University of Tehran, College of Engineering, Tehran, Iran

^b Department of Electrical and Computer Engineering, San Francisco State University, CA, USA

ARTICLE INFO

Article history:

Received 29 November 2012

Accepted 25 January 2013

Available online 7 March 2013

ABSTRACT

In this paper, we propose an accurate model for the read static noise margin (SNM). The model includes the effects of soft oxide breakdown (SBD), negative and positive bias temperature instabilities (NBTI and PBTI, respectively). To assess the accuracy of the proposed model, its predictions are compared with those of HSPICE simulations for 32, and 22 nm technologies. The comparison verifies the high accuracy of the model. The results show a maximum error of 4.5% for a wide range of supply voltages. Using this model, the effect of bias temperature instabilities on the aggravation of the read SNM by SBD is also studied. The study shows that both NBTI and PBTI phenomena worsen the effect of SBD on the read SNM by 34%.

© 2013 Elsevier Ltd. All rights reserved.

1. Introduction

Reliability concerns have slowed down the operating voltage reduction with each new technology node while the gate oxide has become thinner for a given dielectric material [1]. This results in larger electric fields in the gate oxide which could form traps in the oxide. As the number of traps increases, they start to overlap forming a conduction path between the gate and channel which may create a gate tunneling current. This type of breakdown which is known as soft oxide breakdown (SBD) may occur in both SiO₂ and high-*k* gate dielectrics [2,3]. The SBD phenomenon can deteriorate the functionality of SRAM cells [4–6].

Larger vertical electric fields can cause another reliability problem for transistors which is called bias temperature instability (BTI) [7]. For PMOS transistors, when negative gate biases are applied, high energy holes break Si–H bonds at the Si–SiO₂ interface forming interfacial traps. These traps increase the threshold voltage of the device, and hence, affecting the performance of the transistor (NBTI effect) [7]. Similarly, in the case of NMOS transistors with high-*k*, under positive gate biases, a significant charge trapping may occur increasing the threshold voltage with time (PBTI effect) [8].

The effect of NBTI and PBTI on the stability and performance of SRAM cells have been investigated in the literature (e.g. [9–11]). The studies reveal that the most important parameter of SRAM cells which degrades with these bias temperature instabilities is the read stability (read SNM) [9–11]. In addition, the effects of SBD on different performance and functionality parameters of

SRAM cells have been investigated in [4–5,10–16]. In particular, the work presented in [12] studies the effect on the read stability for a 90 nm technology. The study shows that SBD is a dominant factor in the read stability degradation. In [13], a read SNM model which considers SBD along with NBTI was proposed. The model was based on the simple square law model for the *I*–*V* characteristic and did not consider the PBTI effect.

The contributions of this paper are as follows:

- We use a more accurate expression for the *I*–*V* characteristic to present a more tangible read SNM model for smaller technologies.
- The proposed model considers the SBD effect as well as both PBTI (important for transistors with high-*k* gate dielectrics) and NBTI effects.

The remainder of the paper is organized as follows. In Section 2, the models used for the SBD, NBTI, and PBTI effects are described while, in Section 3, a read SNM model considering the SBD effect with short channel *I*–*V* models is derived. In Section 4, the accuracy of the model is investigated by comparing its results to those of HSPICE. In addition, using this model, the read SNM degradation in the simultaneous presence of NBTI, PBTI, and SBD effects is studied. Finally, Section 5 concludes the paper.

2. SBD and BTI modeling

After the occurrence of the soft breakdown phenomenon, the gate current, *I_g*, may be modeled as [12]

$$I_g = I_0 \exp(tGR) \quad (1)$$

* Corresponding author. Tel.: +98 21 8208 4920; fax: +98 21 8877 8690.

E-mail address: afzali@ut.ac.ir (A. Afzali-Kusha).

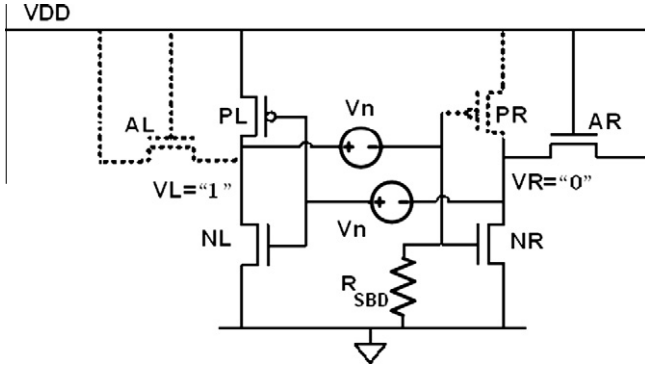


Fig. 1. Schematic of a 6T SRAM cell when is accessed with static noise sources V_n and SBD resistor inserted [13].

Here, I_0 is the initial oxide tunnel current, t is the elapsed time, and GR is the defect current growth rate which has an exponential relation with the stress voltage and oxide thickness as

$$GR = K_1 \exp(\theta_1 V_g - \theta_2 T_{ox}) \quad (2)$$

where V_g is the gate stress voltage, T_{ox} is the gate oxide thickness, and θ_1 , θ_2 , and K_1 are constants which may be found from experimental data [12].

The breakdown may occur between the gate and diffusion region (source or drain) or between the gate and the channel of the transistors. Experimental data shows that the pull down source breakdown causes more severe stability degradation in a conventional 6T SRAM cell which is shown in Fig. 1 [17], and hence, similar to [13], only the gate-source breakdown of the pull down transistor under stress (NR in Fig. 1) is considered in this work. Using Eq. (1), the SBD is modeled as a resistor (R_{SBD}) given by [12]:

$$R_{SBD} = \frac{V_{dd}}{I_0} \exp(-tGR) \quad (3)$$

where V_{dd} is the supply voltage.

Next, we should model the NBTI and PBTI effects which increase the magnitudes of the threshold voltages of PMOS and NMOS transistors, respectively, as a function of time (t). The increase, which is denoted by ΔV_{th} , may be modeled by the DC reaction–diffusion (RD) framework as [7]

$$|\Delta V_{th}| = K_{DC} t^n \quad (4)$$

Here, K_{DC} is a constant which depends on the gate–source bias (V_{gs}), temperature, and other technology parameters. Fig. 2 shows the

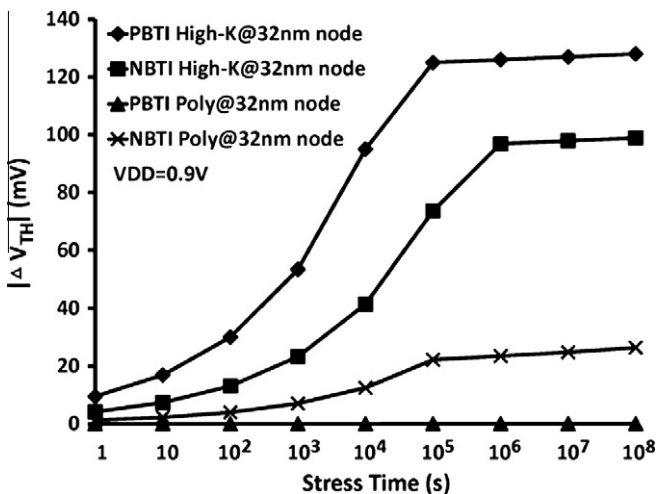


Fig. 2. V_{th} change due to the NBTI and PBTI using reaction–diffusion framework calibrated with published data [18].

change in V_{th} due to NBTI and PBTI using the reaction diffusion framework which has been calibrated with published data for a 32 nm technology node [18]. The results are for poly (oxide/polysilicon) and high- k (high- k /metal gate) cases. While the PBTI effect on the threshold voltage is dependent on both dielectric and gate materials, the threshold voltage change due to the NBTI effect is only dependent on the dielectric material [18]. The results reveal that the PBTI can be ignored for the case of poly gate while it should be considered for the case of high- k .

3. Read SNM modeling considering SBD

Next, we should model the read SNM of the 6T SRAM cell during the read operation. For this purpose, we use the circuit which is shown in Fig. 1 where static noise sources (V_n) and soft oxide breakdown resistance (R_{SBD}) have been added. The resistance R_{SBD} which models the gate-to-source soft breakdown of NR is modeled as a linear resistor between the gate and the source. The resistance could degrade the read SNM considerably, and hence, we have considered only this scenario of breakdown in the analysis. The same approach has been taken in [13]. In addition, since the chance of multiple breakdown events is quite low, we ignore them in this work.

To improve the read SNM modeling approach presented in [13], we employ a more accurate expression for the I – V characteristics. Instead of the square law model, in this work, we use the BSIM3v3 short channel model equations for hand calculations [19]. In the linear region ($V_{ds} < V_{dsat}$), the drain current (I_{ds}) is given by [19]:

$$I_{ds} = \beta \frac{1}{1 + V_{ds}/(E_{sat}L)} \left(V_{gs} - V_{th} - \frac{A_{bulk}V_{ds}}{2} \right) V_{ds} \quad (5)$$

where A_{bulk} is the bulk charge coefficient, L is the channel length, E_{sat} is the minimum electric field for the onset of velocity saturation, V_{gs} , V_{ds} , and V_{th} are the gate–source, drain–source, and threshold voltages, respectively, and

$$\beta = \mu_{eff} C_{ox} \frac{W}{L} \quad (6)$$

where μ_{eff} is the effective mobility, C_{ox} is the gate capacitance per unit area, and W is the channel width. In the saturation region ($V_{ds} > V_{dsat}$), the current–voltage characteristics is expressed as [19]

$$I_{ds} = \frac{\beta}{2A_{bulk}} \frac{1}{1 + (V_{gs} - V_{th})/(A_{bulk}E_{sat}L)} (V_{gs} - V_{th})^2 \left(1 + \frac{V_{ds} - V_{dsat}}{V_A} \right), \quad (7)$$

where

$$V_{dsat} = \frac{E_{sat}L(V_{gs} - V_{th})}{A_{bulk}E_{sat}L + V_{gs} - V_{th}} \quad (8)$$

Assuming PR is off, one may write the KCL equation at the node R as

$$I_{NR} = I_{AR} \quad (9)$$

Also, we suppose that NR and AR operate in the linear and saturation regions, respectively, and hence, we can write

$$I_{NR} = \beta_{NR} \frac{1}{1 + V_{ds-NR}/(E_{sat-NR}L_{NR})} \left(V_{gs-NR} - V_{th-NR} - \frac{A_{bulk-n}V_{ds-NR}}{2} \right) V_{ds-NR} \quad (10)$$

$$I_{AR} = \frac{\beta_{AR}}{2A_{bulk-n}} \frac{1}{1 + (V_{dd} - V_{ds-NR} - V_{th-AR})/(A_{bulk-n}E_{sat-AR}L)} \times (V_{dd} - V_{ds-NR} - V_{th-AR})^2 \times \left(1 + \frac{V_{dd} - V_{ds-NR} - \frac{E_{sat}L_{AR}(V_{dd} - V_{ds-NR} - V_{th-AR})}{A_{bulk-n}E_{sat}L_{AR} + V_{ds-NR} - V_{th-AR}}}{V_A} \right) \quad (11)$$

It has been shown that the transfer characteristics of $V_{gs-NR} - V_{ds-NR}$ have a fairly constant slope around its operating point where NR is in the linear region [20]. The linear approximation of this characteristic may be expressed as [20]

$$V_{ds-NR} = V_0 - kV_{gs-NR} \quad (12)$$

The parameters in Eq. (12) may be found by fitting the model predictions to the simulation results [13]. However, these parameters are sensitive to the threshold voltage of NR which is increased by PBTI. For the study of the PBTI effect, we need to find analytical models for these parameters as a function of the threshold voltage. As the first step in finding the parameters k and V_0 , let us take partial derivatives of both sides of Eq. (9) with respect to V_{gs-NR} and V_{ds-NR} .

$$\begin{aligned} \frac{\partial I_{NR}}{\partial V_{gs-NR}} dV_{gs-NR} + \frac{\partial I_{NR}}{\partial V_{ds-NR}} dV_{ds-NR} \\ = \frac{\partial I_{AR}}{\partial V_{gs-NR}} dV_{gs-NR} + \frac{\partial I_{AR}}{\partial V_{ds-NR}} dV_{ds-NR} \end{aligned} \quad (13)$$

By dividing both sides by dV_{gs-NR} , we obtain

$$\frac{\partial I_{NR}}{\partial V_{gs-NR}} + \frac{\partial I_{NR}}{\partial V_{ds-NR}} \frac{dV_{ds-NR}}{dV_{gs-NR}} = \frac{\partial I_{AR}}{\partial V_{gs-NR}} + \frac{\partial I_{AR}}{\partial V_{ds-NR}} \frac{dV_{ds-NR}}{dV_{gs-NR}} \quad (14)$$

Using Eq. (12), one may write

$$\frac{dV_{ds-NR}}{dV_{gs-NR}} = -k \quad (15)$$

Also, from Eq. (14), one may write

$$k = \frac{\frac{\partial I_{NR}}{\partial V_{gs-NR}} - \frac{\partial I_{AR}}{\partial V_{gs-NR}}}{\frac{\partial I_{NR}}{\partial V_{ds-NR}} - \frac{\partial I_{AR}}{\partial V_{ds-NR}}} \quad (16)$$

The above equation (Eq. (16)) is valid at all points in the operation region of our interest, and hence, may be solved at any arbitrary point in this region. Let us consider $V_{gs-NR} = V_{dd}$ where the corresponding V_{ds-NR} is denoted by V_{ds0} . The voltage V_{ds0} , which is small, can be found from Eq. (9) by equating V_{gs-NR} and V_{ds-NR} equal to V_{dd} and V_{ds0} , respectively. Using proper approximations, one may write

$$\begin{aligned} (V_{dd} - V_{th-NR} - \frac{1}{2} A_{bulk-n} V_{ds0}) V_{ds0} \\ = \frac{\beta_{AR}}{2A_{bulk-n}\beta_{NR}} \times \frac{(V_{dd} - V_{ds0} - V_{th-AR})^2}{1 + \frac{V_{dd} - V_{th-AR}}{A_{bulk-n} E_{sat} L_{AR}}} \\ \cdot \left(1 + \frac{V_{dd} - \frac{E_{sat-AR}(V_{dd} - V_{th-AR})}{E_{sat-AR} + V_{dd} - V_{th-AR}}}{V_A} \right) \end{aligned} \quad (17)$$

which is a second order equation with respect to V_{ds0} . Using V_{gs-NR} and V_{ds-NR} , one can use Eqs. (10), (11), and (16) to find k . Finally, V_0 is found from Eq. (12).

Similarly, assuming AL is off, one may write the KCL equation at the node L as

$$f = I_{NL} + V_{gs-NR}/R_{SBD} - I_{PL} = 0 \quad (18)$$

Considering the fact that NL and PL operate in the saturation and linear regions, respectively, we have

$$\begin{aligned} I_{NL} = \frac{\beta_{NL}}{2A_{bulk-n}} \frac{1}{1 + (V_n + V_{ds-NR} - V_{th-NL}) / (A_{bulk-n} E_{sat} L_{NL})} (V_n \\ + V_{ds-NR} - V_{th-NL})^2 \\ \times \left(1 + \frac{V_n + V_{gs-NR} - \frac{E_{sat-NL}(V_n + V_{ds-NR} - V_{th-NL})}{A_{bulk-n} E_{sat} L_{NL} + V_n + V_{ds-NR} - V_{th-NL}}}{V_A} \right), \end{aligned} \quad (19)$$

As $V_n + V_{ds-NR} - V_{th-NL}$ has a small value and $V_n + V_{gs-NR}$ is close to V_{dd} , I_{NL} may be approximated as

$$I_{NL} \approx \frac{\beta_{NL}}{2A_{bulk-n}} (V_n + V_{ds-NR} - V_{th-NL})^2 \times \left(1 + \frac{V_{dd}}{V_A} \right), \quad (20)$$

and

$$\begin{aligned} I_{PL} = \beta_{PL} \frac{1}{1 + \frac{V_{dd} - V_n - V_{gs-NR}}{E_{sat} L_{PL}}} \\ \times \left(V_{dd} - V_n - V_{ds-NR} - V_{th-PL} - \frac{A_{bulk-p}(V_{dd} - V_n - V_{gs-NR})}{2} \right) \\ \times (V_{dd} - V_n - V_{gs-NR}) \end{aligned} \quad (21)$$

Similarly, since V_{ds-PL} ($V_{dd} - V_n - V_{gs-NR}$) is a small voltage, I_{PL} may be approximated as

$$\begin{aligned} I_{PL} \approx \beta_{PL} \left(V_{dd} - V_n - V_{ds-NR} - V_{th-PL} - \frac{A_{bulk-p}(V_{dd} - V_n - V_{gs-NR})}{2} \right) \\ \times (V_{dd} - V_n - V_{gs-NR}) \end{aligned} \quad (22)$$

Substituting Eqs. (20) and (22) into Eq. (18) yields a quadratic equation with respect to V_n as

$$pV_n^2 + qV_n + z = 0 \quad (23)$$

where

$$p = \frac{\beta_{NL} \left(1 + \frac{V_{dd}}{V_A} \right)}{2A_{bulk-n}} + \beta_{PL} \left(-1 + \frac{A_{bulk-p}}{2} \right) \quad (24)$$

$$\begin{aligned} q = \frac{\beta_{NL}(V_0 - kV_{gs-NR} - V_{th-NL}) \left(1 + \frac{V_{dd}}{V_A} \right)}{A_{bulk-n}} + \beta_{PL}(V_{dd} + (1 \\ - A_{bulk-p})(V_{dd} - V_{gs-NR}) - V_0 + kV_{gs-NR} - V_{th-PL}) \end{aligned} \quad (25)$$

$$\begin{aligned} z = \frac{\beta_{NL}(V_0 - kV_{gs-NR} - V_{th-NL})^2 \left(1 + \frac{V_{dd}}{V_A} \right)}{2A_{bulk-n}} + \frac{V_{gs-NR}}{R_{SBD}} \\ - \beta_{PL} \left(V_{dd} - \frac{A_{bulk-p}}{2} (V_{dd} - V_{gs-NR}) - V_0 + kV_{gs-NR} - V_{th-PL} \right) (V_{dd} \\ - V_{gs-NR}) \end{aligned} \quad (26)$$

SNM is equal to V_n when the condition of coinciding roots for the quadratic equation is satisfied [20]. For this equation, there is some V_{gs-NR} which sets the delta of the quadratic equation (Eq. (23)) equal to zero.

It was shown in [13] that there was almost a linear relation between the read SNM multiplied by the SBD resistance squared and the resistance. The same characteristics have been plotted in Fig. 3 for 32 and 22 nm metal gate/high- k technologies [21] where the PBTI effect is also important. The linear relation which is observed for different threshold voltages of the PMOS transistor affected by NBTI (PL in Fig. 1) and NMOS transistor affected by PBTI (NR in Fig. 1) is valid for SNM values which are positive. For this plot, we have assumed the same amounts of threshold voltage shifts for both PL and NR . Therefore, similar to [13], we can use the following linear relationship for modeling this dependence.

$$(SNM(R_{SBD}) - SNM(\infty)) \cdot R_{SBD}^2 = \gamma + \lambda \cdot R_{SBD} \quad (27)$$

Rewriting Eq. (27) using the parameters a and b yields

$$SNM = SNM(R_{SBD} = \infty) - \frac{a}{R_{SBD}} - \frac{b}{2 \cdot R_{SBD}^2} \quad (28)$$

where

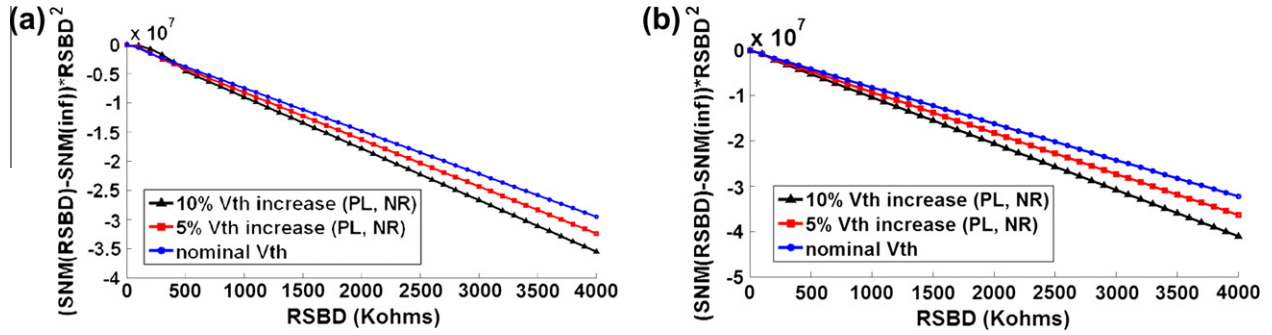


Fig. 3. SBD induced variations in read SNM multiplied by SBD resistance squared for different threshold voltages of PL and NR for (a) 22 nm, (b) 32 nm.

$$a = -\lambda = \lim_{R_{SBD} \rightarrow \infty} R_{SBD}^2 \frac{\partial SNM}{\partial R_{SBD}} \quad (29)$$

$$b = -2\gamma = \lim_{R_{SBD} \rightarrow \infty} \left(\frac{\partial \left(R_{SBD}^2 \frac{\partial SNM}{\partial R_{SBD}} \right)}{\partial \left(\frac{1}{R_{SBD}} \right)} \right) \quad (30)$$

Now, in order to obtain the derivative of SNM with respect to R_{SBD} , we take the partial derivative of f (defined in Eq. (18)) with respect to V_{gs-NR} , V_n , and R_{SBD} and obtain

$$\frac{\partial f}{\partial V_{gs-NR}} dV_{gs-NR} + \frac{\partial f}{\partial V_n} dV_n + \frac{\partial f}{\partial R_{SBD}} dR_{SBD} = 0 \quad (31)$$

Therefore, one can obtain the derivative of the noise margin with respect to the soft breakdown resistance as

$$\frac{dV_n}{dR_{SBD}} = - \frac{\frac{\partial f}{\partial V_{gs-NR}} \frac{dV_{gs-NR}}{dR_{SBD}} + \frac{\partial f}{\partial R_{SBD}}}{\frac{\partial f}{\partial V_n}} \quad (32)$$

Thus, the derivative of SNM with respect to R_{SBD} may be easily found from Eq. (32). Note that in using Eq. (32), V_n is equal to SNM, V_{gs-NR} is obtained from setting the delta of the quadratic equation (Eq. (23)) equal to zero, and V_{ds-NR} is obtained from Eq. (12). Then, coefficients a and b also can be found from this and Eqs. (29) and (30), respectively. The first term in Eq. (28), which represents the SNM without considering the SBD effect, may be obtained using existing accurate models for the SNM which are functions of the threshold voltages of the transistors (see, e.g., [22–24]). For these models, to include the BTI effects, we only need to add ΔV_{th} due to NBTI and PBTI using the models reported in the literature (e.g. [18]). The other terms in Eq. (28), which are attributed to SBD, can be found from our expressions for a , b , and R_{SBD} . There are other models for R_{SBD} which also may be used in our model (see, e.g. [12]).

4. Results and discussion

The accuracy of the proposed model is assessed by comparing the model predictions with those of HSPICE simulations for 22 and 32 nm metal gate/high- k technologies [21]. First, we present the results for the read SNM versus R_{SBD} for the nominal threshold voltage as well as 5% and 10% threshold voltage shifts of both the transistors PL and NR. The results which are shown in Fig. 4 reveal a very good accuracy for the model. Therefore, this hints that the model may provide a fast yet accurate estimation of the SNM compared to the simulation method.

In [13], it was shown that both the SBD and NBTI effect should be considered together to obtain the correct model for predicting the variation of the read SNM over the time. In Fig. 5, we have presented similar results with the difference of including PBTI too. The figure shows the difference of the read SNM changes for the case of

considering both the BTI effects and the SBD simultaneously and the case where SBD and the NBTI/PBTI effects are considered separately. In the latter case, the change was obtained by adding the read SNM reduction due to the SBD effect when $\Delta V_{th} = 0$ and the NBTI/PBTI effects when $R_{SBD} = \infty$. Note that the results plotted in Fig. 5 are versus R_{SBD} and obtained assuming that the increases in the MOS threshold voltages due to the BTI effects were 5% and 10%. As the figure indicates, when R_{SBD} becomes smaller (stronger SBD effect) and threshold voltage change becomes larger (severe BTI effects), the difference becomes larger. NBTI/PBTI phenomena worsens the effect of SBD on the read SNM by 16% (8%) and 31% (34%) for the 5% (10%) increase in threshold voltages due to the BTI effects for 22 and 32 nm technologies, respectively. The same behavior was observed in [13].

This behavior is due to the fact that the change in the SNM value due to SBD is a function of the threshold voltage shifts [13]. Because the coefficients for the SBD terms (a and b) are themselves functions of the threshold voltages, and hence, for a better accuracy both the NBTI and PBTI effects along with the SBD effect should be considered together. Note that the slope in Fig. 3 (λ in Eq. (29)) becomes more negative when the threshold voltage change becomes larger, and consequently, $a(-\lambda)$ becomes higher. Thus, ΔSNM due to SBD becomes more which is also apparent from Eq. (28) (in which the second term becomes larger). It is also apparent from Eq. (28) that ΔSNM due to SBD is more sensitive to a (MOS threshold voltages) as R_{SBD} decreases. In Fig. 6, we have drawn the results of the model and HSPICE simulations for the variations of λ as a function of the threshold voltage change of PL and NR for the two technologies. This graph demonstrates that increasing the BTI effects makes the SBD effect more detrimental on SNM.

Next, we plot the read SNM as a function of the stress time for the 22 and 32 nm technology. For this graph, we used the data in Fig. 2 for the V_{th} drift due to NBTI and PBTI for high- k , Eq. (3) for the SBD resistance calculation, and three arbitrary values of GR as 1.6, 3.2, and $6.4 \times 10^{-8}/s$ (we did not have access to industrial data which is process dependent). As shown in Fig. 7, different growth rates result in different times for the onset of substantial change in the read SNM.

We also study the effect of the supply voltage on the read SNM degradation. For this purpose, the read SNM values for different supply voltages versus time have been shown in Fig. 8. For these results, the changes of V_{th} due to NBTI and PBTI for the supply voltages of 0.7, 0.8 and 0.9 V have been obtained from the analytical expressions given in [25] and the SBD resistance from Eq. (3) by assuming that GR increases 5 dec/V with V_g [12]. The results show that while for smaller supply voltages the initial SNM value is lower, the rate of the SNM degradation due to NBTI/PBTI and SBD is smaller too. The accuracy degrades as the supply voltage scales more. This may be due to the assumption that all transistors operate in on state, but in lower supply voltages some transistors may

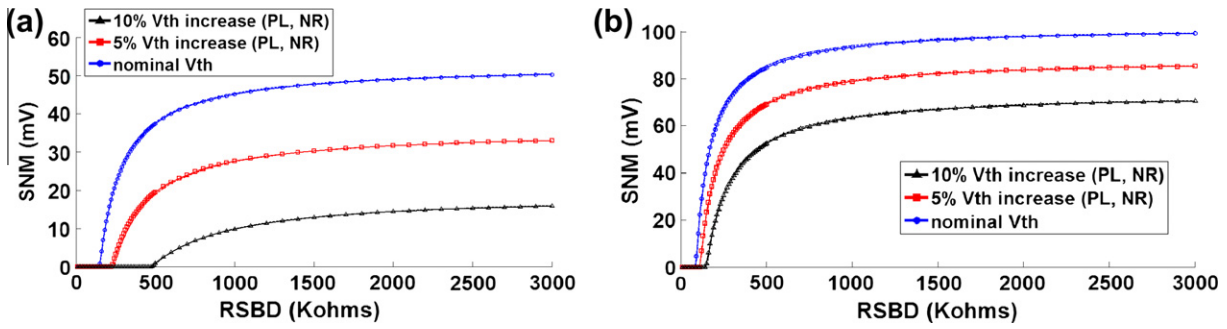


Fig. 4. Read SNM versus R_{SBD} obtained from simulations (dotted) and model (symbol) for (a) 22 and (b) 32 nm technologies with 0%, 5%, and 10% threshold voltage shifts of PL and NR.

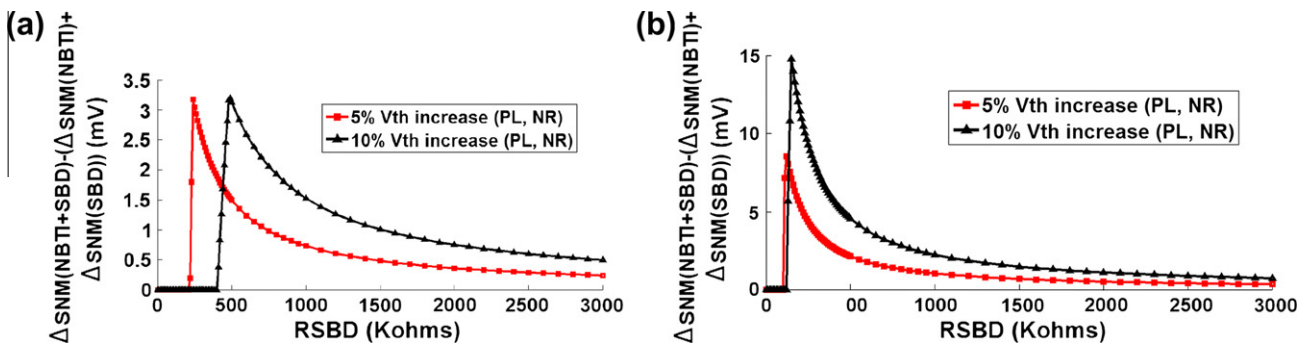


Fig. 5. The difference of Read SNM changes versus R_{SBD} when considering both NBTI/PBTI and SBD with those obtained from the addition of the read SNM changes when considering the NBTI/PBTI and SBD effects separately with threshold voltages of PL and NR as the running parameter for (a) 22 and (b) 32 nm technologies.

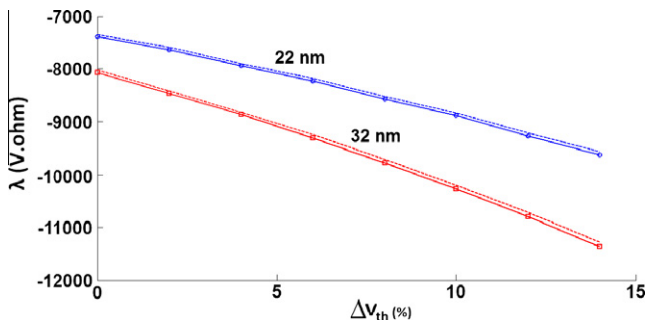


Fig. 6. λ as a function of the change in the threshold voltage of PL and NR obtained from simulations (dotted) and model (solid) for different technologies.

approach operating in subthreshold region. Even for $V_{dd} = 0.7$ V, the error is very small (the mean error for V_{dd} equal to 1, 0.9, 0.8 and 0.7 V is 1.1%, 1.5%, 1.9% and 4.5%, respectively).

Finally, Fig. 9 compares the Cumulative Distribution Function (CDF) of the read SNM versus minimum read SNM (RSNM0) obtained using 15,000 HSPICE Monte Carlo simulations and our proposed model under process variations and aging effects (NBTI/PBTI and SBD) for the 32 nm technology. We consider the threshold voltage of transistors due to process variations as Gaussian random variables [26]. The 3σ of the threshold voltages were set to 20% of their nominal values [22]. The CDF value at each RSNM0 shows the percentage of the cells whose read SNM values are smaller than RSNM0. The figure shows, for example, if the target read SNM is assumed to be 30 mV, the percentage of the cells with smaller read SNM values than 30 mV are about 0.15% and 22% initially and after 1 year, respectively. The comparison reveals a very good accuracy for the model which is evaluated in a very short period of time due to its analytical nature. Therefore, when we study the impact of process variations and aging on SRAM cell, using the proposed model is a very efficient method of calculating the read SNM compared to HSPICE simulations.

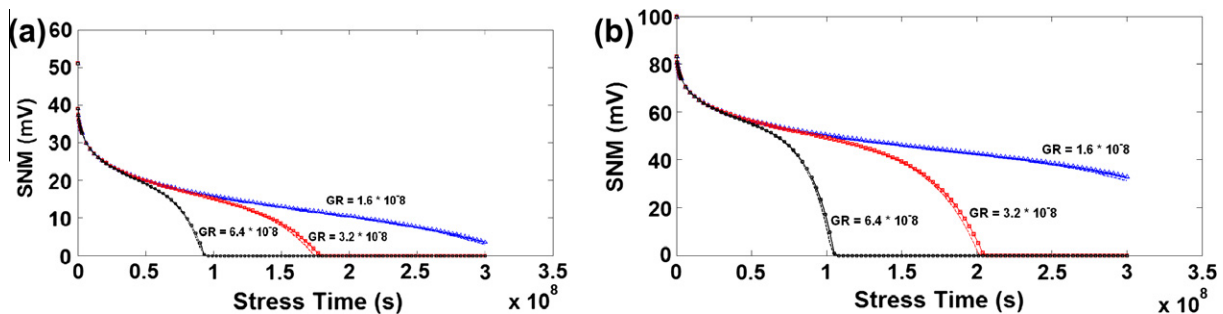


Fig. 7. (a) Read SNM from simulations (symbols) and model (solid) versus stress time for (a) 22 and (b) 32 nm technologies. GR is the running parameter.

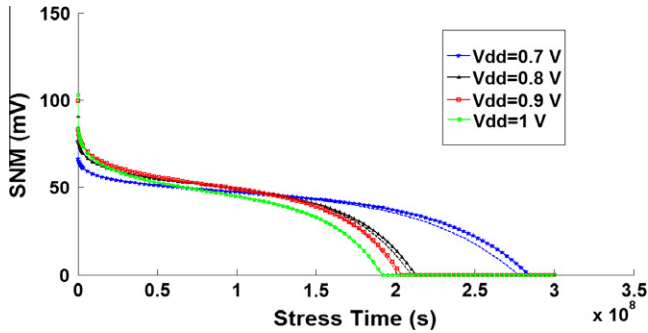


Fig. 8. Read SNM values obtained from simulations (symbols) and model (solid) versus stress time for different supply voltages for the 32 nm technology. GR is $3.2 \times 10^{-8}/s$ for $V_{dd} = 0.9$ V.

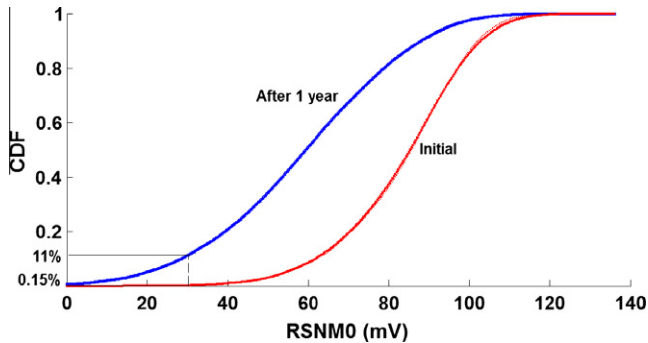


Fig. 9. CDF of read SNM obtained from simulations (dotted) and model (solid) versus minimum read SNM (RSNMO) under process variations and aging effects (NBTI/PBTI and SBD) for the 32 nm technology initially and after 1 year. GR is $3.2 \times 10^{-8}/s$ for $V_{dd} = 0.9$ V.

5. Conclusion

In this work, we proposed an analytical read SNM model which considered the soft oxide breakdown effect using an accurate model for the I - V characteristic. Both the NBTI and PBTI effects were considered in the model by including the change of the threshold voltages in the SNM model. The accuracy of the model was verified by comparing its prediction with those of HSPICE simulations for 32 and 22 nm technologies. The comparison revealed a very good accuracy for the model in these technologies. The accuracy of the model was verified for a wide range of supply voltages. The model can be used for the prediction of the minimum supply voltage which should be used for having a target yield when the lifetime is given. In addition, the results showed that both NBTI and PBTI phenomena worsen the SBD effect on the read SNM. This suggested that the effect of NBTI/PBTI and SBD should be included in the model simultaneously.

Acknowledgements

The first three authors acknowledge the financial support by the Iranian National Science Foundation (INSF).

References

- [1] International technology roadmap for semiconductors. <<http://www.itrs.net/Links/2011ITRS/Home2011.htm>>.
- [2] Omura Y. Comprehensive understanding of field-dependent conduction mechanisms of sub-4-nm-thick post-soft-breakdown SiO_2 films. *J Appl Phys* 2010;107(1):014501-1-1-9.
- [3] Degraeve R, et al. Review of reliability issues in high-k/metal gate stacks. In: Proc IPFA; 2008. p. 1-6.
- [4] Gerrer L, Ghibaudo G, Rafik M. Unified compact model of soft breakdown oxide degradation and its impact on CMOS circuits reliability. *IEEE Trans Device Mater Rel* 2012;12(1):171-6.
- [5] Cheffah S, Huard V, Chevallier R, Bravaix A. Soft oxide breakdown impact on the functionality of a 40 nm SRAM memory. In: Proc IRPS; 2011. p. CR.3.1-2.
- [6] Stathis JH. Physical and predictive models of ultra thin oxide reliability in CMOS devices and circuits. In: Proc IRPS; 2001. p. 132-49.
- [7] Schroder DK, Babcock JA. Negative bias temperature instability: road to cross in deep submicron silicon semiconductor manufacturing. *J Appl Phys* 2003;94(1):1-8.
- [8] Zafar S, Callegari A, Gusev E, Fischetti MV. Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks. *J Appl Phys* 2003;93(11):9298-304.
- [9] Yang HI, Hwang W, Chuang CT. Impacts of NBTI/PBTI and contact resistance on power-gated SRAM with high-K metal-gate devices. *IEEE Trans Very Large Scale Integr (VLSI)* 2011;19(7):1192-204.
- [10] Bansal A et al. Impacts of NBTI and PBTI on SRAM static/dynamic noise margins and cell. *Microelectron Rel* 2009;49(6):642-9.
- [11] Kang K, Kuflluoglu H, Roy K, Alam MA. Impact of negative-bias temperature instability in nanoscale SRAM array: modeling and analysis. *IEEE Trans Comput-Aided Des Integr Circ Syst* 2007;26(10):1770-81.
- [12] Qin J, Li XJ, Bernstein JB. SRAM stability analysis considering gate oxide SBD, NBTI and HCI. In: Proc IEEE IIRW; 2007. p. 33-7.
- [13] Afzal B, Ebrahimi B, Afzali-Kusha A, Mahmoodi H. Modeling read SNM considering both soft oxide breakdown and negative bias temperature instability. *Microelectron Rel* 2012;52(12):2948-54.
- [14] Chandra V, Aitken R. On the impact of gate oxide degradation on SRAM dynamic and static write-ability. In: Proc ASP-DAC; 2011. p. 707-12.
- [15] Chandra V, Aitken R. Analytical model for SRAM dynamic write-ability degradation due to gate oxide breakdown. In: Proc DATE; 2011. p. 1-4.
- [16] Gerrer L, Ghibaudo G, Ribes G. Oxide soft breakdown : from device modeling to small circuit simulation. In: Proc ESSDERC; 2009. p. 355-8.
- [17] Rodriguez R, Joshi RV, Stathis JH, Chuang CT. Oxide breakdown model and its impact on SRAM cell functionality. In: Proc SISPAD; 2003. p. 283-6.
- [18] Zafar S, et al. A comparative study of NBTI and PBTI (charge trapping) in $\text{SiO}_2/\text{HfO}_2$ stacks with FUSI, TiN, Re gates. In: Proc IEEE Symp. VLSI Technol. Dig. Tech. Paper; 2006. p. 23-5.
- [19] Cheng Y et al. BSIM3v3 MOSFET model user's manual. Berkeley, CA: Department of Electrical Engineering and Computer Sciences, University of California; 1995.
- [20] Seevinck E, List R, Lohstroh J. Static-noise margin analyses of MOS SRAM cells. *IEEE JSSC* 1987;22:748-54.
- [21] Predictive technology models. <<http://www.eas.asu.edu/~ptm/latest.html>>.
- [22] Afzal B, Ebrahimi B, Afzali-Kusha A, Pedram M. An accurate analytical I-V model for sub-90-nm MOSFETs and its application to read SNM modeling. *J Zhejiang Univ - Sci C (Comput Electron)* 2012;13(1):58-70.
- [23] Chen Q, Guha A, Roy K. An accurate analytical SNM modeling technique for SRAMs based on butterworth filter function. In: Proc ICVLSID; 2007. p. 615-20.
- [24] Bhavanagarwala AJ, Tang X, Meindl J. The impact of intrinsic device fluctuations on CMOS SRAM cell stability. *IEEE J Solid-State Circ* 2001;36(4):658-65.
- [25] Vattikonda R, Wang W, Cao Y. Modeling and minimization of PMOS NBTI effect for robust nanometer design. In: Proc DAC; 2006. p. 1047-52.
- [26] Agarwal K, Nassif S. The impact of random device variation on SRAM cell stability in sub-90-nm CMOS technologies. *IEEE Trans Very Large Scale Integr (VLSI) Syst* 2008;16(1):86-97.