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Impact of NBTI on performance of domino logic circuits in nano-scale CMOS

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ABSTRACT

Negative Bias Temperature Instability (NBTI) in pMOS transistors has become a major reliability concern in the state-of-the art digital circuit design. This paper discusses the effects of NBTI on 32 nm technology high fan-in dynamic OR gate, which is widely used in high-performance circuits. The delay degradation and power dissipation of domino logic, as well as the Unity Noise Gain (UNG), are analyzed in the presence of NBTI degradation. We have shown the degradation in the output inverter pMOS transistor of the domino gate has a dominant impact on the delay in comparison with the keeper impact. Based on this analysis we have proposed that upsizing just the output inverter pMOS transistor can compensate for the NBTI degradation. Moreover, the impact of tuning the duty cycle of the clock has been investigated. It has been shown that although the keeper and the precharge transistors experience more NBTI degradation by increasing the low level in the clock signal, the total performance of the circuit will improve. We have also proposed an adaptive compensation technique based on Forward Body Biasing (FBB), to recover the performance of the aged circuit.

1. Introduction

High fan-in domino OR circuits or similar structures are widely used in the design of register and cache array bit lines in order to achieve higher performance and compactness. However, robustness is a major concern for domino gates [1]. With technology scaling, the supply voltage is scaled down to decrease the power consumption. In order to improve the performance, the transistor threshold voltage has to be correspondingly scaled to maintain enough drive current and to avoid the performance degradation [2]. However, the threshold voltage scaling results in the substantial increase of the subthreshold leakage current [2,3].

The dynamic node of the domino gate is susceptible to noise during the evaluation phase (when the clock is high). When all the inputs of the domino gate are low, the dynamic node can still discharge due to the leakage current in the pull down network or due to the noise in the input terminals. This necessitates a keeper to hold the state of the dynamic node during the evaluation phase. The use of the keeper transistor prevents the dynamic node from discharging due to noise but degrades the performance of the gate during evaluation by providing contention current. The contention current that the keeper provides results in a short-circuit power dissipation in the keeper transistor [4] and complicates the trade-offs among power, delay and robustness. Proper transistor sizing has become one of the main challenges in timing optimization of dynamic circuits due to its effect on charge sharing, noise-immunity, process variations, leakage, etc. [5].

The DC robustness of a domino gate, corresponds to the Unity Noise Gain (UNG), which is defined as the DC input noise voltage generating an equal level of noise in the final output of the domino gate and is used as a metric of robustness [6]. There are some factors affecting the robustness in dynamic logic including high leakage current, crosstalk noise, supply noise, charge sharing and process variation and a lot of work has been done to compensate for these factors. Although NBTI has been considered as one of the design parameters for long term circuit reliability concerns, compared to the research on the above aspects, little work has been reported on the impact of NBTI on nano-scale domino gates, to the best of our knowledge.

In this paper the effects of NBTI degradation on the performance of wide fan-in OR domino gates in a 32-nm technology are analyzed and based on the results of this analysis, appropriate exploitation of NBTI mitigating techniques for dynamic logic including transistor sizing, clock duty cycle tuning and body biasing is discussed. In the developed discussions delay, power and UNG as main metrics of performance and robustness in dynamic circuits are considered.

The remainder of the paper is organized as follows. In Section 2, a review on the NBTI phenomenon is presented. The effects of pMOS NBTI degradation on the domino logic are explained based on the simulations in Section 3. In Section 4, the impact of

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upsizing the pMOS transistor in the output inverter has been investigated. The impact of the clock duty cycle tuning on the circuit performance has been discussed in Section 5. In Section 6, a compensation technique based on adaptive body biasing method is used to compensate the NBTI degradation and the corresponding simulation results are explained. Finally the conclusion is presented in Section 7.

2. NBTI degradation

Negative bias temperature instability (NBTI) is emerging as one of the major reliability concerns by technology scaling [7]. NBTI occurs when the pMOS transistor is negatively biased ($V_{gs}=-V_{DD}$) at elevated temperatures and it causes the absolute value of the threshold voltage (V_{th}) to increase. This shift in the threshold voltage can increase the delay of the transistor [8], degrade the circuit speed about 10–20% and potentially lead to a functional failure [9].

It is believed that NBTI is caused by broken Si–H bonds, which are induced by positive holes from the channel. Then H, diffuses away and positive interface traps are left, which leads to the change of V_{th} [10]. During dynamic operation of the circuit there are periods of stress and recovery. In the stress phase ($V_{gs}=-V_{DD}$), the generation of the hydrogen species and the positive interface charges (as explained) causes the absolute value of threshold voltage of the pMOS transistor to increase. During the recovery phase ($V_{gs}=0$), the interface traps can be annealed by the hydrogen species and thus, NBTI degradation can be recovered to some extent. Depending on the duty cycle and input patterns, over 75% of previous NBTI-induced degradation can be annealed by biasing the pMOS gate at supply voltage [10,11]. Therefore, the consideration of the recovery phase and its dependence on node switching activity are critical to correct analysis and design margining for the NBTI-induced degradation.

It has been shown that NBTI is independent of frequency for relatively high frequencies (more than 100 Hz) [11,12]. Based on the reaction diffusion (RD) framework [13], the increase in V_{th} due to NBTI under constant DC stress closely follows a power law with respect to time t, with a fixed exponent n and can be asymptotically expressed as $\Delta V_{th}\sim t^n$. Time exponent n represents the experimental dependency of the degradation process. Measurements have indicated a value of n between 1/6 and 1/4 for long term degradation [14,15]. For dynamic NBTI, the increase in V_{th} can be simply expressed as

$$\Delta V_{th} \approx f_{AC}(S.P)K_{DC}t^n \quad (1)$$

where K_{DC} is a technology-dependent constant that depends on the temperature, V_{DD}, the device geometry, the oxide nitrogen concentration, and other factors. Factor f_{AC} represents the AC dependency of the process, which is a function of signal (or stress) probability (S.P) [14]. Fig. 1 shows the shift in threshold voltage ($|\Delta V_{th}|$) of a PMOS transistor due to NBTI versus time for different S.P values and $V_{gs}=-V_{DD}=-0.9$ V. The graphs in this figure have been achieved by fitting Eq. (1) (with $n=0.25$) to the values presented as a bunch of graphs in [16] for a 32 nm technology at 125 °C. Using the corresponding equations resulted by fitting, the graphs have been extended in time to include longer NBTI lifetimes.

The dependence of NBTI-induced threshold voltage shift to supply voltage and temperature (which is incorporated in coefficient K_{DC} in the above equation) can be more explicitly expressed as [17,18]

$$\Delta V_{th} \propto \exp(\beta V_G)\exp(-E_a/KT) \quad (2)$$

where β and E_a are the fitting parameters, V_G is the applied gate voltage, K is the Boltzmann constant and T is the temperature.

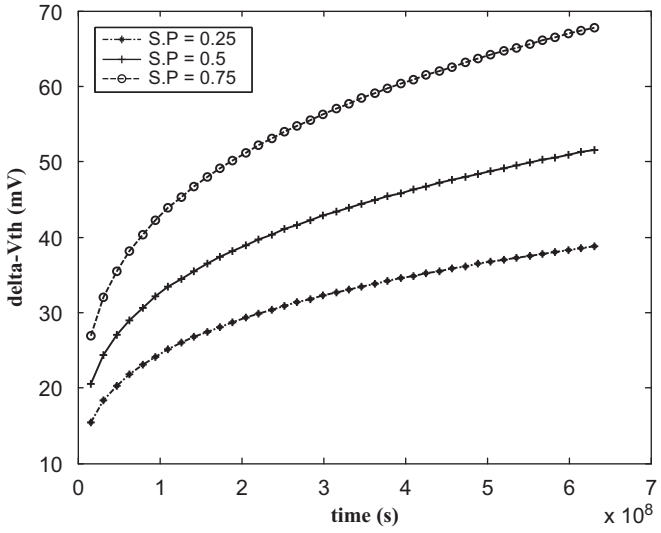

Fig. 1. Shifted threshold voltage of a 32 nm pMOS transistor versus time for different S.P values.

Considering $E_a=0.145$ eV and $\beta=0.75$ as proposed in [17] we have extrapolated the V_{th} degradation for different temperatures and different operating voltages in Fig. 2(a) and (b), respectively.

Different NBTI-aware design techniques have been proposed to mitigate the NBTI effects on circuit performance including gate/transistor sizing [19,20], V_{DD}/V_{th} dynamic adjustment [21,22], guard-banding [23], decreasing supply voltage/signal probability [24], NBTI-aware synthesis [25], input vector control (IVC) [26,27], etc.

In the following sections a wide fan-in domino gate is analyzed in the presence of NBTI and the results are used to properly utilize a few NBTI-aware design techniques for a domino gate.

3. Impact of NBTI degradation on wide fan-in domino logic: simulation and analysis

To investigate the NBTI impact on dynamic logic circuits, we have designed a commonly-used dynamic OR gate based on the standard footed domino gate (Fig. 3) having a fan-in of 8 with a supply voltage of 0.9 V and for a UNG more than 250 mV. UNG has been measured by applying a slow ramp at all inputs and doing transient simulation. The voltage that the output and the applied ramp intersect is UNG [28,29]. Fig. 4 shows the corresponding waveforms. The output inverter is skewed for fast low-to-high transition to improve performance. The capacitor load has been considered to be 10 fF. The circuit has been simulated using the 32-nm Predictive Technology Models (PTM) [30] by HSPICE at 110 °C. The aspect ratios of all devices are listed in Table 1.

If we consider a duty cycle of 50% for the clock, and an activity factor of 0.5 for the uncorrelated inputs, the keeper transistor will be under the NBTI stress for about 50% of the time intervals. In the precharge phase, the dynamic node is charged and the output of the inverter goes low making the keeper transistor stressed ($V_{gs}=-V_{DD}$). In the evaluation phase, the possibility of having a low level in the inverter output is $1/2^8$ (for an 8-input OR gate having an activity factor of 0.5), which is negligible. So we can assume that the keeper transistor is under the NBTI stress for 50% of the time intervals. The same analysis applies to the pMOS transistor of the inverter connected to the dynamic node since the dynamic node will be low for about 50% of the time intervals (mostly in the evaluation time) making this transistor to be stressed. The precharge pMOS transistor (connected to the clock)

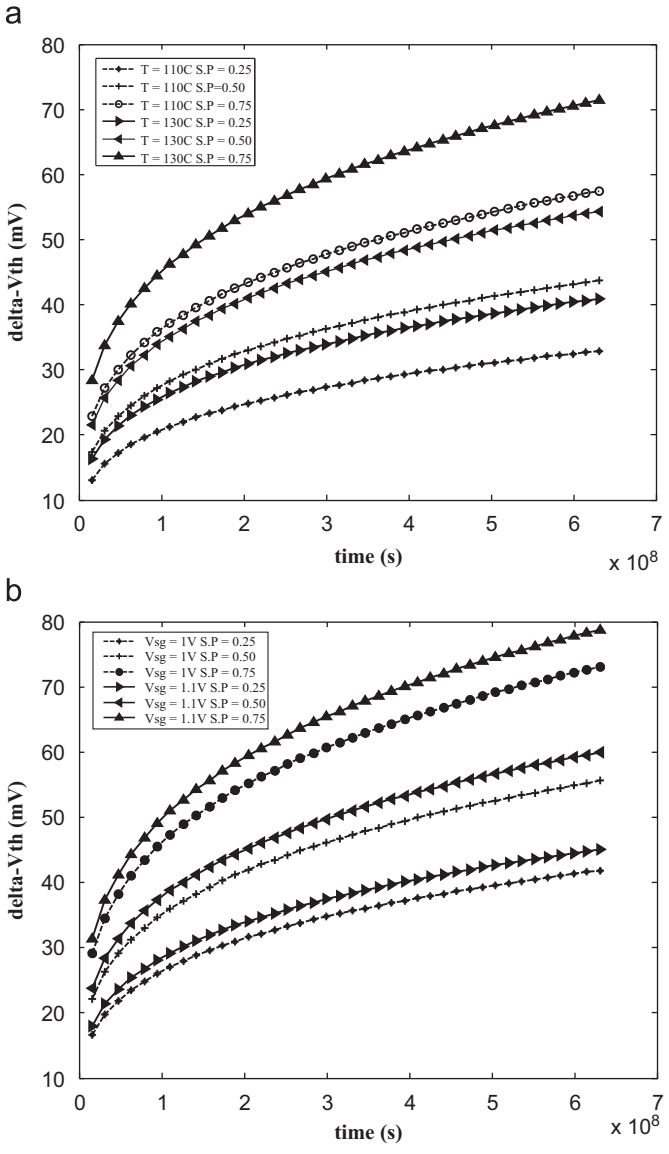

Fig. 2. Shifted threshold voltage of a 32 nm pMOS transistor versus time: for different temperatures and S.P values (b) for different stress voltages and S.P values.

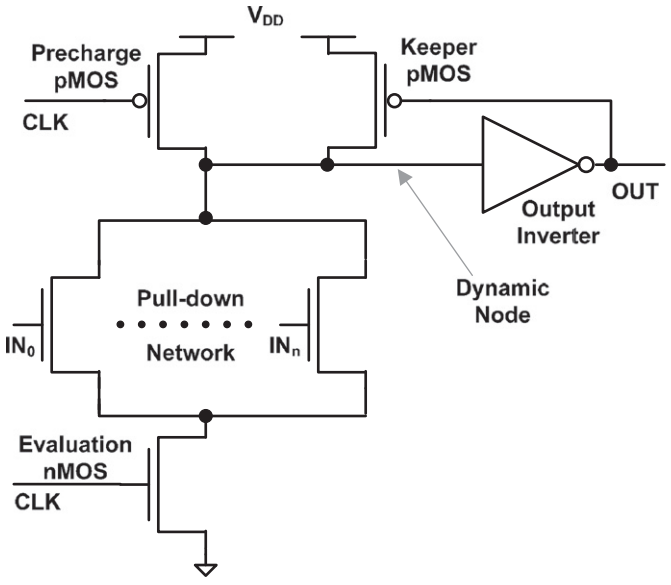

Fig. 3. Standard footed domino OR gate.

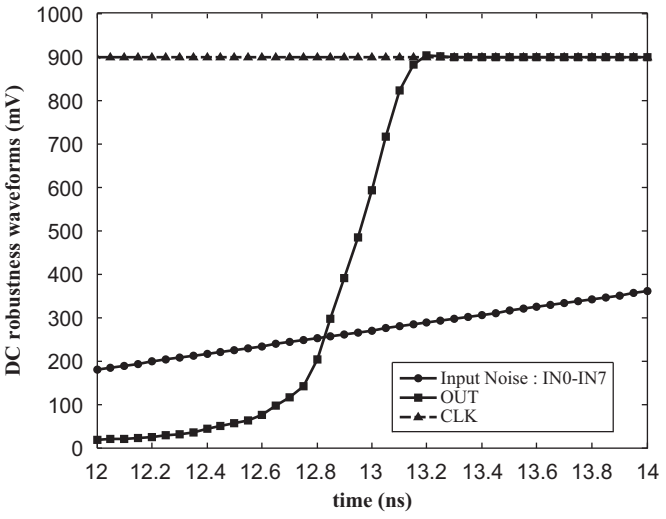

Fig. 4. UNG measurement waveforms.

is also obviously under the NBTI stress for 50% of the time intervals assuming a duty cycle of 50% for the clock. So it is expected that the NBTI degradation for all the pMOS transistors available in a wide fan-in domino logic OR gate to be equal.

To analyze the effect of the NBTI degradation for each of the pMOS transistors available in the circuit, the circuit has been simulated while considering the NBTI-induced ΔV_{th} in each of the pMOS transistors individually. Then, the circuit was simulated considering the degradation of all pMOS transistors at the same time. The main performance metrics including delay, average power and UNG of the circuit have been measured. All the simulations have been performed for different values of threshold voltage shift up to 50 mV to cover different desired NBTI lifetimes. The NBTI degradation is modeled as a voltage source in series with the pMOS gate (as shown in Fig. 5). The threshold voltage of the pMOS transistors in the used technology is 200 mV.

The percentages of change in delay, power and UNG of the circuit versus different values of threshold voltage shifts are shown in Fig. 6(a), (b) and (c), respectively. As it can be seen in this figure, when the NBTI degradation is considered only for the

Table 1
Aspect ratios of devices in the simulated dynamic gate.

	Keeper pMOS	Precharge pMOS	Pull-down nMOS	Evaluation nMOS	Inverter-nMOS	Inverter-pMOS
W/L	4	6	10	10	4	17

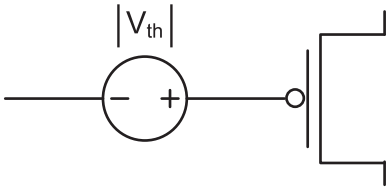

Fig. 5. NBTI model used in simulations setup.

precharge transistor, there is a negligible change in delay, power and UNG. That is because the precharge transistor is off during evaluation.

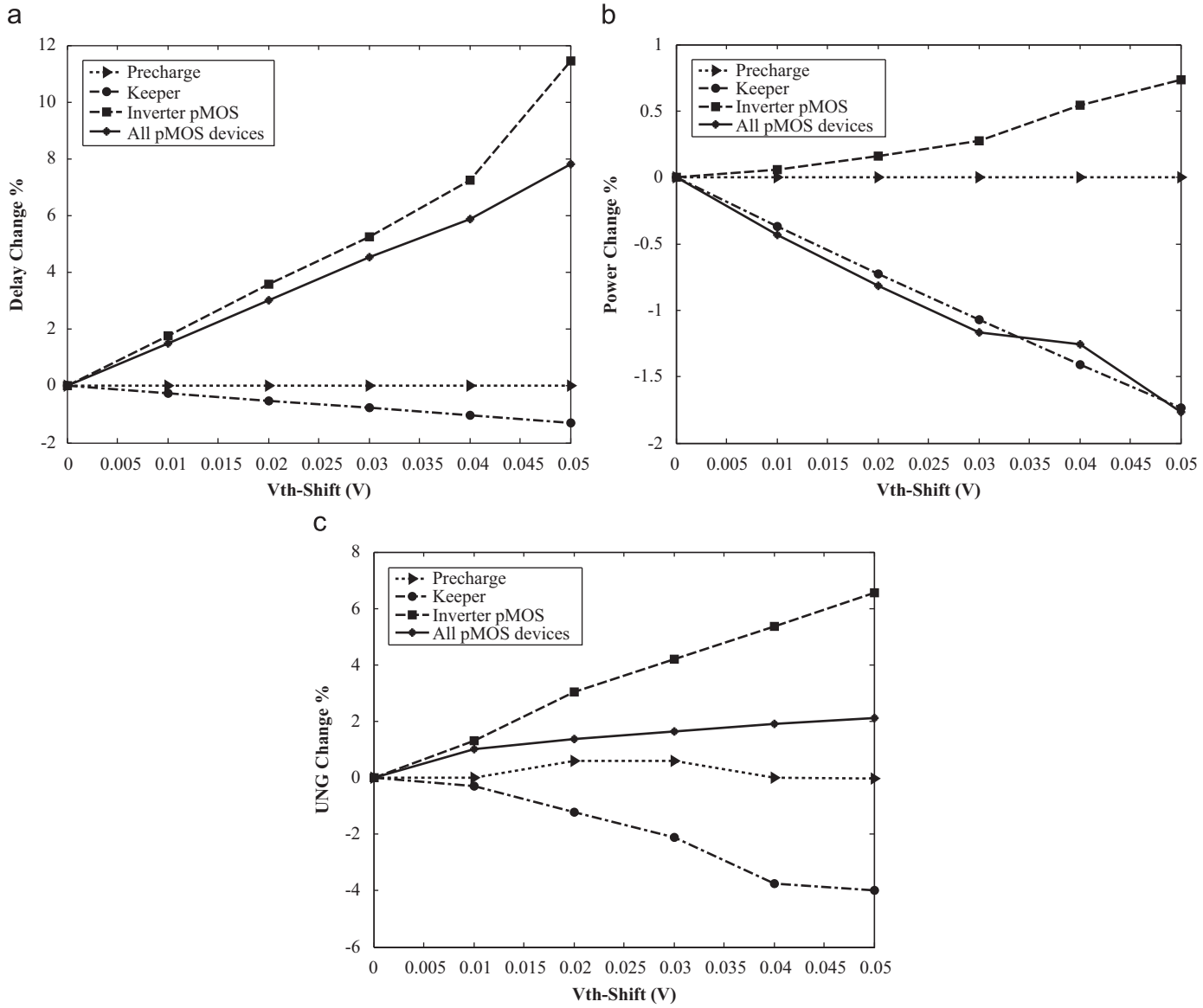

Fig. 6. Percentage of change in the performance metrics versus V_{th} shift for different pMOS devices in the circuit: (a) change in delay (b) change in power (c) change in UNG.

When the NBTI degradation is considered just for the keeper threshold voltage, simulations show a decrease in the gate delay. This is opposed to the common impact of NBTI, which increases the delay in circuits. The reason is that the NBTI degradation makes the keeper weaker leading to less contention between the keeper and the pull down network so the change in the signal will occur faster. This also decreases the average power because of the decrease in the leakage and the contention power. The UNG also decreases because the keeper has become weaker.

It is noticeable that the keeper width can change the percentage of the shift in performance due to NBTI. Fig. 7(a) shows the percentage of the delay change for different keeper widths (leading to different UNG values). In this figure the simulation results for 3 different keeper widths are shown. The second keeper width is 1.5 times that of the first keeper width and the third keeper width is 2 times that of the first keeper width. As it can be seen, increasing the keeper width leads to more decrease in delay. Besides, increasing the number of inputs in the dynamic OR gate necessitates increasing the keeper width to maintain iso-robustness (UNG $\sim$28%). This also leads to an increase in the impact of keeper degradation on the circuit delay. This situation is shown in Fig. 7(b) in which the change of circuit delay versus V_{th} shift for an 8-input OR gate is compared with that of a 16-input OR gate having the same UNG.

If the NBTI degradation is considered just for the pMOS transistor of the output inverter, average power is affected in two opposite directions. The power tends to decrease because of a higher threshold voltage in the output pMOS. At the same time, the power tends to increase because of a slower transition in the output, which makes the keeper turn off later. This leads to an increase in contention power and UNG (Fig. 6(b) and (c)). The delay also increases opposed to the impact of NBTI shift in the keeper as shown in Fig. 6(a). This can be described using a simplified model for our domino gate, which is based on the model proposed in [31]. This simple model is shown in Fig. 8.

In the figure, the keeper transistor has been replaced with a time varying current source (i_{p1}) that is controlled by the source–gate voltage of the keeper, which is affected by the output voltage. The pMOS transistor in the output inverter is similarly replaced with a time varying current source (i_{p2}) that is controlled

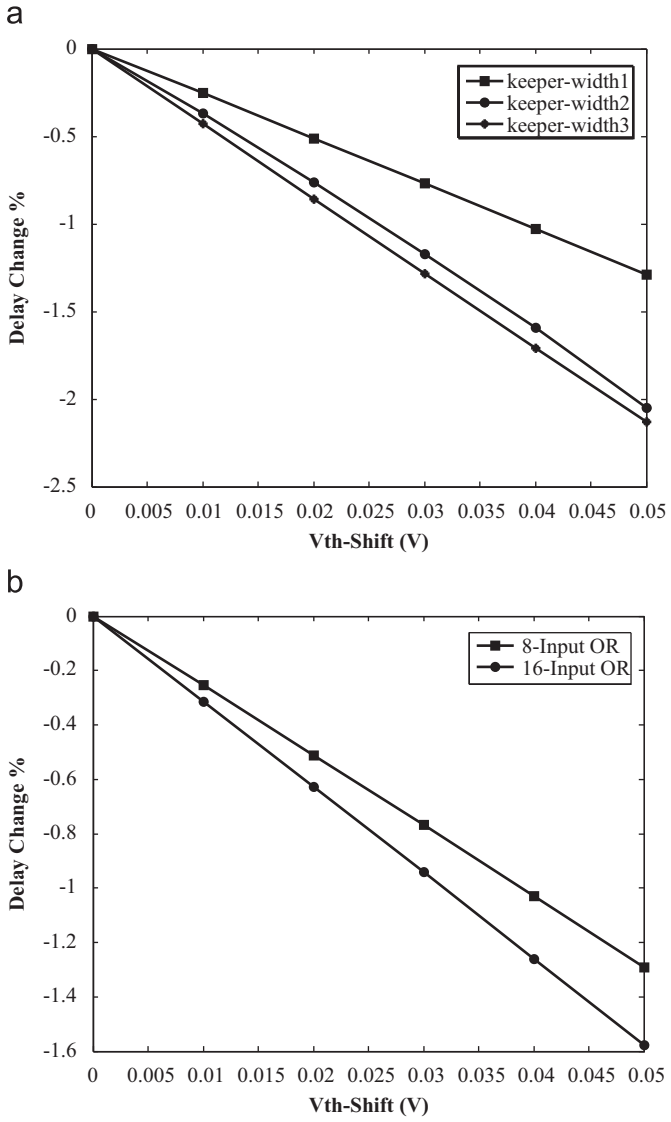

Fig. 7. Percentage of delay change versus V_{th} shift: (a) for different values of keeper widths (b) for different input numbers with the same UNG.

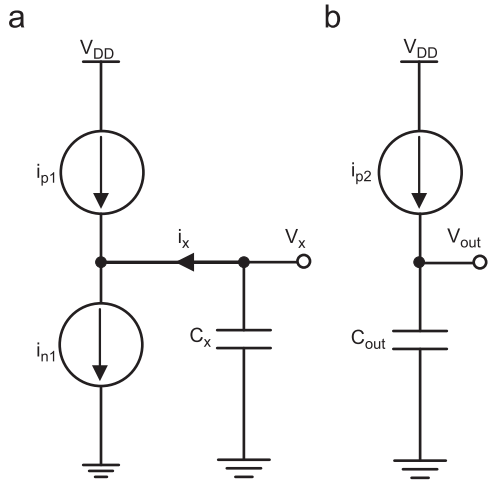

Fig. 8. (a) Simplified model of the dynamic node for a high-to-low transition. (b) Simplified model of inverter gate for a low-to-high transition of the output node.

by the source–gate voltage of this transistor. The pull-down network of the dynamic stage of the domino gate has also been replaced with a current source (i_{n1}). The precharge transistor of the dynamic stage has been removed since it is off during the evaluation phase. C_x is the capacitance at the dynamic node and C_{out} is the capacitance at the output node. The pull-down network of the output static inverter affects the charging process through its parasitic capacitances, which can be included in C_{out}. We define the discharge current of C_x as $i_x = i_{n1} - i_{p1}$.

If we consider the NBTI degradation in the keeper transistor, the current of this transistor will have a change like $-\Delta i_{p1}$ assuming that $\Delta i_{p1} > 0$. So i_x will have a change equal to $+\Delta i_{p1}$ and it leads to a decrease in the slope of V_x that is equal to

$$\frac{\Delta V_x}{\Delta t} = -\frac{i_x}{C_x} = -\frac{i_{n1} - i_{p1} + \Delta i_{p1}}{C_x} = \frac{\Delta V_x}{\Delta t}\Big|_{nominal} + \frac{-\Delta i_{p1}}{\Delta t} \quad (3)$$

According to the above equation, an NBTI-induced decrease in i_{p1} leads to a lower value of V_x at any point of time compared to the nominal value, so the gate voltage of the pMOS transistor in the output inverter is lower compared to the nominal case. Therefore, this transistor delivers a higher current and its own NBTI degradation is somehow alleviated. Consequently the delay will decrease.

Similarly, an NBTI-induced decrease in the current of the output inverter pMOS transistor ($-\Delta i_{p2}$) leads to a decrease of $-\Delta V_{out}$ slope that is equal to

$$\frac{\Delta V_{out}}{\Delta t} = \frac{i_{p2} - \Delta i_{p2}}{C_{out}} = \frac{\Delta V_{out}}{\Delta t}\Big|_{nominal} + \frac{-\Delta i_{p2}}{\Delta t} \quad (4)$$

So at any point of time there will be a decrease in V_{out} which corresponds to a decrease in the gate voltage of the keeper transistor leading to an increase in the v_{sg} of the keeper, increasing its current. This leads to a higher delay and power consumption because the contention between the keeper and the pull down network will increase. In other words, the NBTI degradation in the pMOS transistor of the output inverter makes this transistor weaker and causes the output 0-to-1 transition to be slower leading to an increase in delay. Besides, this makes the keeper turn off later in the evaluation phase (due to the explained feedback mechanism) which in turn, increases the delay. So the pMOS transistor of the output inverter has a dominant role in the total timing behavior of a domino gate in the presence of NBTI degradation.

When considering the NBTI degradation for all pMOS transistors simultaneously, the impacts of NBTI-induced degradation of the keeper on the performance metrics act opposed to the NBTI impacts of the output inverter pMOS transistor. However, the total effect is not a linear sum of the individual impacts because the NBTI-induced degradations of these two transistors have also a mutual impact on each other due to the feedback mechanism explained above.

4. Impact of upsizing

According to the analysis presented in Section 3, it can be predicted that upsizing only the pMOS transistor in the output inverter can compensate for the NBTI degradation in a domino gate since it has a dominant role in the total behavior of the domino gate in presence of NBTI. Assuming a 50 mV shift in the threshold voltage of all pMOS transistors available in our domino gate over the lifetime of the circuit, the pMOS transistor in the output inverter has been upsized about 17.8% to compensate for the NBTI-induced degradation in delay based on simulations.

The simulation results for the circuit with the upsized inverter pMOS transistor have been shown in Table 2. The delay and the power changes in this table have been normalized, respectively, to the nominal values of delay and power of the domino gate with

Table 2
Comparison between the domino gate with a normal and an upsized output inverter.

		Precharge pMOS, ΔV_{th} (mV)	Keeper, ΔV_{th} (mV)	Inverter pMOS, ΔV_{th} (mV)	UNG	Delay change	Power change
1	Domino gate with normal inverter	0	0	0	257		
2	Domino gate with normal inverter	50	50	50	263	7.81	−1.76
3	Domino gate with upsized inverter	0	0	0	253	−7.95	0.77
4	Domino gate with upsized inverter	50	50	50	258	−0.43	−1.09

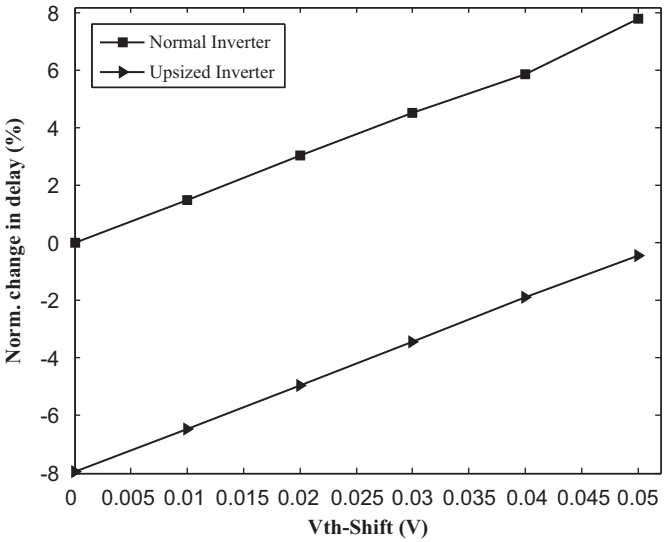

Fig. 9. Change in delay versus V_{th} shift during the lifetime of the degraded circuit.

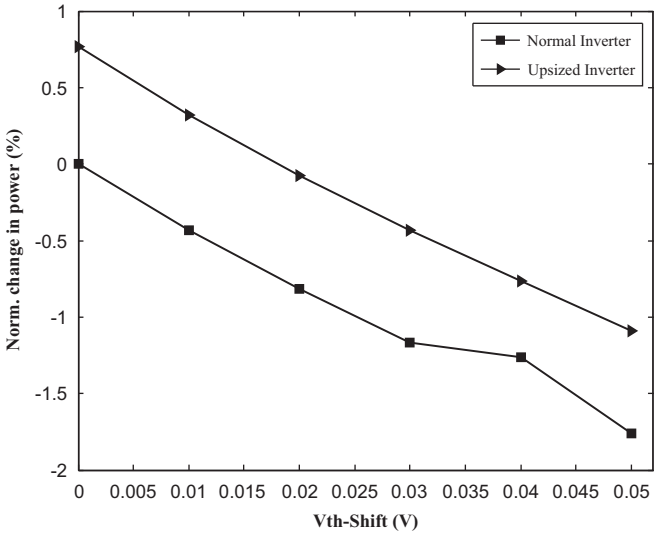

Fig. 10. Change in power versus V_{th} shift during the lifetime of the degraded circuit.

a normal inverter and without any NBTI degradation. The UNG values are normalized to V_{DD}.

The first and the second rows of this table correspond to the normal domino gate without and with NBTI degradation, respectively. The last 2 rows of Table 2 show the circuit with an upsized pMOS transistor in the output inverter without and with NBTI degradation, respectively. As it can be seen, upsizing this pMOS transistor decreases the initial delay (in the circuit without degradation) and it has a negligible impact on power and UNG. But in the degraded circuit, it can completely compensate for the NBTI-induced shifts in UNG, delay and power as predicted.

Fig. 9 shows a comparison of change in delay between the circuit with a normal inverter and the circuit with an upsized inverter versus different shift values in the threshold voltage of all pMOS transistors available in the circuit. All shift values in delay are normalized to the delay of the circuit with a normal inverter and without any NBTI degradation. It can be seen that the delay in the circuit with an upsized inverter is always less than the nominal delay during the lifetime of the circuit.

Fig. 10 shows a similar comparison for change in power. As it can be seen, there is an increase in the power consumption; however, this change (normalized to the initial nominal power of the circuit with a normal inverter) is less than 1%. Although an increase in power due to upsizing the output pMOS transistor is expected, it must be noticed that the transition of the keeper in the evaluation phase has also become faster, which leads to a decrease in the contention power and cancels out the increase of power to some extent. Moreover the power consumption decreases during the lifetime of the circuit by the induced increase in the threshold voltage of pMOS transistors. Based on our analysis and simulation results, upsizing the output pMOS transistor can be a successful NBTI mitigating technique in domino logic. However, the overhead in area and the self-loading effect (which occurs when the intrinsic capacitance of the upsized transistor dominates the extrinsic load) can limit the effectiveness of this technique.

5. Impact of clock duty cycle

The duty cycle (D.C) is usually defined as the percentage of a period when the signal stays high. Since the NBTI stress occurs when $V_g=0$ for a pMOS transistor, we define the parameter S.P (Signal Probability) as the percentage of a period when the signal level is low. The duty cycle (or S.P) affects the NBTI degradation since it changes the relative time that a pMOS transistor is under stress or recovery [32].

In a wide-OR domino gate, we changed the clock duty cycle to investigate its effect. Since the precharge pMOS transistor is directly connected to the clock, decreasing the clock duty cycle increases this pMOS transistor degradation. It also increases the duration of the precharge phase and correspondingly the percentage of the time that the dynamic node is high and the output node is low. Since the dynamic node is connected to the gate terminal of the output inverter pMOS transistor and the output node is connected to the keeper's gate terminal, the NBTI degradation of the keeper increases but the degradation of the inverter pMOS transistor decreases. In fact while the clock input is at the low level, the precharge transistor and the keeper are under stress and when the clock input is at the high level, the inverter pMOS is under stress so we have

$$\text{S.P (precharge)} \approx \text{S.P (keeper)} \approx 1 - \text{D.C (clock)} \quad (5\text{-a})$$

$$\text{S.P (inverter pMOS)} \approx \text{D.C (clock)} \quad (5\text{-b})$$

Table 3
Percentage of change in the circuit delay for different clock duty cycles.

	Clock D.C	Precharge pMOS	Keeper	Inverter pMOS	Delay Change (%)
1	0.25	S.P=0.75 ΔV_{th}=50 mV	S.P=0.75 ΔV_{th}=50 mV	S.P=0.25 ΔV_{th}=28.6 mV	3.75
2	0.5	S.P=0.5 ΔV_{th}=38 mV	S.P=0.5 ΔV_{th}=38 mV	S.P=0.5 ΔV_{th}=38 mV	5.61
3	0.75	S.P=0.25 ΔV_{th}=28.6 mV	S.P=0.25 ΔV_{th}=28.6 mV	S.P=0.25 ΔV_{th}=38 mV	8.56

We assumed a fixed lifetime corresponding to a 50 mV shift in the threshold voltage of the keeper for a clock duty cycle equal to 0.25 (or equivalently an S.P of 0.75 for the keeper). As shown in Fig. 2(a) for a temperature of 110 °C, this shift of the threshold voltage occurs at $t=3.6120\times10^8$ s. Then considering different values for the clock duty cycle, we found the corresponding S.P values for each of the pMOS transistors in the circuit based on Eq. 5(a) and (b) and used the extrapolated values of Fig. 2(a) to find the corresponding degradation values at $t=3.6120\times10^8$ s. Then the circuit delay has been measured using the HSPICE simulations. The simulation results have been shown in Table 3. In each row of this table, the change of the degraded circuit delay (in reference to the circuit delay without degradation) normalized to the circuit delay without degradation has been presented for a different clock duty cycle. As it can be seen, decreasing the clock duty cycle decreases the delay on the whole. This is because a more degraded keeper and a less degraded output inverter pMOS transistor tend to decrease the delay (as explained in Section 3). However, while decreasing the clock duty cycle, enough time must be left for the evaluation phase of the domino gate.

6. Impact of forward body biasing (FBB)

The upsizing technique (explained in Section 4) is a one-time solution adding adequate guard-band at design time. During the initial stages of the circuit operation, the added positive slack is more than necessary. On the other hand, NBTI causes the transistor threshold voltage to increase over time, resulting in larger delay but a lower subthreshold leakage (I_{SUB}) because $I_{SUB}\propto\exp(-V_{th}/mkT)$. This provides the opportunity to trade-off the slack in leakage to restore the degraded performance based on adaptive body biasing (ABB).

The MOS threshold voltage is dependent on its source–body voltage (V_{SB}) and if $|V_B|$ is less than $|V_S|$, the resulting FBB will cause the threshold voltage to decrease thus compensating for the NBTI effect and speeding up the circuit [33]. It is possible to determine the amount of required FBB based on the exact temporal degradation of the circuit, and hence necessary amounts of body bias can be adaptively applied, to exactly meet the target specifications under all conditions.

We have utilized this technique in the previous 0.9-V circuit. The circuit has been simulated to find the appropriate FBB needed to compensate for different shift values in the threshold voltage. The results have been shown in Fig. 11. As it can be seen, there is almost a linear relationship between the required FBB and the corresponding shift in the threshold voltage as expected in the deep submicron technologies.

If the most required FBB in the circuit lifetime is applied from the beginning instead of incrementing it over time, simulations show a decrease of 5.01% in UNG and an increase of 3% in power (in comparison with the nominal values) in the initial stages of the circuit operation. But using the appropriate ABB, the changes

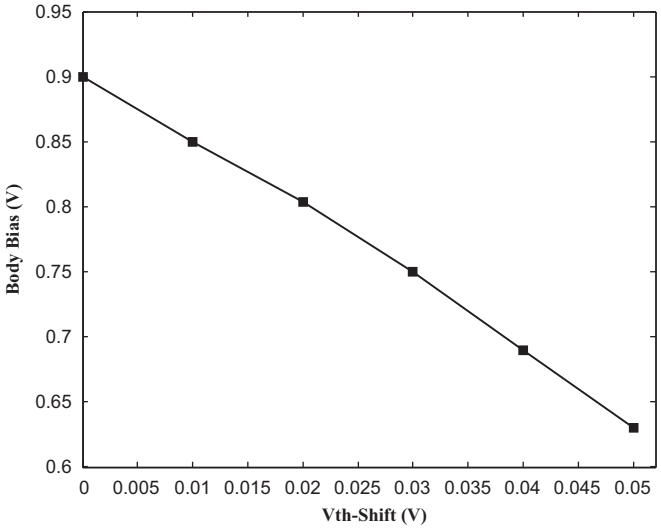

Fig. 11. Required body bias versus the NBTI degradation.

in power and UNG during the entire circuit lifetime are completely negligible.

The value of the FBB voltage required to compensate for the NBTI degradation can be applied adaptively using a look-up table and a timer in different time stamps as proposed in [22] . The shift in the threshold voltage due to NBTI can be calculated based on the formulations corresponding to a specific technology and the required FBB values are stored in the look-up table. The entries in the look-up table are indexed by the total time for which the circuit has been in operation. This time can be tracked with $t0$ representing the beginning of the lifetime of the circuit (say after burn-in, testing and binning). The timer control enables the system to determine the total time for which the circuit has been in operation. Since it is impossible to determine the exact temporal degradation of a circuit in advance, it is proposed to compute the worst-case degradation of the circuit, at different time stamps and then find the amount of the compensation voltage required to be adaptively applied at those time stamps, to meet the target delay.

7. Conclusion

The impact of NBTI on the performance, power and noise margin of a 32-nm high-fan in domino OR gate was investigated. It has been shown that the NBTI-induced degradation in the keeper transistor decreases the delay and power consumption at the expense of a decrease in the UNG. However, the NBTI-induced degradation of the output inverter pMOS transistor affects the circuit in an opposite direction and increases the delay and power of the domino gate on the whole and has a dominant effect. Based on this result, it has been shown that upsizing just the inverter pMOS transistor can compensate for the NBTI degradation, although area overhead and self-loading effect are the concerns, which must be considered.

The impact of the clock duty cycle tuning has also been investigated and it has been shown that it has an opposite effect on the keeper and the precharge transistor from one side and the output inverter pMOS transistor from the other side. It has been shown that decreasing the duty cycle can improve the performance on the whole. However, this technique is restricted to the minimum required evaluation time for the domino gate.

Finally it has been shown that adaptive body biasing technique can be exploited to compensate for NBTI degradation too. This

technique avoids the area overhead of upsizing, but requires a mechanism to adaptively produce and apply the required body bias.

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