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Arbitrary Two-Pattern Delay Testing Using a Low-Overhead Supply Gating Technique

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Abstract With increasing defect density and process variations in nanometer technologies, testing for delay faults is becoming essential in manufacturing test to complement stuck-at-fault testing. This paper presents a novel test technique based on supply gating, which can be used as an alternative to the enhanced scan based delay fault testing, with significantly less design overhead. Experimental results on a set of ISCAS89 benchmarks show an average reduction of 34% in area overhead with an average improvement of 65% in delay overhead and 90% in power overhead during normal mode of operation, compared to the enhanced scan implementation.

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1 Introduction

Delay faults in a circuit occur when a net functions properly but fails to meet timing requirement. Delay faults are sometimes caused by defects that are not large enough to cause a stuck-at failure by changing logic level, but affect the signal propagation time. With increasing defect density and unanticipated process variations [2], delay failures are getting more likely to arise in sub-100 nm technologies. Therefore, it is becoming mandatory for manufacturing test to cover not only stuck-at faults, but delay faults as well [9–11].

Scan architectures provide an efficient way to test for delay faults with good fault coverage. Scan-based structural delay testing not only helps detection but also diagnosis of delay faults [9] and, hence, is a popular choice for delay fault testing. However, testing for delay faults requires launching a transition at the input of the Circuit Under Test (CUT), and capturing the response of the circuit at rated clock. Although it is easier to apply a transition at the primary inputs (PIs) of the CUT by the tester, it is not straight-forward to make a transition at the state inputs. Based on test application procedure, there are three prevalent techniques for scan-based delay testing. In the first one, called *broad-side* delay test, no transition is applied to the state inputs. State portion of the second pattern is derived as the combinational circuit's response to the first pattern. Although, the testing process is simple and it does not require any additional Design-For-Testability (DFT) logic, the *broad-side* case can suffer from poor

fault coverage [15, 22]. In the second method, referred as *skewed-load* delay testing, transition in the state inputs is induced by shifting the scan values by one bit position. However, design requirement for *skewed-load* case can be costly because of fast switching scan enable signal [22]. Moreover, since the second pattern (launching pattern) is highly correlated to the first one (*initialization pattern*), the test generation for high fault coverage can be difficult [3].

The third approach, referred as *enhanced scan* method, allows easy application of a state transition and enables deterministic choice of any launching pattern in the scan flip-flops for best possible fault coverage [3, 8, 15, 16]. Enhanced scan method improves fault coverage for all delay fault models, however, it is particularly useful for path delay fault testing, where a set of critical timing paths need to be sensitized and tested for delay violations. For a sequential circuit with enhanced scan, we can use a combinational path delay test generation algorithm to generate delay tests, which helps to achieve high fault coverage with short test generation time [8, 14, 16]. Although enhanced scan has high combinational path testability, it involves high DFT overhead due to addition of an extra latch, named as hold latch, at the output of each scan flip-flop to hold the initialization pattern [3]. The latch resides in the stimulus path between the scan flip-flops and the combinational logic (as shown in Fig. 1) and can considerably affect circuit performance during normal mode of operation. Adding to the overhead, the latch takes up significant amount of die-area and consumes power in normal mode. Figure 1b also shows a multiplexer-based holding logic which can be used in place of a hold latch. There have been a large number of investigations to devise alternative delay fault testing strategies with reduced DFT overhead and acceptable coverage [5, 19, 20, 22]. However, these techniques are either not as efficient as enhanced scan method with respect to fault coverage and required number of test patterns, or they complicate the test generation/application considerably.

It can be argued that the higher coverage achieved by enhanced scan approach is contributed by paths which are not sensitizable in normal operation [17]. On the other hand, functional justification or broadside approach, although has lower fault coverage, is capable of covering paths that can be functionally sensitized. However, with increasing defects per million (DPM) rate in nanometer technologies [13], high coverage assists in failure analysis, yield learning and consequent improvement in DPM [13]. Higher coverage also helps to reduce test length and test data volume, which are important parameters in external ATE based testing. Moreover, enhanced scan approach has the intrinsic benefit of power reduction during test application (due to prevention of switching propagation to combinational circuit).

The Level Sensitive Scan Design (LSSD) [6, 7] is a test scheme for sequential designs, that can be used for enhanced-scan-like arbitrary two-pattern test application. Several alternative implementations of LSSD have been explored for enhanced-scan-like test application [23, 24]. Compared to muxed scan approach, LSSD has the advantage of isolating the functional flip-flop from the scan path. However, LSSD uses extra latches per input flip-flop [6] resulting in considerable area and power overhead. Although the extra latch is not in the signal propagation path, the extra loading on the first

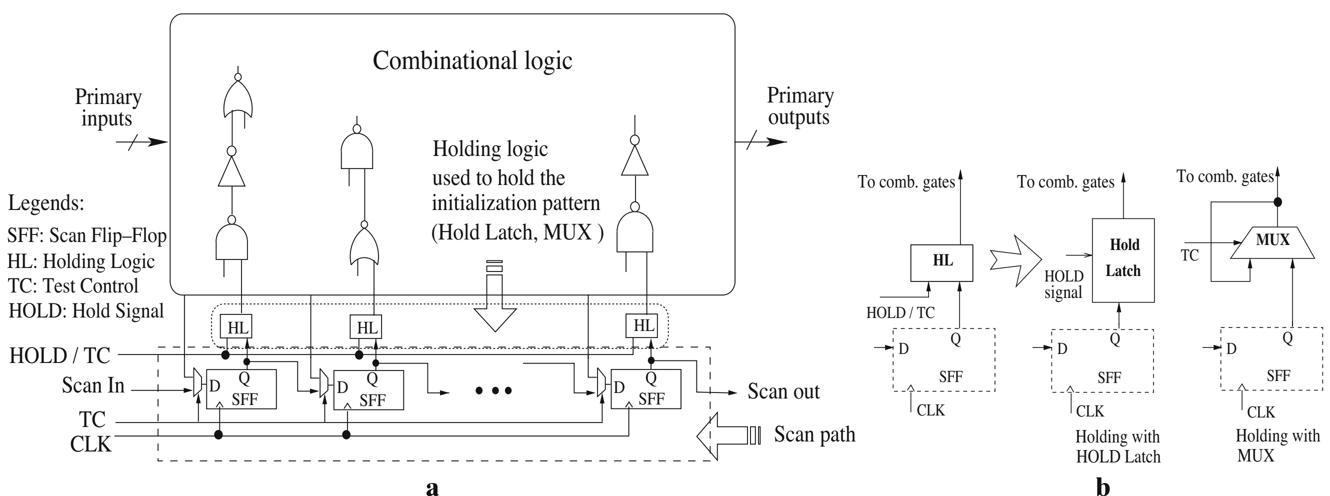

Fig. 1 **a** Scan architecture with additional logic for delay fault test. **b** Holding logic

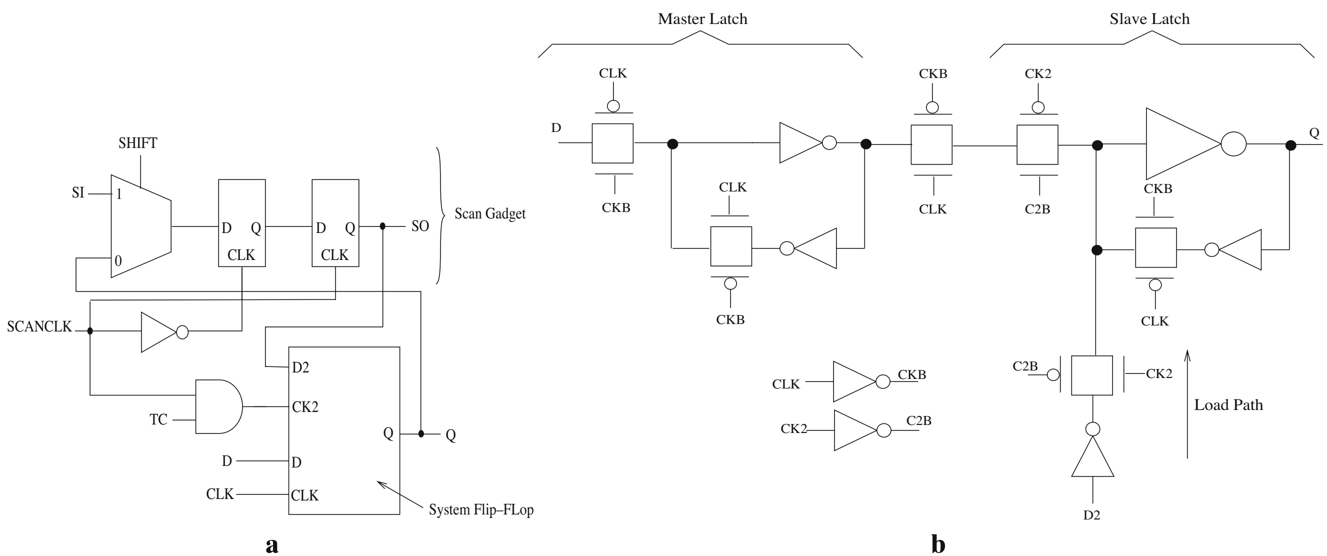

Fig. 2 **a** HSSG scheme. **b** Implementation of system flip-flop of the HSSG scheme

latch (due to the additional DFT hardware) increase power and delay of the system flip-flop. A recently proposed scan design by Intel [14], based on hold-scan, uses a scan gadget along with the system latch as shown in Fig. 2 (hereafter, we refer to this technique as Hold Scan using Scan Gadget or HSSG scheme). The scan chain is implemented by scan gadget element, which provides the basic scan test functions (shift, load, and capture). In this scheme, two extra latches added for the scan chain implementation do not switch during the normal mode, however they add to the leakage power and area overhead. More importantly, the system flip-flop is a more complicated flip-flop with two clock and two data inputs, one for system operation and the other for loading to/from the scan chain. A master-slave implementation of the system flip-flip of the scan gadget scheme is shown in Fig. 2b. The internal circuit for the flip-flop is provided in [14], but we designed a flip-flop for this purpose, which is optimized as suggested by our industry contact. The connection from the second input to the slave latch for load function is implemented by a transmission gate. This extra circuitry adds to the system flip-flop power in the normal mode of operation.

Muxed scan and LSSD both have some advantages and disadvantages and the choice of either of them depends on several design constraints (on die-area, delay, time to market etc.). In this paper, we propose a circuit technique alternative to enhanced scan, which allows enhanced scan-like test application, but comes at a much lower hardware overhead. The technique is suitable for muxed scan implementation. We refer the technique as First Level Hold (FLH) that employs the principle of "supply gating", in a novel way, to hold the state of combinational logic. Instead of holding the initialization pattern at the scan-hold latch as done in the case of enhanced scan [3], we hold the state of the combinational circuit in response to the first pattern by gating the VDD and GND of the first level gates.

Earlier, we have proposed application of supply gating for low-power scan design [1]. However, the technique in [1] is targeted towards test power reduction and cannot be applied to arbitrary two-pattern delay fault testing since it does not hold the state of the combinational logic in response to an initialization pattern. In this paper, we propose a design technique based on the concept of supply gating that allows enhanced-scan-like test application. We use two extra transistors, one in the pull-up and the other in pull-down, to "gate" the supply lines for the first level logic gates during scan shifting, thus, cutting off any charge/discharge path for the output logic level of the gates. Hence, the output state of the first level logic gates at the fanout cone of the scan flip-flops hold their state, irrespective of the activity in the scan registers due to rippling of scan values. Once the first level logic gates hold their states, the other levels also retain their states, since no signal activity propagates to them. Test application remains as in enhanced scan approach, except that the control for holding state is now moved from the hold latches to the gating control of the first level logic.

FLH does not require any extra control signals and does not change the test generation/application process. Moreover, unlike enhanced scan test, it does not introduce extra level of logic in the timing path of a

circuit and hence, the delay overhead reduces greatly compared to the enhanced scan. We have compared FLH technique with enhanced scan method (based on hold latch) and the 4-latch version of hold-scan [14]. Experiments performed on a set of ISCAS89 benchmarks show superior results with FLH in terms of area, delay, and power overhead compared to the alternative methods. It is worth noting that FLH also maintains the power-saving advantage of enhanced scan in the test mode, since it prevents redundant switching in the combinational block by isolating it from the activities in scan register.

The rest of the paper is organized as follows: Section 2 illustrates the proposed gating technique for delay testing. Section 3 describes scan architecture using FLH. Section 4 presents comparison results in terms of area, delay, and power for a set of benchmark circuits. Section 5 explains the test power saving capability of the proposed technique. Finally, Section 6 concludes the paper.

2 FLH for Delay Fault Test

The requirement of enhanced scan based delay fault testing is to apply a transition at the state inputs of a combinational block by holding its output state in response to the initial pattern before applying the second pattern. This can be achieved by adding a hold latch as in the enhanced scan at the input of the combinational circuit (Fig. 1). We propose to apply supply gating (using sleep transistors) in the first level of logic and thereby achieving enhanced-scan capability. Supply gating by sleep transistor insertion has evolved as a powerful means to reduce the circuit leakage [18]. In this technique, a series-connected transistor is inserted in the pull-down (a NMOS) and/or pull-up (a PMOS) path. This extra transistor is known as the sleep transistor. During the normal mode of operation the sleep transistors are turned on to ensure correct operation, and in the stand-by mode they are turned off to reduce the circuit leakage. An illustration of such a sleep transistor technique is shown in Fig. 3. Here, we use supply gating for the purpose of delay fault testing.

Putting the first level of gates in the sleep mode during the scan shift prevents switching propagation throughout the combinational logic and maintains the state of the circuit. Figure 4 shows sleep transistors with supply gating applied to a first level logic gate for a cascade of inverter gates.

In order to understand if a gate in the sleep mode can retain its output voltage level despite input switching, let us consider the circuit in Fig. 4 with IN at '0' and OUT1 at '1' when the SLEEP signal is applied (SLEEP switches to high). When the SLEEP signal is '1', the node OUT1 is floated since there is no path to VDD or GND from this node. In this case, the voltage of OUT1 can remain at '1' due to the charge that is held in that node. However, since OUT1 is floated, the charge held in OUT1 node can leak due to leakage of transistors connected to that node. This leakage include the sub-

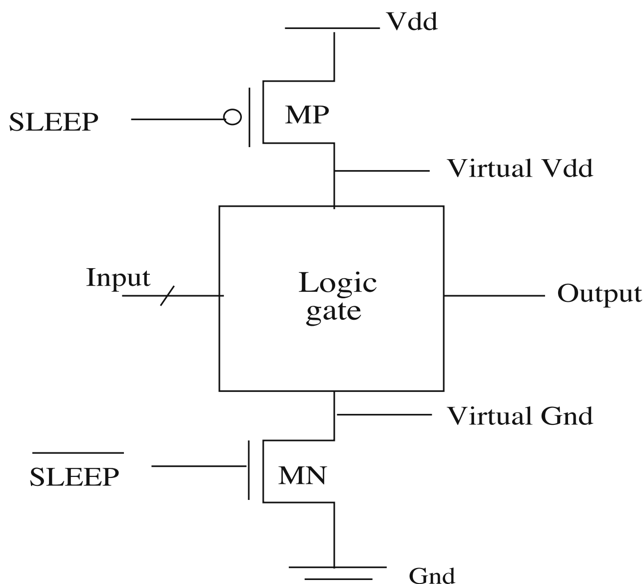

Fig. 3 Sleep transistor for leakage power reduction in standby mode

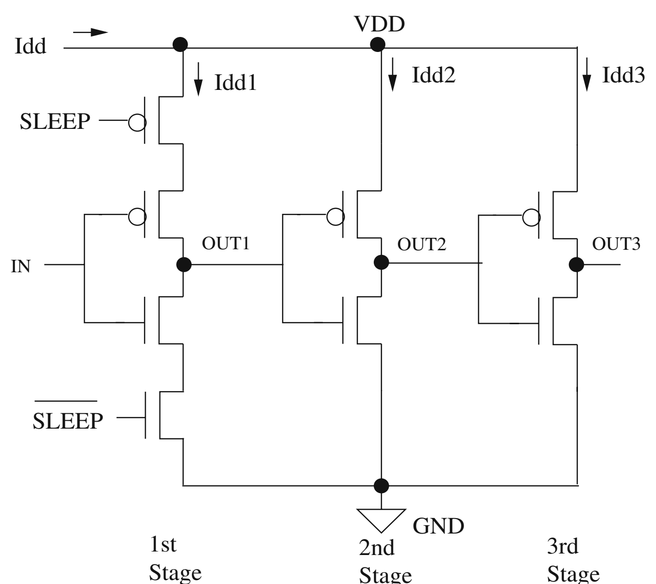

Fig. 4 Supply gating applied to first level gate

threshold leakage of the sleep transistors and the gate leakage of the pull-up and pull-down networks as well as the gate leakage of the following inverter connected to node OUT1. This charge leakage can result in a change in the state of OUT1 node. This is particularly aggravated if IN switches to ‘1’ in the sleep mode and stays at ‘1’ for a long enough time. This scenario is simulated in *Hspice* for the circuit shown in Fig. 4 using the 70 nm Berkeley Predictive Technology Models [21]. Figure 5a shows how OUT1 voltage gradually decays and settles down at some intermediate voltage level. As observed, the voltage of OUT1 falls below 600 mV in less than 100 ns.

Assuming a scan chain of 1000 flip-flops and a scan frequency of 250 MHz, the time to scan a vector is 4 μs, which is much longer than 100 ns. The voltages of the outputs of the inverter chain for this scenario are shown in Fig. 5a. If the voltage of the output of a first level gate is not at VDD or GND, this could cause static short circuit current on the following logic gates being driven by the first level gate. As OUT1 slowly decays below $Vdd - Vth$ (Fig. 5a), in the second inverter (Fig. 4), both the PMOS and NMOS transistors get turned ON causing static short circuit current to flow through this inverter (Idd2 in Fig. 5b). Consequently, the output of the second inverter (OUT2) rises resulting in static current on the third inverter (Idd3). If OUT1 decays below the trip point of the second gate, a switching also occurs on the second gate as shown in Fig. 5a. This results in a change in the state of the circuit. Moreover, as observed from Fig. 5b, this could result in significant static short circuit current in the sleep mode. Although the voltage rise/drop decrease as it propagates through the logic gates, the continuous flow of short circuit current in the gates at second stage could result in high power dissipation.

Therefore, the principal issue associated with this scheme (Fig. 4) is that the outputs of the first level gates are floated in the sleep mode. The voltage of a floated output is determined by the leakage balance between the pull-up PMOS and pull-down NMOS network of the gate. The leakage impact can be reduced by using high Vth sleep transistors. However, this may not still guarantee a holding of state since the leakage exponentially increases with temperature and technology scaling. Using high Vth sleep transistor will impose more delay penalty for the first level gate as well. In addition to leakage, crosstalk noise or transient effects due to soft error can also easily change the voltage of a floated output. Crosstalk noise can particularly occur in this circuit because the switching of input (IN) can couple to OUT1 through the gate-to-drain capacitances of both PMOS and NMOS transistors of the first level gate (MP1 and MN1 in Fig. 4). Moreover, the switching of the inputs can result in charge sharing between the floated output node and intermediate nodes of the NMOS or PMOS network in complex gates resulting in change of the output voltage.

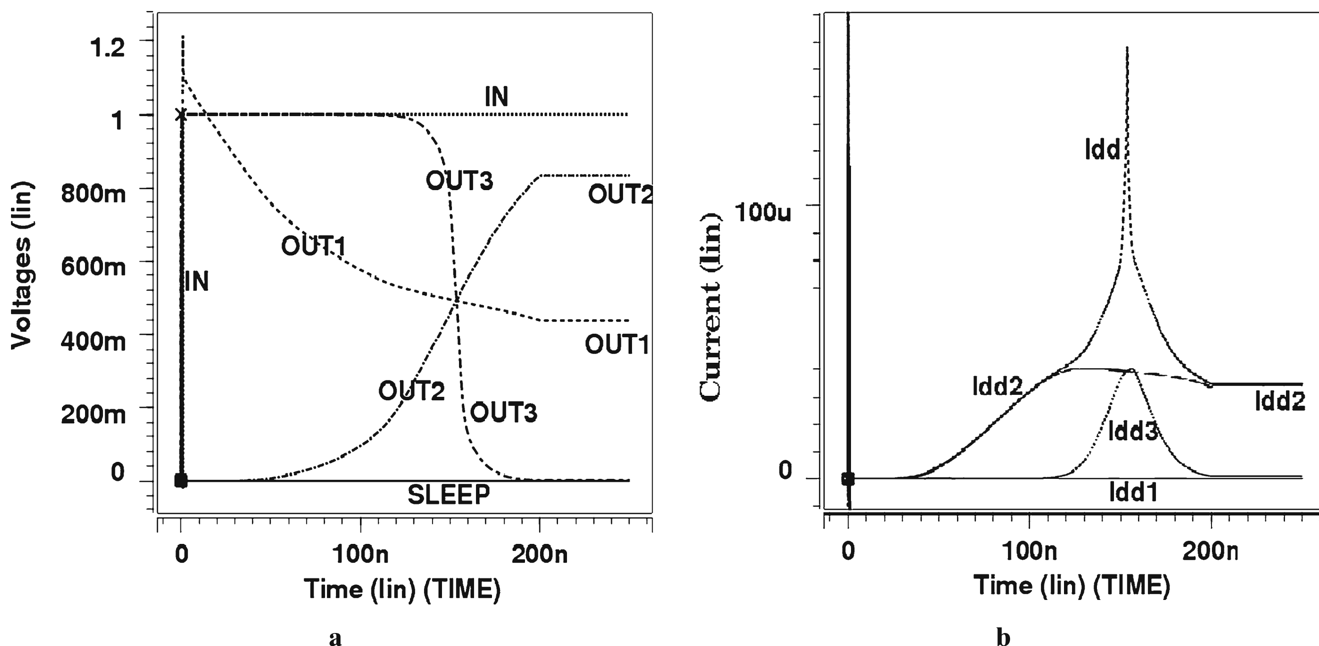

Fig. 5 State holding failure of the circuit in Fig. 4: **a** Voltage and **b** Current waveforms in sleep mode

In order to avoid floated nodes in the sleep mode and ensure hold capability, the outputs of the first level gates need to be forced to VDD or GND, depending on their initial logic state. This can be achieved by adding a latch element (cross-coupled inverters) at the output node. The latch element needs to be enabled only in the sleep mode to hold the output state of the first level gate. The general scheme of the proposed supply gating scheme is shown in Fig. 6. The two inverters, INV1 and INV2, form a cross-coupled inverter loop if MN1 and MN2 are ON. In the sleep mode (TC='0'), MN1 and MN2 are ON and the inverter loop holds the state of the output node. In the normal mode (TC='1'), however, these transistors are off and the gate can control its output. Therefore, in this scheme, the output of the gate never gets floated and there cannot be any static short circuit current on the next stage gates in the sleep mode. The proposed scheme is called "FLH" since only the first stage is set in the hold mode. In the proposed scheme, the inverters (INV1 and INV2) and MN1, MN2 can use minimum-sized transistors to minimize their impact on area, circuit delay, and power during normal mode of operation. Minimum-sized inverters are large enough to be able to hold the state of the output node in the hold mode despite the presence of leakage and noise. Use of minimum-sized transistors for the latch element reduces loading on the outputs of first level gates, resulting in minimal delay and power penalty. The size of the supply gating transistors can be optimized for delay under the given area constraint.

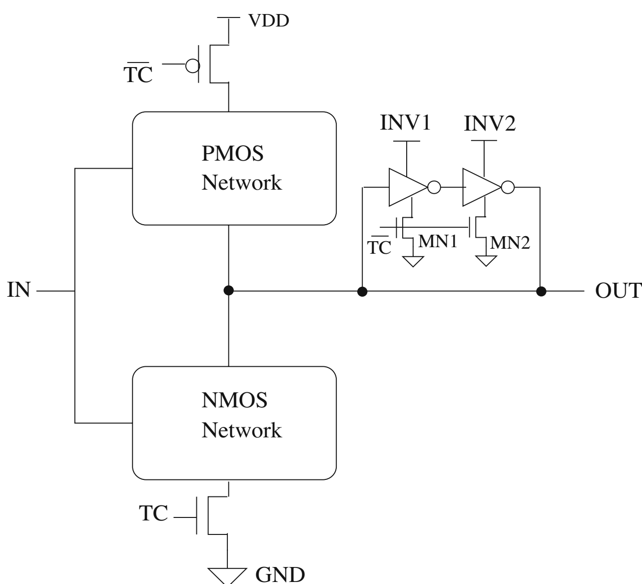

Fig. 6 Proposed supply gating scheme with output hold capability

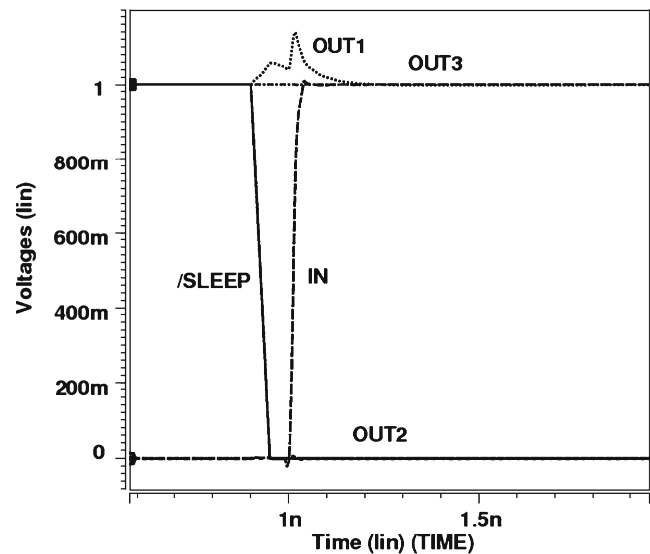

Fig. 7 Simulated waveforms of the circuit in Fig. 4 with the proposed supply gating scheme applied to it

Figure 7 shows the simulated waveforms of the FLH scheme applied to the inverter chain in Fig. 4. As observed from the waveforms, the circuit can strongly hold its state (OUT1, OUT2, and OUT3) despite the switching at the input (IN).

3 Scan Architecture Using FLH

Figure 8 shows the proposed FLH technique applied to a general sequential circuit. FLH does not require any extra timing control signals. It only requires the test control (TC) signal, that is used in conventional scan-based testing, and its complement ($\bar{TC}$). Enhanced scan method also requires two control signals, TC and HOLD, as shown in Fig. 1. The timing diagram during test application is shown in Fig. 8b. During scan-in, TC is set to '0' to prevent activity in the scan chain from affecting the combinational circuit. Once scan-shifting is completed for the first pattern (V1), it is applied to the combinational circuit by turning the gating transistors on, while the PI bits are applied. After the combinational circuit stabilizes, the second pattern (V2) is scanned-in while V1 is held since the gating transistors in the first level gates are turned off. Next, the transition is launched by activating TC and applying the PI bits. Finally, the results are latched after one rated clock period.

3.1 Synchronization of Launching Signals

An important issue for both enhanced scan and FLH methods is the synchronization of the vector launching signal (TC/Hold in Fig. 1 and TC/$\bar{TC}$ in Fig. 8) and the capturing clock, which is the system clock (CLK). Any delay skew between the vector launching signal and capturing clock increases or decreases the time left for signal propagation in the combination block, resulting in inaccuracy of the delay fault testing. If the vector launching signal arrives later than the clock edge, the actual time left for the combination block would be less than the clock cycle time, and therefore, the delay test would be pessimistic. On the other hand, if the vector launching signal arrives earlier than the clock edge, it may result in a loss of the state of the circuit because the second vector has not been completely shifted yet (the last shift of the second vector happens on the clock edge on which the second test vector should be applied too). The vector launching signal is generated on the clock edge by an edge-triggered circuit. In case of FLH, since the clock has to propagate through the clock tree to reach the local flip-flops and then there is clock-to-output delay of flip-flops before the second vector settles down at the outputs of the flip-flops, the overall delay from clock edge to the completion of the

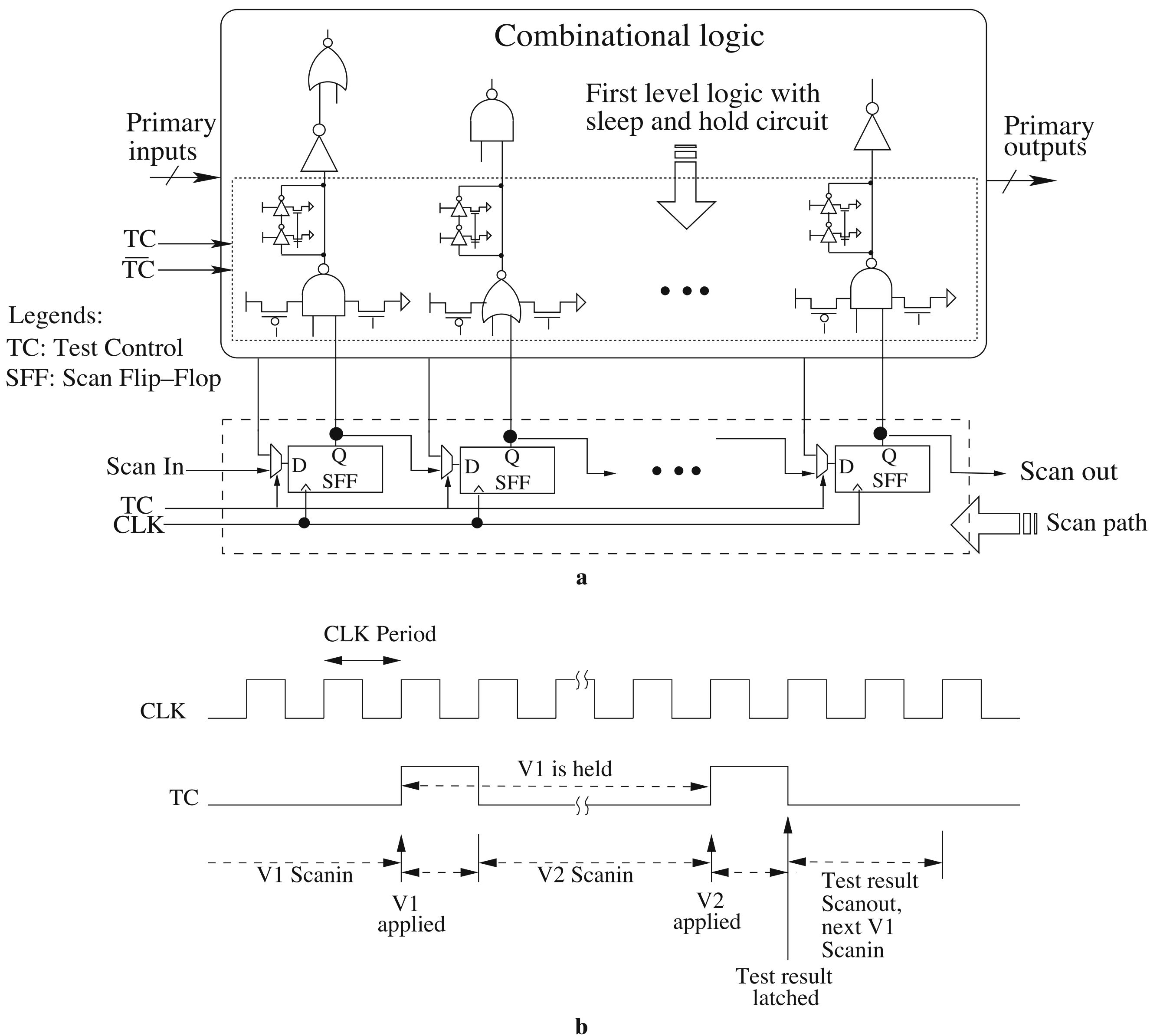

Fig. 8 **a** Modified scan architecture with holding logic at first level gates. **b** Timing diagram for delay testing with FLH

second vector can provide enough timing margin for the propagation of the vector launching signal for small circuits. However, for large circuits, since the vector launching signal drives all the masking logic, it has large load capacitance that can result in considerable propagation delay. Early application of the launching signal is not also acceptable as discussed above. However, the vector launching signal can be applied earlier than the clock edge if it is locally AND-ed with the clock signal to generate the local vector launching signal for individual inputs.

A simple scheme for local generation of the vector launching signal and the corresponding timing is shown in Fig. 9. As shown in the timing diagram (Fig. 9b), the global TC signal arrives half a cycle earlier then the positive clock edge; however, since it is AND-ed with the local clock, the vector launching signal (local TC) is not activated until the local clock edge arrives (the local clock switches to high). A similar solution is applicable to the enhanced scan scheme as well. Such a synchronization scheme requires additional hardware (local NAND gating logic); however, these extra circuits are not in the signal data paths, and therefore, do not add to delay and power in the normal mode. Moreover, they are all minimum-sized gates to reduce overhead in area, leakage power, and clock switching capacitance. In our simulations, the extra transistors for synchronization increased the area overhead by 1.8% on an average for the FLH method. Note that in HSSG, core clock is shared between system and scan flip-flops and the scan clock network uses a hierarchy of clock buffers driving the scan states. Hence, unlike FLH, it requires an additional clock network below the global clock grid (with associated area and power overhead) for the scan elements [14].

3.2 Fault Models, Test Generation, and Scan Insertion

The proposed delay testing technique using supply gating does not affect delay fault models. The gating transistors are turned ON during normal mode of operation, hence, the conventional stuck-at fault model, transition and path delay fault models remain valid. Moreover, FLH does not require any change in pattern generation by Automatic Test Pattern Generation tools. Thus, fault coverage is virtually unaffected. Any additional DFT logic is likely to increase the fault set. Since the number of extra transistors in FLH is comparable or less than enhanced scan and HSSG methods, FLH logic does not induce additional penalty on total fault set.

During the scan insertion step, state elements selected to be scanned are replaced by a scanned state element. Test synthesis tools can be easily modified to insert scan elements with additional logic for FLH (Fig. 6). For each scanned state element, the gating logic of FLH needs to be inserted to each of its first level fanout gates. It can be noted that additional logic for FLH (gating transistors and the embedded latch) does not require to modify a logic gate. Hence, it is not necessary to change the standard cell library in case

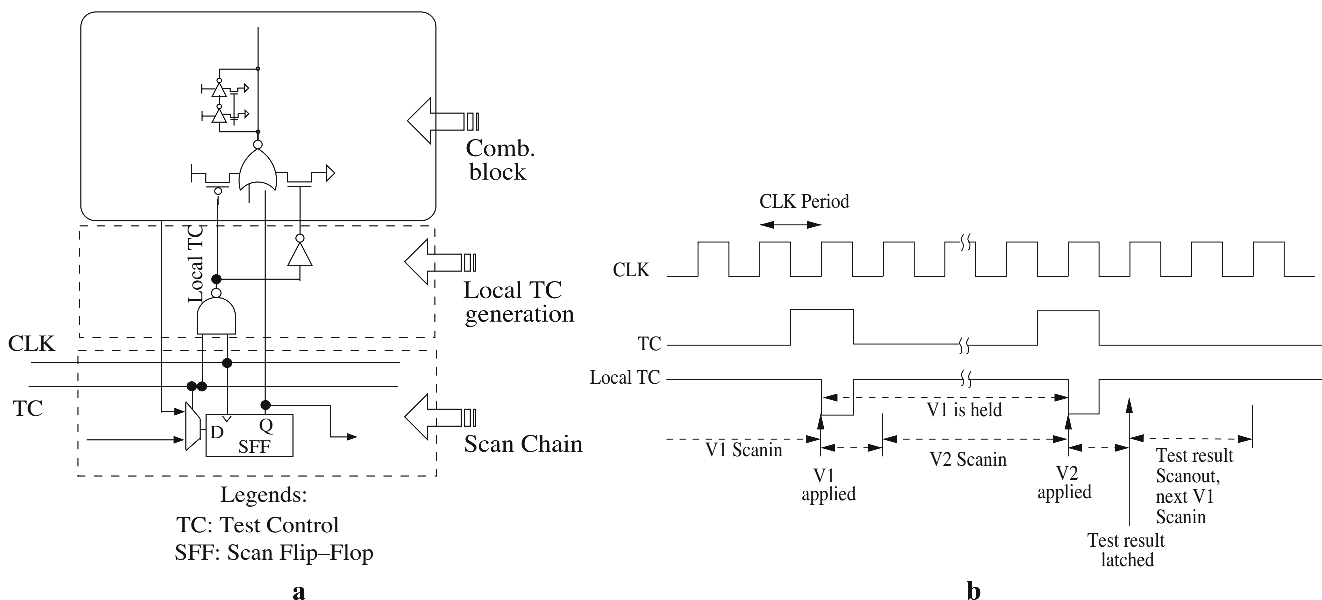

Fig. 9 Local generation of vector launching signals (TC and TCB) for synchronization with clock: **a** Schematic. **b** Timing diagram

Table 1 Comparison of percentage area increase for 70 nm technology

ISCAS89 Ckt	# Flip-flops	Total fanouts	Unique fanouts (Ratio*)	% of area increase over original design with			% Improvement over HSSG	% Improvement over enhanced scan
				Enhanced scan method	HSSG method	FLH method		
S298	14	46	35 (2.5)	15.10	37.13	14.00	62.30	7.28
S344	15	36	32 (2.1)	14.83	36.46	11.73	67.83	20.88
S641	19	19	19 (1.0)	14.24	35.01	5.28	84.92	62.91
S838	32	128	96 (3.0)	14.35	35.29	15.97	54.75	−11.27
S1196	18	24	23 (1.3)	8.17	20.09	3.87	80.73	52.61
S1423	74	185	160 (2.2)	15.07	37.05	12.08	67.39	19.81
S5378	179	410	280 (1.6)	15.67	38.54	9.09	76.41	41.98
S9234	211	635	445 (2.1)	14.98	36.83	11.71	68.19	21.78
s13207	638	1166	729 (1.14)	26.75	65.78	11.34	82.77	57.62
s15850	534	1152	837 (1.57)	22.65	55.71	13.17	76.36	41.87
S35932	1728	4272	2692 (1.6)	16.80	41.32	9.71	76.50	42.22

*Ratio = Ratio of the unique fanouts to number of flip-flops

of a cell-based design. However, integrating the gating logic into the layout of a standard-cell element allows more efficient routing and hence, can reduce the area overhead in physical implementation.

4 Results and Comparisons

To estimate the effectiveness of the FLH scheme, we simulated a set of ISCAS89 benchmark circuits and obtained area, power, and performance overhead in case of FLH, enhanced scan, and HSSG approaches. The simulations were performed using the 70 nm BPTM models [21] to observe the effect of supply gating in a sub-100 nm scaled technology. The gate-level netlists were first technology-mapped to *LEDA* 0.25 μm standard cell library using Synopsys design compiler by setting the mapping effort to medium. The library contains complex gate types e.g. “aoi” (and-or-invert) and “mux”, and hence, the total number of logic gates is reduced from that in original benchmark. The benchmark circuits are then translated to *Hspice* netlists and scaled to 70 nm. We assumed full-scan implementation of the benchmarks. Power is measured in *NanoSim* by applying 100 random vectors to the inputs and delay is measured by *Hspice* simulation of the critical path of a circuit. Tables 1 to 3 show comparisons of the proposed gating techniques with the existing techniques.

The scan flip-flops in the case of enhanced scan scheme and the FLH scheme are custom scan flip-flops (Fig. 10b) with the multiplexer embedded inside. Such custom implementation reduces area, delay, and power of the scan flip-flop. In case of FLH, size of the gating transistor is chosen to be five times of minimum transistor size. For this size of the gating transistor, we have observed that there is not considerable reduction in delay by increasing the gating transistor size.

Table 2 Comparison of delay overhead for 70 nm technology, supply 1V, temperature 25°C

ISCAS89 Ckt	Crit-path logic levels	% of delay increase over original design with			% Improvement over HSSG	% Improvement over enhanced scan
		Enhanced-scan	HSSG method	FLH method		
s298	8	11.14	3.61	3.73	−3.24	66.54
s344	11	8.26	3.06	3.91	−27.64	52.67
s641	22	5.16	1.68	2.53	−50.84	50.92
s838	20	4.07	1.63	1.49	8.66	63.52
s1196	16	6.42	2.14	1.84	13.88	71.26
s1423	46	2.72	0.86	1.20	−39.54	55.83
s5378	13	6.99	2.65	2.43	8.23	65.21
s9234	16	4.27	1.91	1.35	29.20	68.39
s13207	21	4.55	1.53	0.99	35.03	78.18
s15850	28	3.66	1.28	0.86	32.80	76.47
s35932	14	11.54	3.74	3.29	12.08	71.49

Table 3 Comparison of power overhead during normal mode for 70 nm technology, supply 1V, temperature 25°C

ISCAS89 Ckt	% of power increase over original design with			% Improvement over HSSG	% Improvement over enhanced scan
	Enhanced-scan	HSSG method	FLH method		
s298	36.51	10.89	8.43	22.63	76.92
s344	34.92	11.21	4.87	56.52	86.05
s641	45.09	14.17	4.36	69.26	90.34
s838	47.04	12.54	13.74	−9.56	70.80
s1196	21.36	6.56	0.86	86.87	95.96
s1423	36.25	10.91	1.21	88.95	96.68
s5378	35.80	12.10	2.34	80.63	93.45
s9234	41.92	11.91	4.67	60.83	88.87
s13207	42.48	13.10	−1.85	114.10	104.35
s15850	40.68	12.62	4.18	66.89	89.73
s35932	37.26	12.71	2.07	83.69	94.44

Table 1 shows comparison in terms of area overhead. Since the layout rules for the 70 nm node are not available, the measure used for area is the total transistor active area ($W * L$ for a transistor). HSSG circuit has the largest area overhead followed by the enhanced scan technique. Note that although the scan gadget in the HSSG method is implemented by all minimum-sized transistors, the total overhead in terms of the active area contributed by the scan gadget and the complex functional flip-flop in HSSG is considerably higher than the other methods. The proposed technique exhibits the smallest area overhead for most benchmark circuits. In both enhanced scan and HSSG method, one holding element (e.g. hold latch) is inserted for each state input of the circuit. However, in FLH, gating logic is inserted in all first level logic gates (Fig. 8), the number of which depends on the number of unique fanout gates of the scan flip-flops. Therefore, for a circuit with large fanout for state inputs, such as s838, the area overhead in the FLH technique can be more than the enhanced scan method. However, number of fanouts in a circuit are usually not high (2.3 on average per scan flip-flop as can be obtained from column 2 and 3) to satisfy delay constraint of a circuit (since higher fanout means higher load at the output of a gate and hence, higher delay). Number of unique fanouts, i.e. the first level gates (as shown in column 4) is further less (1.8 on average per scan flip-flop) due to overlapping fanout cones. FLH shows 34% and 73% reduction in area overhead on an average compared to the enhanced scan and HSSG techniques, respectively. It is worth noting that FLH does not introduce additional TC signals (e.g. HOLD signal in enhanced scan) or additional clock (e.g. scan clock in HSSG method). The TC signal needs to be routed to the scan flip-flops in a standard scan-based design while in the proposed technique, the sleep transistor control signal needs to be routed additionally to the first level logic gates. As shown in Table 1 (column

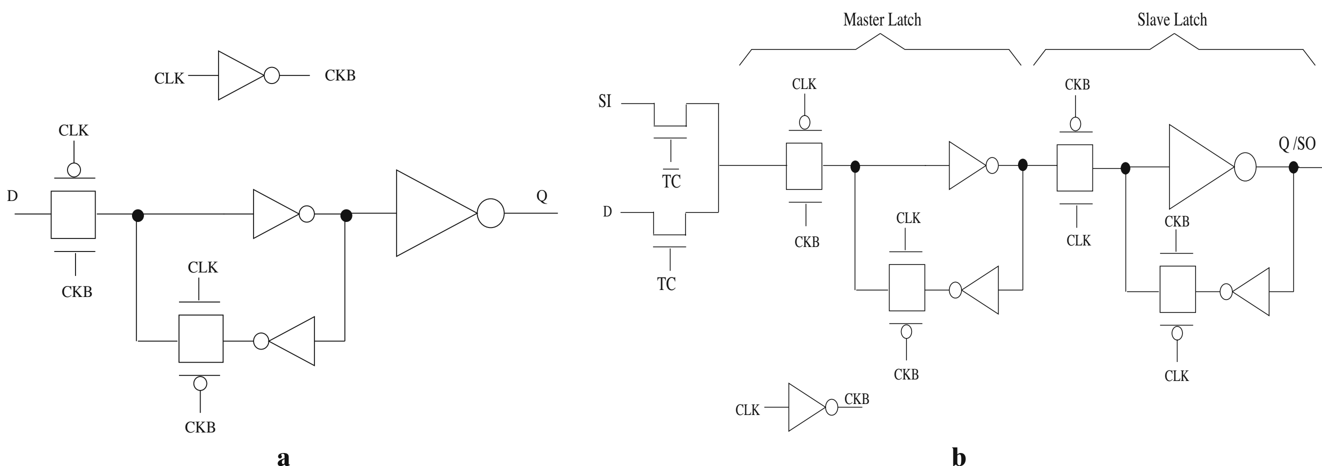

Fig. 10 Customized cells used in our simulation: **a** Latch circuit. **b** Customized scan flip-flop

4), the number of first level gates is comparable to the number of scan flip-flops. Therefore, FLH is expected to have minimal additional area requirement over the other methods due to routing of the TC signal. A fanout reduction method (for the first level of logic) under delay constraint as presented in [1] can further improve area overhead (about 20% on an average) for FLH.

Table 2 shows comparison in terms of impact on circuit delay for different benchmark circuits. As observed from Table 2, the enhanced-scan method shows the largest delay increase. FLH and HSSG method have comparable impact on circuit delay on an average. FLH exhibits reduction of up to 8% in overall circuit delay compared to enhanced scan approach. It is worth noting that the logic depth for the test circuits is fairly high (column 2). Since the original delay of the critical path is very large, the percentage improvement in circuit delay in FLH compared to the others is not large. However, comparing the percentage reduction in delay overhead in FLH with that in enhanced scan method, an average improvement of 65% is observed. As the logic depth decreases for better performance in sequential circuit, the proposed FLH scheme will show much less delay overhead as compared to enhanced scan.

Table 3 shows comparison of total power (sequential and combinational) in the normal mode of operation. Significant power savings are observed for all the benchmark circuits. In fact, for most benchmark circuits the power dissipations of the FLH circuits are close to the power dissipations of the original circuits. This is because in the proposed technique, the supply gating transistors do not switch in the normal mode. The only source of power overhead is due to very few switching of the minimum-sized supply-gated inverters (Fig. 6) and the diffusion capacitance added to the outputs of the first level gates due to the second inverter. Moreover, switching at the outputs of first level gates is less than switching at scan flip-flop outputs. For a circuit with complex gates, it is expected that the probability of switching at the internal nodes reduces with logic level. To verify this, we ran simulation on 4 benchmarks with random inputs and observed the switching both at the outputs of scan flip-flops and at the outputs of first level gates. Average number of switching at first level output nodes were observed to be 20–40% fewer than that at scan outputs. It is interesting to notice that for a large benchmark circuit such as s13207, the power of the FLH circuit is even less than the power of the original circuit. This can be attributed to the fact that the sleep transistor results in active leakage reduction (due to stacking [18]) for the idle gates. For a large circuit, at each time instant, there are many idle first level gates during scan shifting. Saving leakage in those gates, hence, reduces overall power. For all the circuits, the enhanced scan imposes the largest power overhead followed by the HSSG method. FLH shows an average reduction of 34% and 8% overall circuit power compared to the enhanced scan method and HSSG method, respectively. However, the percentage reduction in power overhead compared to the enhanced scan and HSSG is 90% and 66% on an average, respectively.

Note that the additional DFT logic in FLH that causes power overhead during normal operation (the inverters in the embedded latch) are already in low-leakage mode. The extra gating transistors added to the NMOS transistors of inverters (Fig. 6) and controlled by $\bar{TC}$ are off during normal mode, imposing stacking effect [18]. On the other hand, leakage control mechanisms for the enhanced-scan or scan-gadget based hold-scan approach impose additional requirement in terms of process (e.g. dual-Vth technique) or design (stacking).

Although we assume minimum-sized implementation of the HSSG, in certain parts of the circuit requiring at-speed scan in/out and store (e.g. 15% of scan states in Pentium 4 processor), the scan gadget in HSSG should be designed to meet full-speed scan timing requirement [14]. The fast scan gadgets in HSSG, therefore, cannot be sized down and cannot use low-leakage devices. The area and power overhead associated with fast gadgets are higher than shown in Tables 1 and 3. On the other hand, since the system flip-flop is used for scan shifting and store in case of FLH, we can always implement the embedded latch with minimum-sized transistors.

Larger-sized sleep transistors for gates in the critical path can be used to further reduce the delay penalty. It increases the area overhead but does not affect the switching power of the gates. It can be noted that if the sleep transistors are already introduced by the designers for leakage-saving purpose, area overhead due to FLH reduces greatly. The area overhead in that case will be due to the minimum-sized embedded latches in the first level gates (assuming both VDD and GND gating are used for leakage reduction). Thus, the improvement in area overhead will be greater, since the gating transistors contribute to about 2/3 of the total area overhead in FLH.

5 Power Reduction During Test Application

As we have seen in Section 4, FLH induces some penalty in terms of power dissipation in normal mode of

circuit operation due to the extra DFT logic, although significantly less compared to enhanced scan method. However, similar to the enhanced scan method, FLH saves a major part of the energy spent during test application by eliminating switching activity in combinational block.

In a conventional scan-based testing, combinational logic suffers from redundant switching in response to changing scan values during the entire period of scan-shifting. Consequently, a large part of total test energy is dissipated in the combinational block due to wasted circuit operations. Gerstendrfer et al. [12] have shown that on an average about 78% of energy in the test mode can be saved by preventing redundant switching in combinational logic with blocking gates at the output of scan flip-flops. It is worth noting that a enhanced scan flip-flop embeds a blocking gate, and thus, isolates combinational logic from activity in the scan register during shift operation.

On the other hand, FLH does not insert any blocking logic at the scan flip-flop output and allows signal propagation in shift mode to the input of the first level logic. However, supply gating at the first level logic gates, holds the previous output state of the gate and prevents propagation of switching. FLH is, thus, equally effective in completely eliminating redundant switching in the combinational logic.

Neither enhanced scan nor FLH, on the other hand, are effective in saving power dissipated in scan chain due to rippling of scan values. There are two primary components of power dissipated in scan chain: switching power in the scan flip-flop and power in the clock line due to transitions of clock. While clock power is independent of the load capacitance at the output of a scan flip-flop, switching power of a scan element is almost linearly dependent on the output load. In the case of enhanced scan, output load of a scan flip-flop is an optimally designed hold latch. However, in the case of FLH, the load varies depending on fanout of the scan flip-flop. Hence, FLH is likely to consume more power in the scan chain during test mode. However, power dissipation for the HSSG scheme is expected to be higher than FLH due to additional load on the clock line during scan shifting. Table 4 compares the power dissipation in the scan chain for the three methods. The power values include both switching power of scan flip-flop and power in the clock line. As shown in Table 4, FLH suffers an average increase of about 6% in scan power compared to enhanced scan during scan shifting. But sequential power in FLH during test mode is better by about 15% on average compared to HSSG method. During normal operation, however, output load of scan flip-flops in enhanced scan method increases (by about 7X). This is because the input pass transistors of the latch circuit (Fig. 10a) are ON in the normal mode, resulting in more capacitive load at their inputs.

FLH technique, however, holds an advantage over enhanced scan and HSSG implementations in terms of leakage power. As shown in column 7 in Table 4, FLH can reduce leakage up to 51% (and 32% on average) over enhanced scan. Since the whole combinational block remains idle during the scan shift operation, it dissipates considerable amount of power due to leakage current. In our experiment, power dissipation due to leakage was 17.8% (24.6%) of the total test power in case of FLH (enhanced scan) on an average at a 100MHz test clock. The leakage power is expected to rise significantly with technology scaling and temperature rise as explained in [4, 18]. Leakage reduction in FLH compared to enhanced scan is due to two

Table 4 Comparison of power consumption during test mode for 70 nm technology, supply 1V, temperature 25°C

ISCAS89 Ckt.	# Flip-flops	Switching power in scan chain				% improvement over enhanced scan	
		Enhanced scan method (μw)	HSSG method (μw)	FLH method (μw)	% improv. over HSSG	In leakage	In total test power
S298	14	13.96	17.50	16.53	5.55	34.26	−3.78
S344	15	14.96	18.75	16.17	13.74	28.01	2.37
S641	19	18.94	23.75	18.72	21.17	26.54	8.12
S838	32	31.90	40.00	36.49	8.77	31.42	0.72
S1196	18	17.95	22.50	18.37	18.35	9.77	4.09
S1423	74	73.78	92.50	77.95	15.73	31.81	4.53
S5378	179	178.46	223.75	188.31	15.84	50.58	6.52
S9234	211	210.37	263.75	231.94	12.06	32.80	2.05
s13207	638	636.09	797.50	660.13	17.23	32.94	3.61
s15850	534	532.40	667.50	559.78	16.14	35.67	5.01
S35932	1728	1722.82	2160.00	1746.22	19.16	43.59	9.33

reasons: a) stacking effect in the first level gates and b) about 15X less leakage in the embedded latch compared to the hold latch in enhanced scan. It is interesting to observe that although power in the scan chain is about 6% higher in FLH compared to enhanced scan, significant reduction in leakage results in about 5% average improvement in overall test power (column 8, Table 4). Average improvement in total test power compared to HSSG is 19%.

6 Conclusion

This paper presents FLH, a delay fault testing technique based on supply gating at the first level logic. It allows enhanced-scan-like test application but has considerably less DFT overhead than both enhanced scan using hold latch and a recent hold-scan method. The proposed technique is suitable for muxed scan approach. It does not affect test generation, test application, and fault coverage. FLH does not require any extra TC or clock signal. It maintains the power-saving advantage of the enhanced scan method in test mode by suppressing activity in the combinational logic during scan shifting.

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