Adiabatic carry look-ahead adder with efficient power clock generator

H.Mahmoodi-Meimand , A.Afzali-Kusha and M.Nourani

Abstract: Performance and characteristics of an adiabatic logic family are studied and compared with those of combinational and pipelined static CMOS counterparts. An 8-bit adiabatic carry look-ahead adder and its combinational and pipelined static CMOS counterparts are designed using a 0.6-μm CMOS technology. The performance of each circuit is studied in terms of the maximum frequency of operation, the minimum voltage of operation, the circuit energy consumption, and the switching noise generated by the circuit. Based on the simulation results, depending on the operating frequency, the adiabatic adder exhibits energy savings up to 87% compared with its combinational and pipelined static CMOS counterparts. It also exhibits a considerable reduction in switching noise, compared with its static CMOS counterparts. Practical issues in the design of power clock generators needed by adiabatic logic circuits are also explained. Synchronous and asynchronous power clock generators are designed and the more energy efficient circuit for the power clock generation is determined. The power clock generator exhibits a conversion efficiency of 77% at 10MHz operating frequency.

1 Introduction

The demands for low power and low noise digital circuits have motivated VLSI designers to explore new approaches to the design of VLSI circuits. Energy-recovering (adiabatic) logic is a new promising approach, which has originally been developed for low power digital circuits [1–4]. Adiabatic circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their load capacitors by using an AC-type supply voltage [5]. Another major advantage of adiabatic logic families is their best behaviour for lower generation of switching noise. Invoking adiabatic logic circuits will reduce the switching noise of digital circuits. The reason is that, in these circuits, switchings occur with the minimum voltage drop across devices and nodes voltages change slowly [5].

The supply voltage in adiabatic circuits in addition to providing the power to the circuit behaves as the clock of the circuit and for this reason is called power clock. In these circuits the supply voltage is desired to be a ramping voltage, although it can be approximated by a sinusoidal voltage that can easily be generated using resonant circuits. Although some possible power clock generators have been proposed [6–8], most attention in the earlier works has been given to logic operation and performance [1–4] while power clock generators consume a considerable fraction of the total energy consumption in adiabatic circuits. Here, we present a quantitative efficiency comparisons of different configurations of power clock generators for adiabatic circuits.

In this paper, we present the results of comparison between an adiabatic logic circuit with its combinational and pipelined static CMOS counterparts in terms of the maximum frequency of operation, the minimum voltage of operation, the energy consumption, and switching noise generation of the circuit. The logic circuit is an 8-bit carry look-ahead adder (CLA) which has been implemented using all three styles. We also design and compare some synchronous and asynchronous power clock generators for the adiabatic adder and, after assessing the more efficient power clock generator, we include it in the adiabatic adder for our comparative study. The adiabatic logic is based on pass-transistor adiabatic logic (PAL) proposed in [1] and has a fully adiabatic operation.

2 PAL overview

2.1 PAL gates

PAL is a dual-rail adiabatic logic with a relatively low gate complexity that operates with a two-phase power clock [1]. A PAL gate consists of true and complementary pass-transistor NMOS functional blocks (f, /f), and a cross-

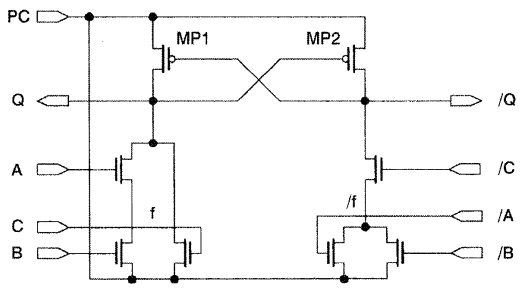

Fig.1 *Implementation of $Q = A \cdot B + C$ in PAL*

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coupled PMOS latch (MP1, MP2), as illustrated by the example of Fig. 1, which shows the implementation of an AND-OR gate: Q = A·B + C. The power is supplied through a sinusoidal power clock (PC). When PC starts rising from low, input states make a conduction path from the power clock (PC) through one of the functional blocks to the corresponding output node and allow it to follow the power clock. The other node will be tristate and kept close to 0V by its load capacitance. This, in turn, causes one of the PMOS transistors to conduct and charge the node that should go to one state, up to the peak of PC. The output state is valid at around the top of the power clock. The power clock will then ramp down toward zero, recovering the energy stored on the output node capacitance.

2.2 PAL cascades

Cascade of logic gates is provided by alternate connection of their power clock ports to PC and its 180° phase shifted signal (/PC). A cascade of four PAL inverters is shown in Fig. 2. All odd logic stages are supplied by the sinusoidal voltage PC, while all the even logic stages are supplied by /PC. The logic operation has only two phases: evaluate (E), when the power clock is ramping up, and discharge (D), when the power clock is ramping down. The E phase of an odd stage coincides with the D phase of an even stage and vice versa. Fig. 3 shows the timing of the signals in a PAL cascade obtained from the HSPICE simulations of this cascade at 10MHz with a 0.6-μm CMOS technology. The input signal was periodic sequence 01110111....

3 Adder designs

To evaluate the performance of the adiabatic logic in terms of frequency and voltage of operation, energy consumption, and switching noise generation, we designed a carry look-ahead adder (CLA) usingPAL, combinational, and pipelined static CMOS logic styles. The schematic diagram of the 8-bit CLA used for our designs is shown in Fig. 4.

All device sizes in the 8-bit PAL CLA are minimum size with W/L ratio equal to 1.5μm/0.6μm in a 0.6-μm CMOS technology. Each primary output was connected to a 50fF load. The first nonadiabatic design was a purely combinational CLA, while the second one was a pipelined version of the fully combinational design. The layouts of the two designs were generated using standard cells and the LEDIT placement and routing tool. The standard cells were optimsed for low power and high speed. We have integrated these three layouts in a test chip whose layout is shown in Fig. 5.

4 Power clock generation

In adiabatic circuits, power and clock lines are mixed into a single power clock line, which has both the functions of powering and timing the circuit. A DC to AC converter named power clock generator is needed for the generation

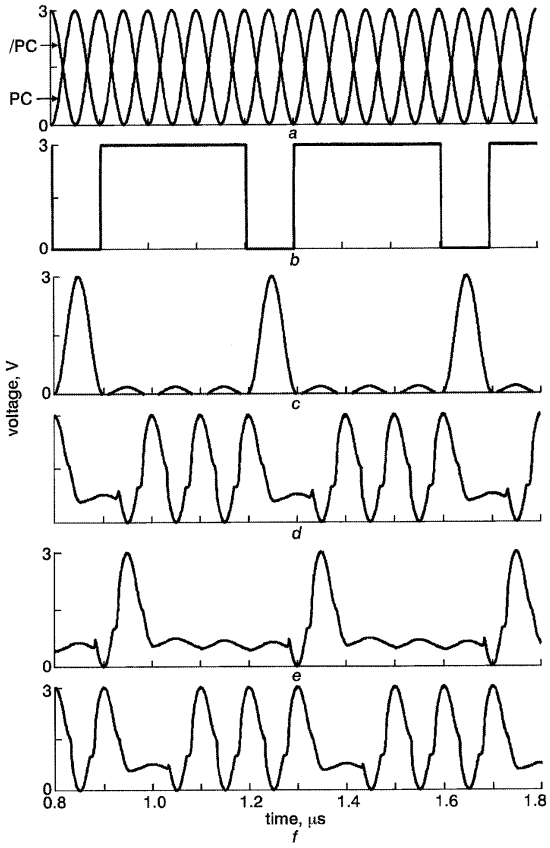

Fig. 3 *Waveforms obtained from HSPICE simulations of a 4-stage pipeline of PAL inverters*
a Power clock (PC and /PC)
b Input of 1st stage
c Output of 1st stage
d Output of 2nd stage
e Output of 3rd stage
f Output of 4th stage

of the power clock signal. To evaluate the performance of a powerclock generator, the conversion efficiency is defined as the ratio of the dissipated energy in the adiabatic core and the total delivered energy from the DC supply. The LC resonant circuit is suitable for a power clock generator [6]. L is an external inductor and *C* is the distributed capacitance of the power clock line and its connected logic circuits all over the chip. To have a stable frequency of oscillation, the equivalent on chip capacitance should be constant and data independent, which is achieved in the adiabatic logic circuit due to its differential nature. The first step in designing the power clock generator for an adiabatic circuit is circuit modelling to determine the equivalent capacitance. This concept is described in the following Section and illustrated by the example of our adiabatic CLA.

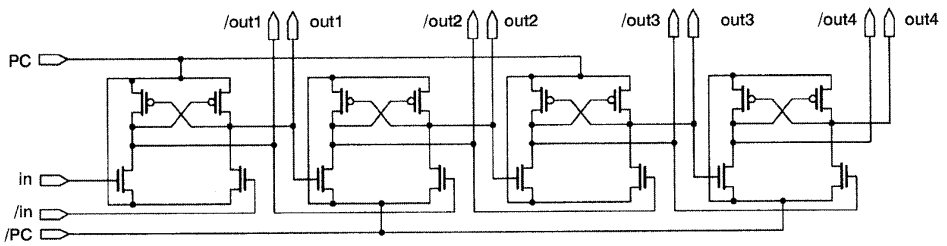

Fig. 2 *4-stage cascade of PAL inverters*

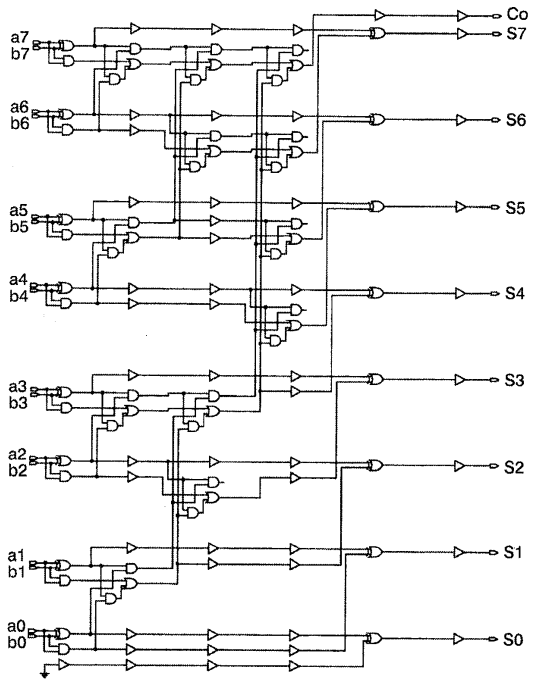

Fig. 4 *Schematic diagram of the 8-bit CLA*

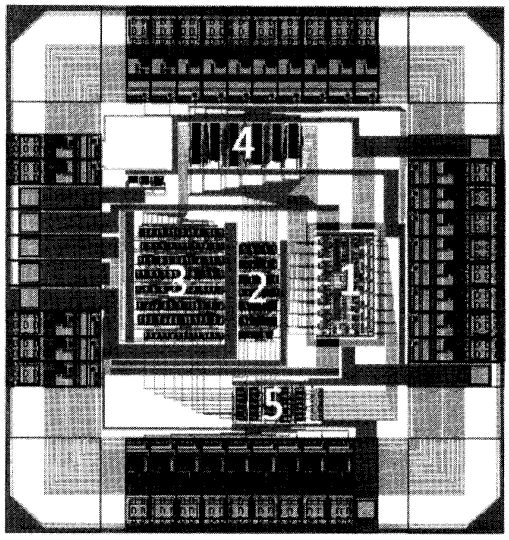

Fig. 5 *Layout of test chip*
1 – adiabatic CLA
2 – combinational CLA
3 – pipelined CLA
4 – input demultiplexer
5 – output multiplexer

4.1 Adiabatic logic model

For each phase, an approximate lumped-element rnodel of the logic includes an equivalent capacitor C to model energy storage, in series with a resistor R to model the losses. The values of the model parameters R and C can be extracted from the simulation tests where an external ideal sinusoidal voltage source is applied as the power clock. For a given clock frequency f_c and a logic activity, the power loss P_L in the logic, and the RMS current I_L supplied to the logic by the power clock can be found from the test. Given P_L and I_L, the model parameters can be found as [8]:

$$R = \frac{P_L}{I_L^2} \tag{1}$$

$$C = \frac{\sqrt{2} I_L}{\pi V_{DD} f_C} \tag{2}$$

where V_{DD} is the peak value of the applied power clock. We have performed this test for our adiabatic CLA and extracted the equivalent R and C for each power clock phase in the frequency range of 10 MHz to 100 MHz The results have been summarised in Table 1, where the tests were performed for the maximum logic activity of the circuit. As expected, the equivalent capacitance is relatively independent of the clock frequency (~5 pF).

Table 1: Results of modelling adiabatic CLA for V_{DD} = 3.3 V

	Phase 1				Phase 2			
f_c (MHz)	P_{L1} (μW)	I_{L1} (μA)	R_1 (Ω)	C_1 (pF)	P_{L2} (μW)	I_{L2} (μA)	R_2 (Ω)	C_2 (pF)
10	20.9	355.3	166	4.85	34.23	385	231	5.25
20	57.4	704	116	4.8	91.67	761	158	5.19
30	104.9	1050	95	4.77	164.7	1126	130	5.12
40	163	1377	86	4.7	250.9	1489	113	5.08
50	229.8	1715	78	4.68	348.8	1834	104	5
60	364.2	2092	83	4.75	453.6	2222	92	5
70	390.5	2413	67	4.7	537.9	2561	82	5
80	478.6	2758	62.9	4.7	645.8	2911	76	4.96
90	585.3	3123	60	4.7	763.5	3280	70	4.97
100	701.4	3415	60	4.66	821	3598	63	4.91

4.2 Integrated resonant power clock generators

Various circuit topologies for resonant energy recovery have been proposed for different adiabatic logic styles and for different applications [6–8]. They can be classified into two main groups: asynchronous and synchronous power clock generators. Asynchronous power clock generators are free running circuits that use feedback loops to self-oscillate without any external timing signals. Fig. 6 illustrates two commonly used asynchronous power clock generators: 2N and 2N2P power clock generators [6]. Many problems are associated with asynchronous structures. Their oscillation frequencies are sensitive to their capacitive load variations in different cycles of the system operation resulting in unstable frequency problems. In addition, in large systems, inputs and outputs of each module must be in synchronisation with other modules prohibiting the integration of the adiabatic module driven by asynchronous power clock generators into a larger nonadiabatic system. In these cases, the synchronous power clock generators can be utilised as an efficient solution without having any of the above problems. Synchronous power clock generators are synchronised to external timebase signals usually available in large systems. [7] illustrates two synchronous power clock generators similar to the asynchronous counterparts except that the gate control signals are derived externally. The capacitors *CE*1 and *CE*2 in Figs. 6 and 7, are external balancing capacitors to achieve more conversion efficiency. We will show that the synchronous power clock generators are more energy efficient than the asynchronous ones.

4.3 Power clock design

We design all four power clock generators for the adiabatic CLA, at 10 MHz operating frequency and 3.3 V supply voltage, and compare the power dissipation and conversion efficiency. Using the results in Table 1, we design each of the power clock generators by placing simple resistors and capacitors equal to the extracted values instead of the

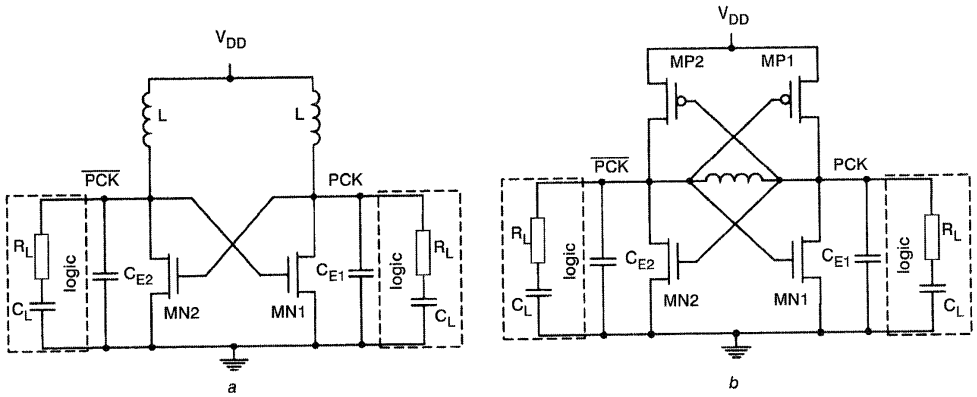

Fig. 6 *Asynchronous two phase power clock generators*
a 2N
b 2N2P

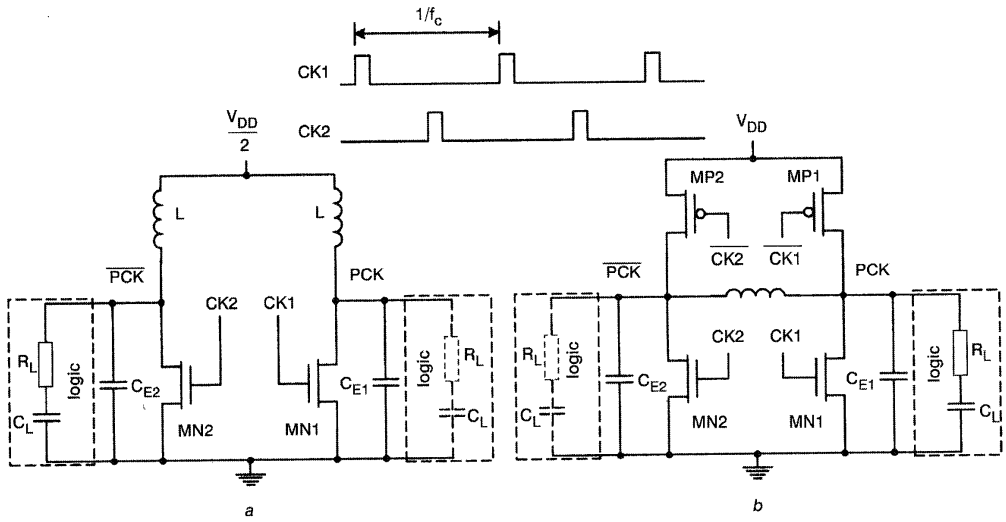

Fig. 7 *Synchronous two phase power clock generators*
a 2N
b 2N2P

adiabatic adder. Then this simple circuit can be quickly designed and simulated to find the optimum design. The value of L is determined by the required frequency and the extracted capacitance. The oscillating frequency for the 2N power clock generators is determined by [9]:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{3}$$

and for the 2N2P power clock generators is determined by:

$$f = \frac{1}{2\pi\sqrt{L\left(\frac{C}{2}\right)}} \tag{4}$$

where C is the equivalent capacitance of each phase. After simulating and optimising the power clock generator with the simple RC model, the designed power clock generator is connected to the adiabatic CLA and simulated again. In this stage, slight modifications may be needed to optimise the design for the highest achievable conversion efficiency. The results, summarised in Table 2, indicate that with synchronous power clock generators, higher conversion efficiencies can be achieved. Between the two synchronous schemes, the 2N power clock generator is simpler, more energy efficient, and resulting in the higher conversion efficiency of 77%. We use this power clock generator to extract the simulation results, presented in the next Section.

Table 2: Power dissipation summary of adiabatic CLA with different power dock generators at 10MHz operating frequency and 3.3V supply voltage

Power clock generator	Asynchronous		Synchronous	
	2N	2N2P	2N	2N2P
Power dissipation of ACLA core	62μW	61μW	58μW	57μW
Power dissipation of DC-AC converter	66μW	77μW	17μW	26μW
Total delivered power	128μW	138μW	75μW	83μW
Conversion efficiency	48%	44%	77%	69%

5 Simulation results

In this Section, we present the results of HSPICE simulations for the adders. The circuits were simulated with the netlists extracted from the layouts. We also applied the worse case input pattern to the adders that would cause the maximum rate of events on the circuit nodes leading to the maximum switching noise and power consumption.

5.1 Energy consumption results

Fig. 8 shows the energy consumption per cycle of tile adders when operating at 10MHz, 50MHz, 100MHz, 150MHz, and 200MHz. The minimum supply voltage for each design is shown next to its data point. As expected,

the pipelined design has the lowest minimum operating voltage and the adiabatic design has the highest one. The adiabatic design, however, has the least energy consumption among the designs. Compared with the combinational adder, the adiabatic adder exhibits energy savings of 82% at 10 MHz and 68% at 100 MHz while in comparison with the pipelined adder, the adiabatic adder exhibits energy savings of 81% at 10 MHz and 87% at 100 MHz. The adiabatic design fails to function above 100 MHz, due to the short duration of the PAL evaluation phase.

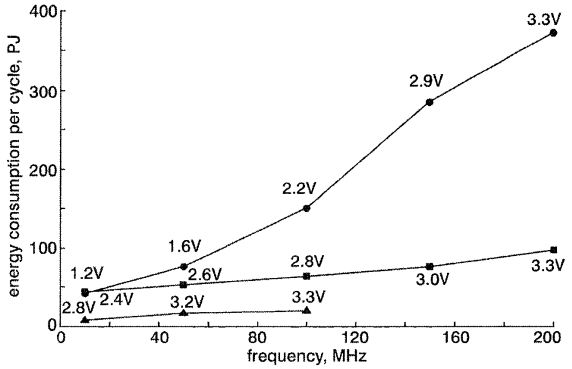

Fig. 8 *Energy consumption against frequency*
—●— pipelined CLA
—■— combinational CLA
—▲— adiabatic CLA

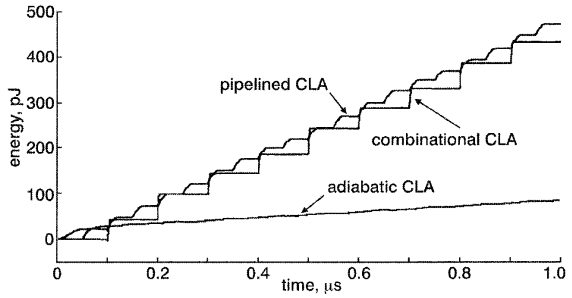

Fig. 9 *Energy profiles of CLAs*

Fig. 9 gives the overall energy profiles of the adders at 10 MHz, while operating at their minimum supply voltage. In the case of the adiabatic adder, energy is recovered from one phase and delivered to the other phase at the same time and the supply only compensates the small losses during this energy transfer. Energy consumption of the combinational adder occurs at the times of the input transitions and energy consumption of the pipelined adder occurs at the active edges of the clocks. The energy consumption characteristic of the CLAs as a function of the supply voltage at constant 10 MHz frequency is shown in Fig. 10. As can be observed from the figure, the energy consumption per cycle of the static CMOS designs is quadratically dependent on the voltage level while the energy consumption per cycle of the adiabatic design is less sensitive to supply voltage variations and does not follow the CV^2 rule.

5.2 Switching noise generation results

Power supply switching noise is composed of resistive (IR) and inductive (LdI/dt) noise Fig. 10. Here I is the supply current while L and R are the effective supply inductance and resistance, respectively. When a number of devices switch at the same time, the cumulative transient current (I) and the slew rate (dI/dt) can be very large, resulting in considerable switching noise even though L and R can be relatively small. In the adiabatic circuits, switchings occur with the minimum voltage drop across devices and both the signals and the power clock change slowly. Thus steep spikes can be effectively removed from the supply current resulting in a considerable reduction in the switching noise.

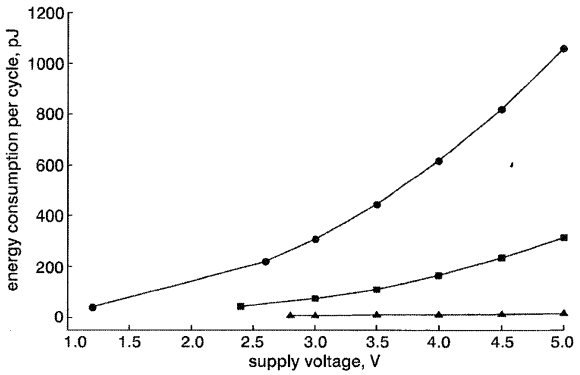

Fig. 10 *Energy consumption against supply voltage for the 8-bit CLAs at constant 10 MHz frequency*
—●— pipelined CLA
—■— combinational CLA
—▲— adiabatic CLA

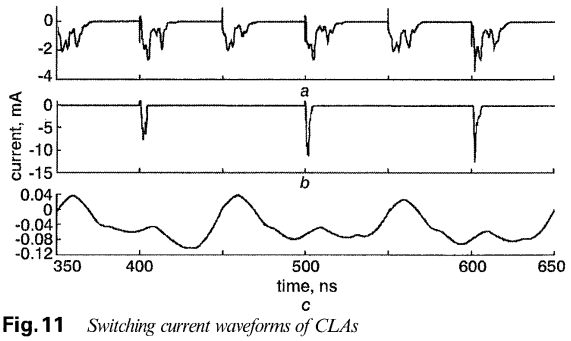

Fig. 11 *Switching current waveforms of CLAs*

The worse case input patterns which would induce the steepest switching current spikes and, therefore, the maximum switching noise, were applied to the CLAs in the HSPICE simulation to extract the switching current waveforms. Fig. 11 shows the switching current waveforms obtained for the CLAs when operating at their minimum supply voltage at 10 MHz The pipelined adder has abrupt total switching currents at the active edges of the clocks with the maximum amplitude of 3.4 mA with many peaks and valleys. The combinational adder has abrupt switching currents at the input transitions with the maximum amplitude of 12.6 mA. The switching current of the adiabatic adder is much more regular with the maximum amplitude of 103 μA which shows 97% and 99% reduction compared to the pipelined and combinational adder, respectively. The maximum current slopes for the pipelined, combinational, and adiabatic designs are 47 A/μs, 47 A/μs, and 1 mA/μs, respectively. This means that the adiabatic design exhibits more than four orders of magnitude reduction in the maximum current slope, compared with the static CMOS designs, which can be translated to the same level of reduction in the inductive part of the switching noise, provided the same power supply effective inductance exists for all three designs.

6 Summary and conclusions

In this paper, an adiabatic logic style has been compared with the combinational and pipelined static CMOS logic

styles. The comparisons were performed by designing an 8-bit carry look-ahead adder using all three methods with a 0.6-μm CMOS technology. Different asynchronous and synchronous power clock generators were also designed for the adiabatic adder, and the results concluded that the synchronous 2N power clock generator was the more efficient power clock generator. The designed circuits were post-layout simulated by HSPICE. Based on the simulation results, the adiabatic CLA exhibited energy savings up to 87% and considerable improvement in switching noise reduction, compared with its static CMOS counterparts. At each operating frequency, the adiabatic design had the highest minimum supply voltage and its maximum operating frequency was about two times less than those of the static CMOS designs. In conclusion, while the adiabatic logic family studied here exhibited considerable improvements in terms of energy savings and the switching noise characteristic, it had the disadvantages of required higher supply voltages and lower speeds of operation.

7 Acknowledgment

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