A Leakage-Tolerant High Fan-in Dynamic Circuit Design Style

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Abstract

A leakage-tolerant design technique for high fan-in dynamic logic circuits is presented. An NMOS transistor with gate and drain terminals tied together (diode) is added in series with the evaluation network of standard domino circuits. Due to the stacking effect, the leakage of the evaluation path significantly decreases, thereby improving the robustness of the circuit against deep-submicron subthreshold leakage and input noise. To improve the speed of the circuit, a current mirror is also employed in the evaluation network to increase the evaluation current. The proposed technique (Diode-Footed Domino) exhibits considerable improvement in leakage and noise-immunity as compared to the standard domino circuits. Simulation results of wide fan-in gates designed using Berkeley predictive technology models of 70nm technology demonstrate at least 1.9X noise-immunity improvement at the same delay compared to the standard domino circuits.

1. Introduction

Domino circuits are widely used in high-speed applications for the implementation of high fan-in circuits [1]. However, domino circuits are vulnerable to noise. The noise-sensitivity of domino circuits is due to their low switching threshold voltage, which is equal to the threshold voltage of NMOS devices in the evaluation network. The substantial increase in deep-submicron noise with technology scaling severely impacts the usefulness of domino circuits [1-3]. With technology scaling, the supply voltage is scaled down to decrease the power consumption. In order to improve performance, the transistor threshold voltage has to be commensurately scaled to maintain a high drive current. However, the threshold voltage scaling results in the substantial increase of the sub-threshold leakage current [4-5]. The main source of noise in deep-submicron circuits is mainly due to high leakage current, crosstalk noise, supply noise, and charge-sharing [3]. As the technology scales down, the leakage of the evaluation transistors exponentially increases due to lower threshold voltage, while the noise at the input of the evaluation transistors may increase due to increased crosstalk [3]. Moreover, the supply voltage and capacitance of dynamic (precharge) nodes scales down, reducing the amount of charge stored on the dynamic nodes. Due to all these concurrent factors, the noise-immunity of domino gates substantially decreases with technology scaling. Since the leakage current is proportional to the fan-in of domino OR gates, the noise-immunity also decreases with fan-in increase.

Leakage and noise-tolerance are of major concern for wide domino OR gates because the evaluation transistors are all in parallel, leaking charge from the precharge node [6-7]. Figure 1 shows standard domino schemes for wide OR gates, where the first scheme (Figure 1-a) uses a footer transistor, and the second scheme (Figure 1-b) is a footless domino gate [7]. In a cascaded chain of domino gates, footless topology is preferred for very high performance designs [1]. The static inverter is skewed for fast low-to-high transition to improve performance [8].

Conventionally, the robustness of standard domino circuits can be improved by upsizing the keeper transistor [1]. The keeper ratio (K) is defined as the ratio of the current drivability of the keeper transistor to that of the evaluation transistor:

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{\text{Keeper transistor}}}{\mu_n \left(\frac{W}{L}\right)_{\text{Evaluation transistor}}} \quad (1)$$

where μ_n and μ_p are the mobilities of electrons and holes in a given technology, respectively. The keeper ratio provides a way to tradeoff robustness and performance in standard domino gates. As the size of the keeper transistor increases, the noise-immunity increases; however, the performance degrades, and the power consumption increases. Therefore, keeper upsizing may not be a viable solution for high leakage and noise-immunity problem in scaled domino circuits [2].

A recently proposed leakage-tolerant technique -- conditional-keeper domino [9], as shown in Figure 2 -- employs two keeper transistors. Transistor K1 is a small keeper that is ON as long as the precharge node is charged. The other keeper, K2, is initially OFF at the onset of the evaluation phase. Then, if the precharge node remains high for a predetermined amount of time of the delay (T_{keeper}), the output of the NAND gate goes low and turns on the larger keeper K2, strongly keeping the precharge node at high for the rest of the evaluation period. The leakage-tolerance can be improved by

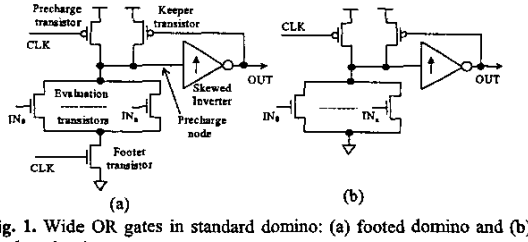

Fig. 1. Wide OR gates in standard domino: (a) footed domino and (b) footless domino.

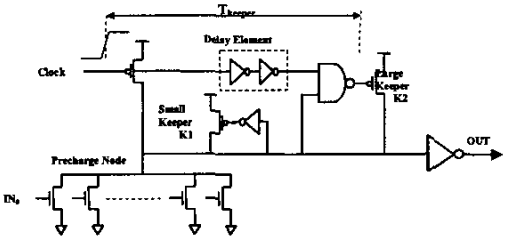

Fig. 2. Wide domino OR gate using conditional-keeper technique [9].

decreasing T_{keeper} delay. However, improving the leakage-tolerance using this technique is limited, since there is a limit on decreasing T_{keeper}. The reduction of T_{keeper} by increasing the size of the inverters in the delay element significantly increases the power consumption, since the inverters are directly connected to the clock and the clock switches every cycle. Moreover, the sensitivity of the delay of the inverters to process variations makes the circuit performance and robustness unpredictable.

We propose a new circuit technique, diode-footed domino, to make the domino circuits more robust, leakage-tolerant, and scalable without considerable performance degradation or power consumption increase. This technique uses a relatively small keeper transistor, but increases the leakage-immunity by a footer transistor in a diode configuration, and improves performance by employing a current mirror technique in the evaluation network.

2. Noise (Leakage) Immunity Metric

For robustness measurement, identical noise pulses are applied to all inputs in the evaluation phase, and the amplitude of the noise at the output of the static inverter (OUT in Figure 1) is measured as shown in Figure 3. In this measurement, the duration of the input noise pulse is kept constant at 30ps (typical gate delay at 70nm technology) and the amplitude of the output noise is observed for different amplitudes of the input noise. The metric we use for leakage and noise robustness comparison is Unity Noise Gain (UNG), defined as the amplitude of the input noise that causes the same amplitude of noise at the output [7]:

$$UNG=\{V_{noise};\ V_{noise}=V_{out}\} \qquad (2)$$

3. Diode-Footed Domino

We modify domino circuit by adding an NMOS

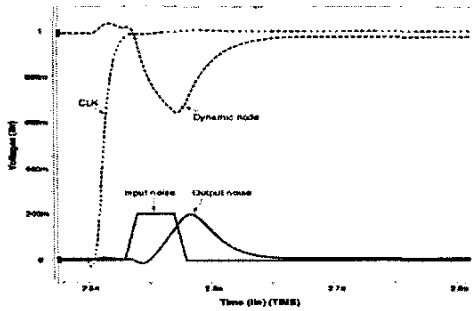

Fig. 3. Noise-immunity measurement for domino gates.

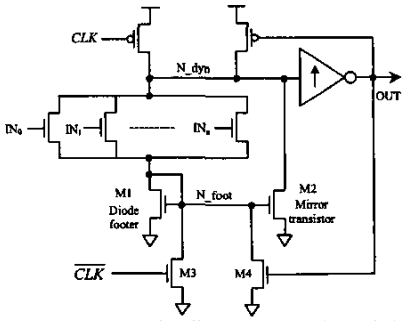

Fig. 4. Wide OR gate using diode-footed domino technique.

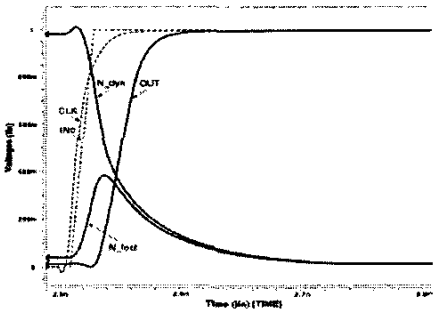

Fig. 5. Simulated waveforms of diode-footed domino.

transistor in a diode configuration (gate and drain terminals connected together) in series with the evaluation network, as illustrated in Figure 4 for an example wide OR gate. The diode-footer (transistor M1) decreases the subthreshold leakage due to a phenomenon called the stacking effect [4]. Due to the leakage of the evaluation transistors, there is some voltage-drop established across the diode-footer (transistor M1) in the evaluation phase. This voltage-drop makes the gate-to-source voltage (V_{gs}) of the OFF evaluation transistors negative, causing an exponential reduction in the subthreshold leakage. Moreover, the voltage-drop across the diode increases the body effect of the evaluation transistors, which also helps in the subthreshold leakage reduction [4]. On the other hand, the diode-footer increases the switching threshold voltage of the gate by the threshold of NMOS devices, and hence, the new gate switching threshold voltage is about $2V_{tn}$. The higher gate switching voltage results in a better noise-immunity, however, at the expense of performance degradation. The reason for performance degradation is that the diode footer decreases the evaluation current. To increase the performance, the mirror transistor (M2 in Figure 4) is used to mirror the evaluation current and drain it from the precharge node (N_dyn). Therefore, the total evaluation current is equal to the evaluation current through the evaluation network plus the mirrored evaluation current. The mirror ratio (M) is defined as the ratio of the current drivability of the mirror transistor to that of the diode footer:

$$M = \frac{\left(\frac{W}{L}\right)_{\text{Mirror transistor}}}{\left(\frac{W}{L}\right)_{\text{Diode footer}}} \qquad (3)$$

Transistor M3 is ON during the precharge phase when the clock is low, and turns off the mirror transistor (M2) to

prevent any possible short-circuit current through M2 during the precharge phase. Transistor M4 is driven by the output to pull down the footer node (N_foot) and the precharge node to zero, if the output goes high in the evaluation phase. This feedback prevents any short circuit power consumption in the static inverter in the evaluation phase. Due to the considerable reduction in the leakage of the evaluation network, a very small keeper size suffices. By increasing the mirror ratio, the performance can be increased. However, this is at the expense of lower robustness, since the mirror transistor also drains some leakage from the precharge node. Hence, the mirror ratio provides a way to tradeoff robustness and performance. Keeper upsizing in standard domino has the same effect as mirror downsizing in the diode-footed domino.

Figure 5 shows the simulated waveforms of the circuit. The waveforms are obtained by HSPICE simulations of the 8-input OR gate in the worst-case I_{off} corner of the 70nm Berkeley Predictive Technology Models (BPTM) [10] at 110°C and 1V supply voltage.

4. Simulation Results and Comparisons

The dynamic OR gates based on the standard footless domino (Figure 1-b), conditional-keeper domino (Figure 2), and the diode-footed domino (Figure 4) having fan-ins of 8, 16, and 32 are simulated using HSPICE in the worst-case I_{off} corner of the 70nm predictive technology at 1V and 110°C. In the standard footless domino gates, the keeper ratio (K, defined in Equation 1) is increased from 0.1 to 1 in order to extract different data points for delay, UNG, and power consumption. A similar experiment is performed for the diode-footed domino gates by increasing the mirror-ratio (M, defined in Equation 3) from 0.1 to 1. In the conditional-keeper gates, the small keeper (K1 in Figure 2) is selected to be a minimum-sized transistor which corresponds to a keeper ratio of 0.1 in our design. For the large keeper (K2 in Figure 2), two different keeper ratios of 0.4 and 0.9 are used. These two designs of conditional-keeper gates are specified with K2=0.4 and K2=0.9 on the figures that are presented in this section. In the conditional-keeper designs, the trade-off between performance and UNG is established by decreasing the delay of the delay element (T_{keeper} in Figure 2) by upsizing its inverters. For performance measurement, the delay from input IN_0 to OUT is measured in the evaluation phase while all other inputs remain in the zero state. Power consumption is also measured when one input goes high and discharges the precharge node in every evaluation phase.

Figure 6 shows UNG-delay curves for the wide dynamic OR gates. As expected, the diode-footed gates show significantly higher noise-immunity compared to the standard and conditional-keeper domino gates. It is also evident from Figure 6 that the effectiveness of the conventional keeper upsizing method is limited in terms of UNG improvement, especially for higher fan-ins, and results in considerable performance degradation. Moreover, for each fan-in, if the UNG is required to be larger than a certain amount, the diode-footed technique exhibits better performance. For example, it can be observed in Figure 6 that if the required normalized UNG for an 8-input domino OR gate is required to be greater than 0.18, then the diode-footed implementation shows better performance and robustness compared to the standard domino design. Similarly, if the required normalized UNG is required to be greater than 0.24, the 8-input diode-footed gate shows better performance and robustness compared to its conditional-keeper counterpart. For 16 and 32-input OR gates, the diode-footed implementations show better performance compared to the standard (conditional-keeper) domino designs, if the normalized UNGs are required to be greater than 0.12(0.16) and 0.07 (0.1), respectively. In the standard and

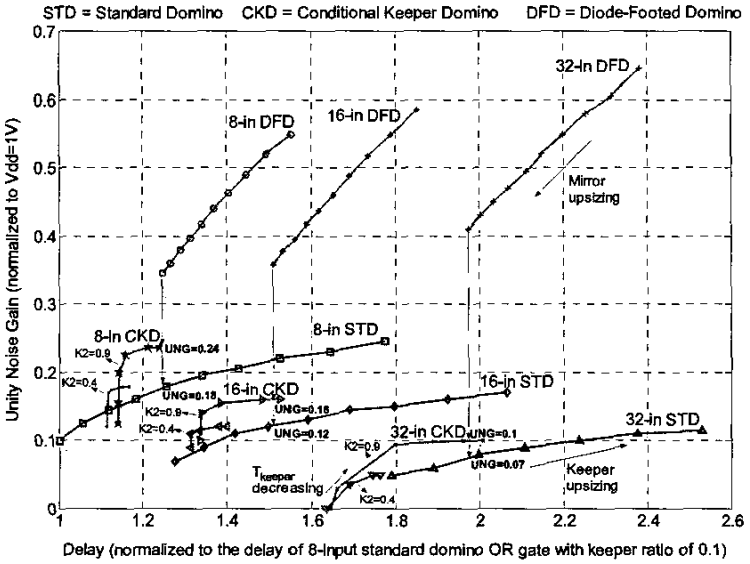

Fig. 6. UNG-delay curves for wide dynamic OR gates.

Table 1. UNG Comparison under same delay (UNG numbers are normalized to V_{dd}=1V)

Fan-in	UNG of standard domino	UNG of conditional-keeper domino	UNG of diode-footed domino	UNG improvement compared to standard domino	UNG improvement compared to conditional-keeper domino
8	0.18	0.24	0.345	1.9X	1.4X
16	0.12	0.16	0.357	2.9X	2.2X
32	0.07	0.1	0.410	5.8X	4.1X

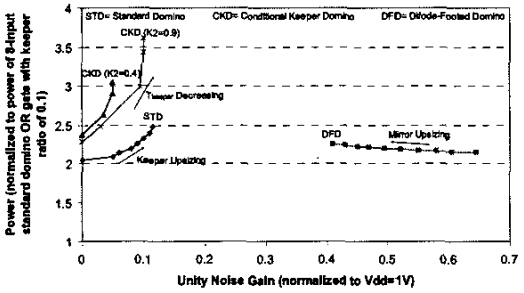

Fig. 7. Power consumption versus UNG for 32-input standard, conditional-keeper, and diode-footed domino OR gates.

conditional-keeper domino gates, the UNG considerably drops with fan-in increase; however, the UNG does not drop with fan-in increase in the case of the diode-footed domino. This is due to the fact that the voltage-drop across the diode-footed transistor (M1 in Figure 4) increases with fan-in increase, causing higher gate switching voltage. Higher gate switching voltage improves noise-immunity. We compare the noise-immunity of the different techniques under same delay (iso-delay UNG). For the diode-footed design the minimum delay point (the end point of the UNG-delay curves in Figure 6) is selected and the UNG of that point is compared with the UNG of the corresponding standard and conditional-keeper domino designs at the same delay. Numerical results for UNGs under iso-delay condition are shown in Table 1. The results exhibit the superior noise-immunity of the diode-footed domino. The noise-immunity improvement is significantly higher for higher fan-in gates. This implies that the diode-footed technique is more effective for high fan-in gates in terms of performance and UNG improvement. The higher the fan-in is or the higher the required robustness is, the more performance improvement is achieved by the diode-footed technique. The required UNG depends on technology and surrounding circuits of the domino gates.

Another deficiency of the keeper upsizing method in the standard domino is that UNG increase by keeper upsizing is at the expense of more power consumption. Keeper upsizing has two negative effects on power consumption: first, it increases the capacitive load on the dynamic and output nodes, which results in more switching power consumption; and second, it increases the contention between the keeper and the evaluation transistors at the beginning of the evaluation phase, which results in more short-circuit power consumption. UNG increase by decreasing T_{keeper} in the conditional-keeper domino is also at the expense of more power consumption. The reduction of T_{keeper} by increasing the size of the inverters in the delay element significantly increases the power consumption, since the inverters are directly connected to the clock which switches every cycle. The diode-footed domino requires a smaller keeper; therefore, the contention and short-circuit power consumption in the evaluation phase is reduced. The power-savings can mitigate the power overhead incurred by the extra transistors required in the diode-footed technique. Figure 7 shows the power consumption of the 32-input standard, conditional-keeper, and diode-footed domino OR gates as keeper ratio, T_{keeper}, and mirror ratio, respectively, are varied for achieving higher UNGs. As observed from Figure 7, the power consumption of the standard and conditional-keeper domino gates significantly increases as the keeper ratio increases and T_{keeper} decreases, respectively. However, the power consumption of the diode-footed domino gate does not change much with the mirror ratio and is comparable to the power of the standard domino gate with a small keeper size.

5. Conclusion

The basic way to tradeoff robustness and performance in conventional domino circuits is keeper-upsizing. However, such a trade-off is no longer viable for future deep-submicron technologies since large keeper transistors have a severe impact on performance and power consumption in high fan-in domino gates. We proposed the diode-footed domino circuit design style and demonstrated that the technique is leakage-tolerant, achieves high-performance and low power compared to the conventional domino styles, and is suitable for scaled CMOS technologies.

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