Impact of Transistor Aging Effects on Sense Amplifier Reliability in Nano-Scale CMOS

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Abstract
Bias temperature instability (among other problems) is a key reliability issue with nanoscale CMOS transistors. Especially in sensitive circuits such as sense amplifiers of SRAM arrays, transistor aging may significantly increase the probability of failure. By analyzing the Current Based Sense Amplifier circuit and Voltage-Latched Sense Amplifier circuit through HSPICE simulations, we observe that under the effects of Negative Bias Temperature Instability (NBTI) aging alone, the failure probability increases for both circuits. However, under Positive Bias Temperature Instability (PBTI) only or the combined effects of both NBTI and PBTI, failure probability reduces over time.

1. Introduction

As CMOS technology is scaled down to nanometer dimensions, transistors show significant degree of variations in their parameters. A prominent example of this variation is threshold voltage change over time due to bias temperature instability (BTI) of which there are two kinds, each effecting either PMOS or NMOS transistors: Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI). Such variations affect the reliability of sensitive circuits such as sense amplifiers. In this research we implement two types of sense amplifiers, a Current Based Sense Amplifier (CBSA) and Voltage-Latched Sense Amplifier (VLSA), and simulate them using the HSPICE tool. We will measure the probability of failure as a reliability metric.

A. Current Based Sense Amplifier (CBSA)

A common design used for sense amplifiers is the Current Based sense amplifier (CBSA) [6]. Ideally, the circuit is symmetrical (**Figure 1**). During a “pre-charge” phase, the nodes “out” and “outb” are precharged to Vdd by the precharging transistors “Mpp1” and “Mpp2”. After that, both “BL” and “BLB” signals are asserted (for example, BL = Vdd and BLB = Vdd - ΔV).When the sensing enable signal (SAE) is asserted, a stronger current is sourced from “Mn1” than in “Mn2” since there is a higher gate input voltage (because BL>BLB) , and so “out” will discharge faster than “outb”. The faster drop of voltage at “out” turns on the strong positive feedback of the cross-coupled inverters and turns on “Mp2” (the PMOS part of the inverter at “outb”), and so then this charges “outb” back to Vdd. While this is happening, “out” is still discharging and so both signals will swing correctly resulting in a correct operation.

Figure 1: Current Based Sense Amplifier (CBSA)

B. Voltage-Latched Sense Amplifier (VLSA)

Another common design of sense amplifiers is the Voltage-Latched Sense Amplifier (VLSA) [5]. Similar to the Current Based Sense Amplifier, this circuit is ideally symmetrical (**Figure 2**). This design operates similarly to the CBSA circuit, but unlike that design, failures would not be caused by a mismatch in current between Mn1 and Mn2 since the operation is not based on the difference in current.

C. Effects of Threshold Voltage Variation on Sense Amplifier Circuits

In both sense amplifier designs, threshold voltage variation can cause operation failures. In the CBSA design, if there is an offset in Vt between transistors “Mn1” and “Mn2” due to BTI or random threshold variations, it could be that even if the gate input voltage at “Mn1” is higher, the induced current at “Mn2” could be larger, causing a faster discharge at “outb” which would cause the circuit to “flip” in the wrong direction, (i.e. an operational failure) (**Figure 3**). This type of failure, though, is caused by a current-mismatch and so would not apply to the Voltage-Latched Sense Amplifier (VLSA) circuit since it is not based on differences of current. In the VLSA design, variation in Vt, though, can cause failures due to a trip-point mismatch with the transistors that make up the cross-coupled inverters. This type of failure can occur in both sense amplifier designs. An initial voltage difference between “out1” and “out2” due to random threshold voltage variations can cause a trip point mismatch and “flipping” of the cross-coupled inverters in the wrong direction if this mismatch is enough to offset the difference between “BL” and “BLB”.

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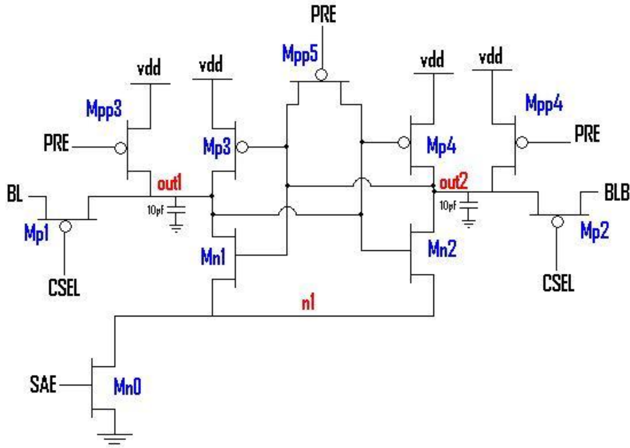

Figure 2: Voltage Latch Sense Amplifier (VLSA)

2. Modeling of Combined effect of Random Threshold Voltage Variations and Transistor Aging Effects

We have simulated each of these models of sense amplifiers, introducing some random variability (with a standard deviation of 33mV) to the threshold voltages of the transistors to model the effects of threshold voltage variations among each transistor, and find the probability of failure of each using the Monte Carlo method over a range of voltage offsets representing the expected threshold voltage drift for each transistor over different time periods.

2.1. Random Threshold Voltage Variations

To estimate failure probability of a sense amplifier, Monte-Carlo simulations are implemented in HSpice using predictive models for 32nm transistors [2], where threshold variation of each transistor is represented as a Gaussian function given by [4]:

$$\sigma_{Vt} = \left[\frac{qT_{ox}}{\varepsilon_{ox}}\sqrt{\frac{(N_a W_d)}{3L_{min}W_{min}}}\right] \times \sqrt{\frac{L_{min}W_{min}}{LW}} = \sigma_{Vt0} \times \sqrt{\frac{L_{min}W_{min}}{LW}} \quad (1)$$

In this way, random threshold variation is generated for each transistor independently in each simulation. In addition to random variations, each transistor's threshold voltage is offset by a calculated value representing the threshold voltage drift due to aging that would be observed for five considered time periods: 0 yrs., 0.25 yrs., 0.5 yrs., 1 yr., 2 yrs.

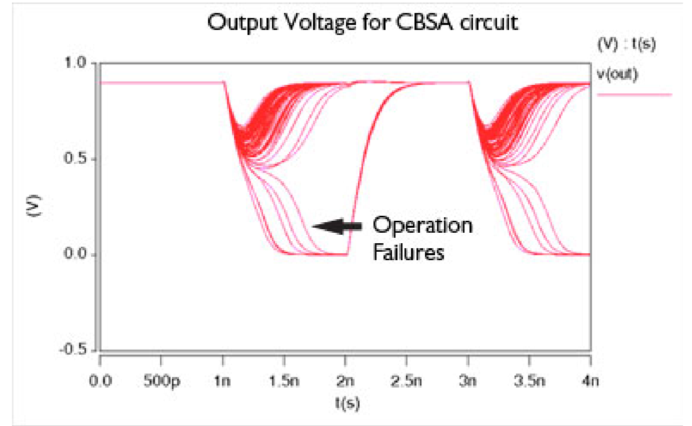

Figure 3: Output of the CBSA circuit showing operation failures

2.2. Threshold Voltage Drift Due to Aging

Threshold voltage drift due to aging, for both NBTI and PBTI effects, is calculated in Matlab using a model of BTI based on a modified equation [3]:

$$\Delta V_{th} = K_v \cdot \beta^{0.25} \cdot T^{0.25} + \delta_v \quad (2)$$

Where,

$$K_v \propto \sqrt{C_{ox}(V_{gs} - V_{th})} \cdot \exp(E_{ox}/E_0) \cdot \exp(-E_a/kT) \quad (3)$$

Here C_{ox} is the oxide capacitance, $E_{ox}=(V_{gs}-V_{th})/T_{ox}$, E_0=2MV/cm, E_a=0.13eV, k is Boltzmann's constant, δ_V=5mV, T=100°C, β is the duty cycle or stress period of the transistor [8]. For the initial time period we considered, 0 yrs., we generated 10,000 sets of voltage values, with the values in each set representing the threshold voltages of each transistor in the circuit, and each varied using our Gaussian function (1) to model initial variations in threshold voltage due to the fabrication process. For the following considered time periods or aging scenarios, 0.25 yrs., 0.5 yrs., 1 yr., 2 yrs., we generated 10,000 sets (each set containing a value for each transistor in the circuit) of voltage drift values per our BTI model (2). These values were themselves varied according to a normal distribution with a mean of our calculated ideal threshold voltage drift value (2) and a standard deviation of 10% of this calculated threshold voltage drift value. For each aging scenario after the initial 0 yrs. scenario, each set of voltages is the sum of the previous scenario and the calculated (but varied) set of threshold voltage drift values. In this way, threshold voltage values across each aging scenario will show continuously increasing voltage drift which should give a more realistic distribution than strictly using a normal distribution of threshold voltages at each aging bracket.

3. Failure Probability Estimation in Sense Amplifier

Simulations are repeated 10,000 times in HSpice using the calculated threshold voltages for each transistor, and the failure probability of each sense amplifier circuit is estimated as a ratio of "number of failures", or the number of simulations that show an improper "flipping" of output voltage implying an operation failure (**Figure 3**), to the "total number of simulations". It is known that increasing the variability of Vt for each transistor will increase the

probability of failure in both sense amplifier models [1]. Since the CBSA circuit is affected by both current and trip-point mismatch, increasing the variability of Vt will change the circuit's failure probability much more dramatically in the CBSA circuit than that of the VLSA circuit. We examine the effects to reliability of further voltage offset to Vt of each transistor for each circuit.

4. Different Scenarios of Aging and Transistor Duty Cycles

In this section, we consider different possible aging scenarios for the CBSA circuit. In an average case, it is equally probable that a sense amplifier reads a value of 0 or 1. Given this average input scenario, corresponding duty cycles are used to determine voltage offsets [9, 10] to each transistor's threshold voltage due to aging (**Figure 4**).

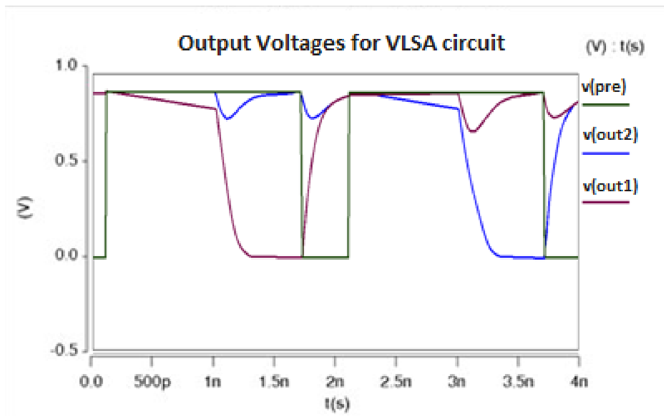

Figure 4: Output voltages of the VLSA circuit showing "average" operation

Likewise, it is also possible that the sense amplifier is consistently reading the same data, in which case transistors in the cross-coupled inverter will show duty cycle values of 0 and 1. This "worst-case" possibility would cause the most threshold voltage offset due to aging and possibly show more failures. In the CBSA design, the transistors Mn1 and Mn2 will almost always be asserted in normal operation of this design for both the "worst case" and "average case" scenarios, so their duty cycle values are 1. These considered scenarios are: (A) Both NBTI and PBTI in effect assuming average duty cycle values for each transistor, (B) Only NBTI in effect using the same average duty cycle values, (C) Only PBTI in effect using average duty cycle values, (D) Both NBTI and PBTI in effect using worst-case duty cycle values, (E) Only NBTI in effect with worst-case duty cycle values, (F) Only PBTI in effect using worst-case duty cycle values.

Table 1: Duty cycle values for each transistor in the CBSA circuit.

Transistor	Duty Cycle (average)	Duty Cycle (worst case)
Mn0	0.5	0.5
Mn1	1	1
Mn2	1	1
Mn3	0.75	1
Mn4	0.75	0.75
Mp1	0.25	0
Mpp1	0.5	0.5
Mp2	0.25	0.25
Mpp2	0.5	0.5

Table 2: Duty cycle values for each transistor in the VLSA circuit.

Transistor	Duty Cycle (average case)	Duty Cycle (worst case)
Mn0	0.5	0.5
Mn1	0.75	1
Mn2	0.75	0.75
Mp1	0.5	0.5
Mp2	0.5	0.5
Mp3	0.25	0
Mp4	0.25	0.25
Mpp3	0.2	0.2
Mpp4	0.2	0.2
Mpp5	0.2	0.2

A. Both NBTI and PBTI in effect assuming average duty cycle values for each transistor

This case assumes that it is equally probable the sense amplifier will read either a value of "0" or "1". In this scenario we observe the effects of both NBTI and PBTI on both CBSA and VLSA circuits assuming an "average" input.

B. Only NBTI in effect using the same average duty cycle values

This case, as above, also assumes an equal probability of the sense amplifier reading either a value of "0" or "1", but in this scenario we examine only the effects of NBTI on both CBSA and VLSA circuits. This will correspond to a scenario with threshold voltage drift only applied to the PMOS transistors, resulting in mismatch among the PMOS transistors making up the circuit. Though for NMOS transistors we still apply the initial variation in Vt, no further change due to aging effects is applied to these transistors for this scenario.

C. Only PBTI in effect using average duty cycle values

Again, as above, this case also assumes an equal probability of the sense amplifier reading either a value of "0" or "1", but in this scenario we examine only the effects of PBTI on both CBSA and VLSA circuits. This will correspond to a scenario with threshold voltage drift only applied to the NMOS transistors, resulting in mismatch among the NMOS transistors making up the circuit.

D. Both NBTI and PBTI in effect using worst-case duty cycle values

In the case, the sense amplifier is consistently reading the same data, so the stress or duty cycles will be unevenly distributed among the transistors making up the cross-coupled inverters corresponding to an input scenario that gives the most threshold voltage offset between transistors due to aging. Though this scenario is not realistic, it can be useful in finding the range of possibilities in failure probability.

E. Only NBTI in effect with worst-case duty cycle values

With an uneven distribution of duty cycles among the transistors making up the cross-coupled inverters, we observe the effect of only NBTI on both circuits. In addition to an uneven distribution of stress (and therefore, threshold voltage drift due to aging), by applying aging only to PMOS transistors, we would observe more threshold voltage mismatch among the transistors.

F. Only PBTI in effect with worst-case duty cycle values

This scenario examines the probability of failure due to an uneven distribution of stress among the transistors, but with only PBTI in effect (further Vt shift is applied only to NMOS transistors).

5. Results and Discussions

Using an aging model (2), we have found the voltage changes due to aging for each transistor for the time periods: 0 yrs., 0.25 yrs., 0.5 yrs., 1 yr., 2 yrs. By using these voltages to offset Vth for each transistor, we can see the effects of aging for the five time periods on the reliability of both the VLSA and the CBSA circuits.

A. CBSA SRAM circuit

The reliability of this circuit actually shows general improvement over time rather than degradation (**Table 3**). The threshold voltages at "Mn1" and "Mn2" show the most increase from the effects of BTI due to they being constantly stressed (their duty cycles being 1) (**Table 1**). Since both transistors show the same rate of increase in threshold voltage, the percentage of voltage change due to random threshold voltage variations will actually decrease for both transistors. This effect minimizes possible voltage offsets (percentage-wise) between the two transistors and so will reduce the probability of failure. In the scenarios where both NBTI and PBTI are in effect (scenarios A and D), there is improved reliability, due to the PBTI effects on transistors "Mn1" and "Mn2", even in the "worst case"(scenario D). In the cases where the effects of PBTI is absent (scenarios B and E), we do not observe any improvement in reliability, and, in fact, we see a decrease in reliability in the "worst case" (scenario E). Without the benefit of the decreased threshold voltage offset between transistors "Mn1" and "Mn2", the observed offset in the sourced currents at "Mn1" and "Mn2" will be increasingly determined by the especially stressed transistor "Mp1" (in scenario E). This being the case, the reliability will decrease as the stress between "Mp1" and "Mp2" are continuously uneven. In the scenarios where there is only PBTI in effect (scenarios C and F), the reliability is about the same when both PBTI and NBTI are in effect, which suggests the effect of minimizing the threshold voltage difference between "Mn1" and "Mn2" (percentage-wise) is more enough to offset the effects on reliability of threshold voltage mismatch among the other transistors.

Table 3: CBSA Probability of Failure for Different Scenarios
A: Both NBTI and PBTI (average)
B: NBTI only (average)
C: PBTI only (average)
D: Both NBTI and PBTI (worst case)
E: NBTI only (worst case)
F: PBTI only (worst case)

Scenario	Failures after 0 years	Failures after 0.25 yrs	Failures after 0.5 yrs	Failures after 1 yr	Failures after 2 yrs
A	11.14 %	10.59 %	10.55%	10.53%	10.45 %
B	11.14 %	11.14 %	11.14%	11.14%	11.14 %
C	11.14 %	10.59 %	10.53%	10.46%	10.43 %
D	11.14 %	10.56 %	9.97%	9.41%	8.88%
E	11.14 %	11.20 %	11.22%	11.31%	11.39 %
F	11.14 %	10.56 %	9.97%	9.41%	8.88%

B. VLSA SRAM circuit

The reliability of the VLSA circuit, as with the CBSA circuit, shows some improvement over time, though at a slower rate (**Table 4**). Only the trip-point mismatch reduction improves the reliability of the VLSA circuit as compared to this improvement combined with the improvement of current mismatch as with the CBSA circuit (**Table 3**). Since a current mismatch would not affect the VLSA circuit, only the reduction of trip-point mismatch improves the reliability and so a slower rate of improvement of reliability, if any, is observed. As with the phenomena observed with the CBSA circuit, the reliability of the VLSA circuit is improved through the equal stressing and aging of transistors "Mp1" and "Mp2" (**Table 2**). By increasing the threshold voltages of these two transistors, the percentage change of threshold voltage due to random variations decreases, thereby reducing the probability of trip-point mismatch and so reduces the probability of failure. While in the "average case" scenarios we see virtually no change in reliability (scenarios A, B, and C), in the "worst case" scenarios where PBTI is in effect (scenarios D and F) show some improvement. It should be noted, however, that the "worst case" scenarios are not probable.

Table 4: VLSA Probability of Failure for Different Scenarios
A: Both NBTI and PBTI (average)
B: NBTI only (average)
C: PBTI only (average)
D: Both NBTI and PBTI (worst case)
E: NBTI only (worst case)
F: PBTI only (worst case)

Scenario	Failures after 0 years	Failures after 0.25 yrs	Failures after 0.5 yrs	Failures after 1 yr	Failures after 2 yrs
A	1.25%	1.26%	1.26%	1.26%	1.26%
B	1.25%	1.25%	1.25%	1.25%	1.25%
C	1.25%	1.26%	1.26%	1.26%	1.26%
D	1.25%	1.20%	1.19%	1.18%	1.18%
E	1.25%	1.25%	1.25%	1.25%	1.25%
F	1.25%	1.18%	1.16%	1.17%	1.17%

6. Conclusions

The reliabilities of the CBSA and VLSA sense-amplifier circuits are improved with aging in most scenarios. Six possible scenarios for each circuit were examined and it was observed that the improvement is mostly due to the effects of PBTI in the CBSA circuit. Increasing the threshold voltage actually reduces the offset in the base NMOS transistors of the circuit, even under the conditions of random threshold voltage drift. In contrast to the CBSA circuit, however, the VLSA circuit shows resistance to the effects of transistor aging. It was found that SRAM cell sense amplifier circuits, though relatively sensitive to the effects of BTI, show an increase in reliability rather than a decrease. Though as transistors are scaled down, there is a significant decrease in sense amplifier reliability[1], the circuit's reliability will not be further decreased by the effects of BTI, and, in fact, can possibly be improved. It should be noted that though reliability is not degraded in some cases, there will likely be an increase in propagation delay due to the increase in threshold voltage values across all transistors [7].

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