Comparative Analysis of Copper and CNT Interconnects for H-Tree Clock Distribution

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***Abstract*— Clock distribution network is an important part of digital integrated circuits. The clock signal carried by the distribution network has to reach every end node at the same time to ensure synchronized switching. Due to mismatches among different nodes of the H-tree, the clock transitions among the final nodes of the distribution tree show some time difference, the maximum of which is called clock skew. In modern CMOS technologies, copper interconnect is popular for high level interconnects such as clock and power routing. Carbon Nanotube (CNT) exhibits less resistivity than copper making it a better material for interconnect. This paper compares the impact on clock skew of H-tree clock distribution network by replacing the traditional copper interconnects with carbon nanotube interconnects. By applying temperature mismatch, threshold voltage mismatch, and process mismatch, our findings show that using carbon nanotube interconnects reduces the clock skew significantly compared to traditional copper interconnects.**

***Index Terms*—Carbon Nanotube, Interconnects, H-tree, Clock Distribution Network, Clock Skew reduction, global clock tree**

I. Introduction

Clock signals are very important in synchronizing the data flow in synchronous digital circuits for correct computation. Due to special variations and mismatches between different clock routes, there are differences in arrival time of the clock edge at different end nodes of a clock distribution network. The maximum of such clock edge arrival time differences is known as clock skews [1].

Clock distribution networks ensure that mismatches and variations causing clock skew are minimized. Clock skew has grown to become a significant performance limiter in nano-scale designs. Clock signal is the most active signal in a chip causing significant amount of power consumption and current densities on the clock network interconnects. Copper interconnects are widely used for high current density interconnects found in power and clock networks. Carob-Nanotubes (CNT) have recently emerges as a competitive candidate for interconnect showing better current density and conductivity than copper.

In this research we have simulated an H-tree clock distribution network in a predictive 32 nm technology. The clock distribution network is a two-level H-tree. There is one H tree in the first level and 4 H-trees in the second level. A single H-tree has 6 buffers; therefore there are 30 buffers in the entire H-tree network. The buffers used in this H-tree network are CMOS inverters made using PMOS and NMOS transistors. The second level H-trees are situated at the four end nodes of the first level H-tree; they receive input from the end nodes of the first level H-tree.

The arrival time of clock signal at different points in a clock distribution network depends on several attributes like supply voltage, threshold voltage of the pmos and nmos transistors in the buffer circuit, temperature of the chip, and variation of temperature across various points in the die. We have simulated the above cases with a H-tree having Copper as well as CNT's as interconnect material. In case of carbon nanotube interconnects, we have developed several models to lower the contact resistance [3]. Studies have pointed that typically the contact resistance between carbon nanotube interconnect and a buffer is about 100kΩ. By increasing the number of contacts in parallel, the contact resistance can be reduced.

II. Power of H-tree

We have conducted a simple power analysis of the H-tree with the above mentioned configurations. Fig. 1 shows the power consumption of the H-tree in worst case scenario of 100^{O}C. In the ideal case (no contact resistance), the CNT based H-tree shows 22% less power consumption that the copper-based H-tree. The low power consumption is attributed to lower resistance of the clock interconnects which improve the rise and fall time of the clock signals resulting in less short-circuit power consumption on the clock-tree buffers. However, the advantage of the CNT interconnect reduces as the contact resistance increases. The power benefit reduces to 9% with 25kΩ contact resistance.

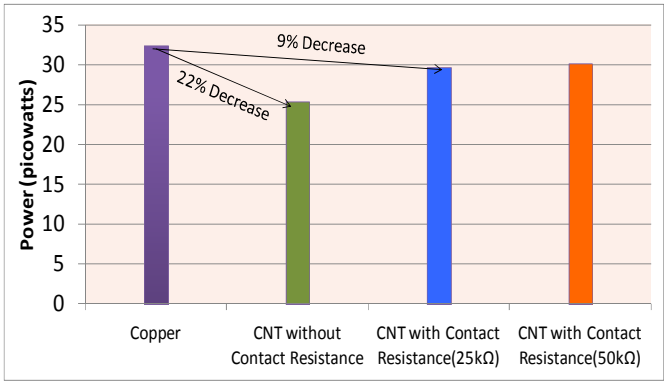

Fig 1. Worst Case Power Consumption of H-tree Clock Distribution Networks

III. Analysis of Clock Skew of H-Tree Network Arising Due to Supply Voltage Mismatch

We have applied a small voltage mismatch between the left and right half of the clock network. All the clock buffers in the left wing of the Clock tree are supplied with 0.8V of supply voltage and those in the right half of the H-tree are supplied

with a 1.0V supply voltage. Results show that CNT outperforms Copper in all cases of contact resistance (Fig. 2). The reduced clock skew is attributed to lower resistance of CNT compared to copper. With the ideal case of no contact resistance the clock skew improvement is 78%; however with the realistic 25 kΩ contact resistance, the improvement is 51%. Once again, it is observed that to exploit the maximum benefit from CNT interconnects, one has to minimize the contact resistance.

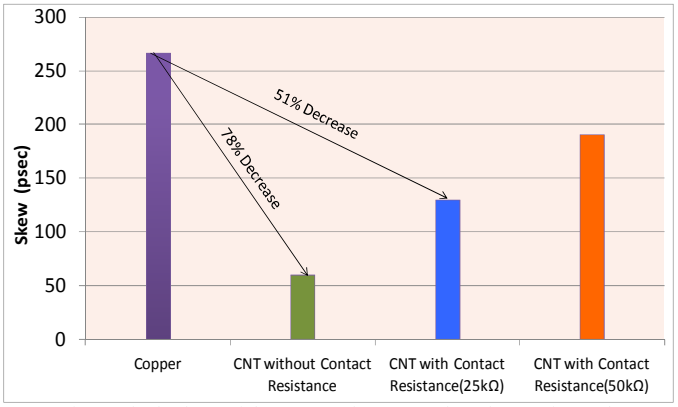

Fig 2: Clock Skew of the H-Tree due to supply voltage mismatch

IV. Analysis of Clock Skew of H-Tree Network Arising Due to Threshold Voltage (Vt) Mismatch

Spatial Vt variations is another cause of clock skew. To simplify the V_t mismatch analysis, we have divided the H-tree into two halves; namely the left half (L-Tree) and the right half (R-Tree). The clock buffers in the L-Tree are assigned lower V_t and the clock buffers in the R-Tree are given highr V_t. The V_t mismatch of 50mV is applied between the L-Tree and R-Tree. Fig 3 shows the Clock Skew of H-tree with V_t mismatch. It shows clearly that the clock skew is lower in all cases of CNT-based H-tree compared to Copper-based H-tree. The clock skew reduction is attributed to the reduced interconnect resistance offered by CNT. In the ideal case of no contact resistance the clock skew reduction is 52%; however, in the more realistic case of 25kΩ contact resistance, the clock skew is reduces by 24% when the copper interconnect is replaced with CNT interconnect.

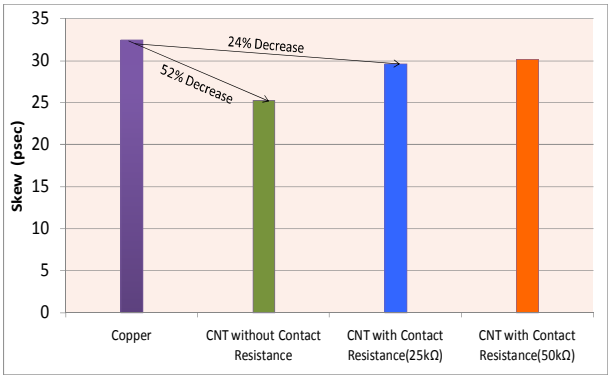

Fig 3: Clock Skew of the H-Tree due to threshold voltage mismatch

V. Analysis of Clock Skew of H-Tree Network Arising Due to Temperature Mismatch

Spatial temperature variation is another cause of clock skew. In this section, we focus on temperature mismatch and the impact of transistor aging. To simplify the analysis, the L-Tree is assigned lower temperature and the R-Tree is assigned higher temperature. The temperature mismatch we have applied is +/- 10 at 100 °C, i.e. 110 and 90 °C to the left and right half of the tree. In order to account for change in interconnect resistance as a result of temperature change, the first order temperature coefficients have been included in the H-tree Copper and CNT interconnect models. Fig. 4 shows the results of clock skew in each case. CNT without any contact resistance would have a clock skew 76% less compared to copper. CNTs with 25kΩ contact resistance shows clock skew reduction of 57% compared to copper interconnect.

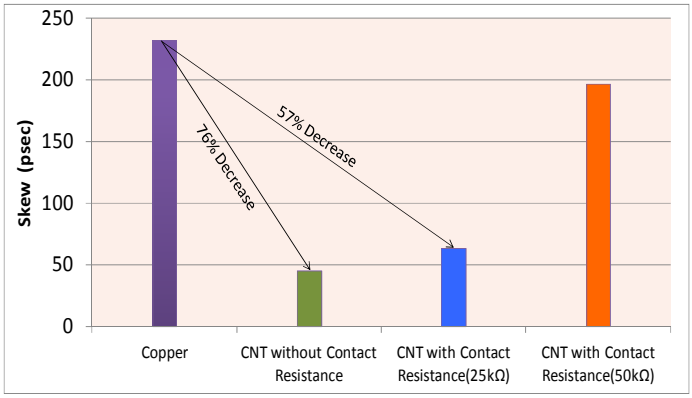

Fig 4: Clock Skew of the H-Tree due to temperature mismatch

VI. Conclusion

In this research, we have observed the impact on clock skew of H-tree clock distribution network by replacing Copper with CNT interconnects. Our results have consistently shown that CNTs outperform Copper interconnects in all cases of mismatch. Moreover, we observe that minimizing the contact resistance is critical to be able to fully exploit the benefits of CNT interconnects. By increasing the number of parallel contacts the overall contact resistance to CNT interconnect can be lowered.

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