Analysis of Reliability of Flip-Flops under Transistor Aging Effects in Nano-scale CMOS Technology

Vikram G Rao
San Francisco State University
vikramgrao@gmail.com

Hamid Mahmoodi
San Francisco State University
mahmoodi@sfsu.edu

***Abstract*— The effect of aging has become an important reliability concern in modern CMOS technology. NBTI and PBTI are known to bring about an increase in threshold voltage of the PMOS and NMOS respectively. This paper studies the effect of NBTI and PBTI on different flip-flop circuits with key parameters such as setup time, hold time, clock to output delay and data to output delay. The results in a predictive 32 nm technology show an increase of 0.43 to 1.23 pico-seconds in data-to-output delay depending on the Flip-Flop type. Moreover, we propose a method to use dual threshold voltage assignment to mitigate the effect of transistor aging on pulse triggered Flip-Flops. Dual V_{th} results show lower delay as well as 30% reduction in delay aging using the proposed dual threshold voltage method.**

I. INTRODUCTION

The Bias Temperature Instability (BTI) is considered as one of the major reliability concerns in modern CMOS technologies. BTI can be of two types: Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI). NBTI has been the major concern over the past few years and is known to largely affect PMOS devices while NMOS devices used to show negligible degradation [1]. However, as High-K metal gate usage was adapted in order to satisfy and extend Moore's law for the fabrication of newer technologies, it has been observed that there is a significant amount of degradation due to PBTI on NMOS devices as well. While the effects of NBTI show little or no improvement from SiO_2 to High-K gate, PBTI has become a major degradation factor for NMOS devices and is considered to be a greater reliability concern for all High-K devices in the future [2]. Since Flip-Flops are widely used for storage in pipelined architectures, their timing characteristics generally determine the operating frequency of the circuit [3].

This paper studies the combined effect of NBTI and PBTI on Flip-Flop circuits with the usage of a predictive 32 nm CMOS technology. Our unique contributions in this paper are as follows:

- We present the combined effect of NBTI and PBTI on six widely used flip-flops.
- The study is performed in a predictive 32nm technology which represents a high-k metal gate CMOS technology.
- We propose a new way of using dual threshold voltage (V_{th}) assignment for reducing the impact of device aging on the performance of the Hybrid Latch Flip-Flop.

II. RESULTS AND DISCUSSIONS

In order to obtain the effect of aging, all simulations for NBTI and PBTI have been performed using Synopsys H-Spice tool. The BTI aging was estimated for each individual transistor in a Flip-Flop circuit using its own parameters of stress for over a period of 5 years. We present results for Setup time, Hold time, and Clock to Output and Data to Output delays. Since Data to Output is the best parameter to judge the overall delay of the circuit, it is used as a final metric of comparison. Since we consider both NBTI and PBTI, both output transitions, low to high and high to low, must be considered in any timing measurement. Thus, we report the timing metrics as their average for low-to-high and high-to-low output transitions. The increase is the difference of the aged value of a metric to the original value of the metric. The timing aging results of various flip-flops are shown in Tables I, II, and II.

Table I: Setup Time measurements

Setup Time	Original (pS)	Aged (pS)	Increase (pS)
MODMSFF	7.5	7.5	0
TGMSFF	8	8.5	0.5
C2MOSFF	22	22.5	0.5
HLFF	-10.5	-11	-0.5
SDFF	-14.5	-15	-0.5
SAFF	-8	-8	0

Table II: Clock to output delay measurements

Clock to Output Delay	Original (pS)	Aged (pS)	Increase (pS)
MODMSFF	10	10.39	0.39
TGMSFF	17.03	17.90	0.87
C2MOSFF	7.72	7.95	0.23
HLFF	13.52	14.08	0.56
SDFF	17.68	18.25	0.57
SAFF	29.50	30.38	0.88

Table III: Hold Time

Hold Time	Original (pS)	Aged (pS)	Increase (pS)
MODMSFF	-5	-5.5	-0.5
TGMSFF	-5	-5	0
C2MOSFF	-22	-22	0
HLFF	14.5	14.5	0
SDFF	16	16	0
SAFF	9	10	1

Table IV shows the measurement results of minimum data to output delay. All flip-flops show an increase in the data to output delay. TGFF shows the largest increase in data to output delay which is due to its long path between the data input and output. It is observed that the pulse triggered flip-

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flops (HLFF and SDFF) show least increase in their delay aging. That is because by transistor aging the transparency window increase which has an opposite effect on the total flip-flops delay. The HLFF shows the least amount of delay increase which is 0.43 pS. Additionally, HLFF shows significantly lower delay compared to the other flip-flops. Thus, it is clear that HLFF is not only the fastest circuit, but also the most resilient to aging. In the next section, we propose a design technique to further reduce the sensitivity of this flip-flop to aging.

Table IV: Data to Output Delay

Data to Output Delay	Original (pS)	Aged (pS)	Increase (pS)
MODMSFF	22.20	22.89	0.69
TGMSFF	35.84	37.07	1.23
C2MOSFF	37.25	38.26	1.01
HLFF	12.95	13.38	0.43
SDFF	14.82	15.44	0.61
SAFF	28.31	29.04	0.73

III. DUAL THRESHOLD VOLTAGE FOR AGING RESILEINCE

In-order to achieve a Flip-Flop design that is largely resilient to aging, it is important to make design changes that would reduce the impact of the aging on the critical path of the flip-flop. Dual threshold voltage (Dual V_{th}) is already a popular method for a low power design [4]. With dual V_{th} designs, non-critical paths are made high V_{th}, which would reduce the leakage, and critical paths are made low V_{th} which improves performance. Dual threshold voltage is also easy to fabricate by adding an additional mask layer during fabrication. Here, we propose use of dual V_{th} for reducing impact of transistor aging on circuit delay. A higher V_{th} transistor is expected to show less aging (V_{th} shift) due to reduction in the electric field stress in the oxide (E_{ox}). Hence it is expected that a high V_{th} circuit is less sensitive to transistor aging.

Here we investigate proper dual V_{th} assignment for reducing the sensitivity of delay of implicitly pulsed flip-flops (HLFF and SDFF) to transistor aging. The overall delay of the inverters/NAND chain of gates in HLFF and SDFF define the transparency window for data sampling [10]. The aging of the inverters/NAND gate results in increase of the transparency time window, and hence reduction in setup time by aging. There are two ways to assign dual V_{th} to the flip-flops: assign low V_{th} to the pulse generating section and high V_{th} to the rest of the circuit and vice-versa. Thus, we investigate four Flip-Flop circuits: LVTHLFF (HLFF with pulse generating section Low V_{th} and rest of the circuit High V_{th}), HVTHLFF (HLFF with pulse generating section high V_{th} and rest of the circuit low V_{th}), LVTSDFF (SDFF with pulse generating section Low V_{th} and rest of the circuit High V_{th}) and HVTSDFF (SDFF with pulse generating section High V_{th} and rest of the circuit Low V_{th}).

Table VIII: Data to Out Delay measurements with dual V_{th} assignment

Data to Q	Original (pS)	Aged (pS)	Increase(pS)
HLFF	12.95	13.38	0.43
LVTHLFF	15.27	15.60	0.33
HVTHLFF	11.30	11.63	0.33
SDFF	14.82	15.43	0.61
LVTSDFF	17.67	18.41	0.74
HVTSDFF	12.34	12.78	0.43

Table VIII shows the minimum data to output delay results of the dual V_{th} assignment. It is observed that application of high V_{th} to the pulse generator reduces the minimum data to output delay which is justified by increased transparency time window. Moreover, the amount of delay aging (increase) is also reduced by assigning high V_{th} to the pulse generator. Compared to the original HLFF, the HVTHLFF reduces the delay by 23%. Compared to the original SDFF, the HVTSDFF reduced the delay increase by 30%. Assignment of low V_{th} to the pulse generator is not recommended because it increases the total delay. Moreover low V_{th} pulse generator causes more delay aging in the case of SDFF.

The above results indicate that the proper way of applying dual V_{th} under transistor aging is to assign high V_{th} to the pulse generator and low V_{th} to the rest of the flip-flops circuit. This assignment not only reduces the overall delay of the flip-flop, but also makes it more resilient to aging.

IV. CONCLUSION

In this paper, we have discussed the combined effect of both NBTI and PBTI on various Flip-Flop circuits. Comparative analyses of the flip-flops were presented using the timing metrics in response to transistor aging. The results indicate that the pulse triggered flip-flops show better tolerance to transistor aging. This is due to the fact that transistor aging increases the transparency time window which has an opposite impact on delay. Moreover, we propose a unique way for applying dual V_{th} to the pulse triggered flip-flops to further improve their tolerance to transistor aging. In the proposed dual V_{th} assignment method, high V_{th} is assigned to the pulse generator section of the flip-flop while the rest of the flip-flop circuits is assigned low V_{th}. This assignment rescued the delay aging by 23% and 30% for HLFF and SDFF, respectively.

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