

Comparative BTI Reliability Analysis of SRAM Cell Designs in Nano-Scale CMOS Technology

Shreyas Kumar Krishnappa, Hamid Mahmoodi
School of Engineering, San Francisco State University, San Francisco, CA USA
E-mail: shreyas.shreyas@live.com

Abstract—Bias Temperature Instability (BTI) causes significant threshold voltage shift in MOSFET using Hafnium-dioxide (HfO_2) High- k dielectric material. Negative BTI and Positive BTI are two types of BTI effects observed in p-channel and n-channel MOSFET. BTI affects the stability and reliability of conventional six transistor (6T) SRAM design in nano-scale CMOS technology. Eight transistor (8T) and Ten transistor (10T) SRAM cell designs are known for their ability to operate at lower supply voltages to reduce power consumption. In this paper, we present a comparative analysis of different SRAM cell designs in terms of their reliability against BTI effects. For a fair comparison, voltage scaling is applied to the 8T and 10T cells to a level where they show same Static Noise Margin (SNM) as that of the 6T cell at nominal supply voltage. In a predictive 32 nm CMOS technology, the supply voltage of 8T and 10T cells is reduced to 0.42 V which is 54% lower than the nominal supply voltage (0.9 V), which the 6T cell is biased at. Due to lower supply voltage in 8T and 10T SRAM designs, the impact of BTI is lower and reliability is far better than the 6T SRAM design, while achieving significant leakage power reduction. Based on the simulation results, we recommend designing SRAM arrays using 8T SRAM cell or 10T SRAM cell in future nano-scale CMOS where BTI effect is a reliability barrier for SRAM design.

Keywords—SRAM, 6T, 8T, 10T, Bias Temperature Instability (BTI) effect, MOSFET, Nano-scale CMOS, voltage scaling, SRAM, Static Noise Margin (SNM), write margin, access time, leakage power

I. Introduction

With recent introduction of High- k material to avoid gate tunneling effect, device reliability issues have become a major challenge in 32 nm node and beyond. Circuit lifetime is reduced due to threshold voltage (V_{th}) shift caused by Bias temperature instability (BTI) [1] due to interface charge trap generated during device “ON” state. BTI is classified into Negative BTI in p-channel MOSFET and Positive BTI in n-channel MOSFET. Change in V_{th} is dependent on applied electrical field, time and temperature. It is crucial to analyze the impact of BTI on different Static Random-Access Memory (SRAM) designs. Conventional six transistors (6T) SRAM cell is significantly affected by V_{th} variation due to BTI effect.

This affects the stability of 6T SRAM in terms of Static noise margin (SNM), Write Margin (WM), Read Margin (RM), and leakage power, in 32 nm and beyond. Alterna-

tive SRAM circuit designs are favored to replace 6T SRAM in 32 nm node [2]. We have analyzed 8T [3] and 10T [4] SRAM cells to show that their cell stability is better than the conventional 6T SRAM cell in the presence of transistor aging effects. The stability is improved by isolation of Write-word line and Read-word line. To the best of our knowledge, for the first time, we have applied BTI V_{th} shift to 8T and 10T SRAM cells and compared the results of aging with 6T SRAM cell in nano-scale CMOS technology.

Negative bias temperature instability (NBTI) is deeply studied for silicon-dioxide (SiO_2) dielectric but for Hafnium (Hf) oxide positive bias temperature instability (PBTI) is reported to be also major bottleneck in deep sub-micron technologies [5]. In this paper, we have studied the combined effect of NBTI and PBTI effect in Hafnium-dioxide (HfO_2) dielectric devices. Incorporating additional transistors in 6T SRAM enhances the SRAM reliability but comes with a penalty of increased chip area. It has recently been reported that 6T SRAM can be used until 15 nm node by upsizing the transistors for suitable SRAM operation with supply voltage (V_{dd}) of 1.1 V to 1.2 V [6]. For further scaling of supply voltage and channel length, alternative SRAM circuit designs are necessary in future technologies [1]. Our simulations are performed in a predictive high performance 32 nm model [7–8] to observe the stability of different SRAM designs under combined NBTI and PBTI effects. The nominal supply voltage of 32 nm technology is 0.9 V which is used for the biasing of 6T SRAM cell. 8T, 10T SRAM designs show enhance Static Noise Margin (SNM) at nominal supply voltage compared to the 6T design. The common method of exploiting the improved SNM is to reduce the supply voltage for reducing power consumption. For a fair comparison, we have scaled the supply voltage of the 8T and 10T design to 0.42 V where their SNM becomes same as the SNM of the 6T design at nominal supply voltage (0.9 V) without applying BTI effects in all three SRAM cell designs. Then, we have applied BTI effects on all three SRAM cell designs to compare their reliability.

BTI effects are dependent on both process parameters (such as V_{th}) and environmental parameters (such as voltage and temperature). The combined effect of process, voltage and temperature on BTI effects for circuit analysis is reported in [9]. This paper presents a comparative analysis of SRAM cell designs with combined effect of voltage scaling and BTI effects. An overview of the model of threshold voltage shift caused by BTI is discussed in Section II. Section III presents analysis and impact of BTI on 6T, 8T, 10T SRAM cell designs in 32 nm node. The dis-

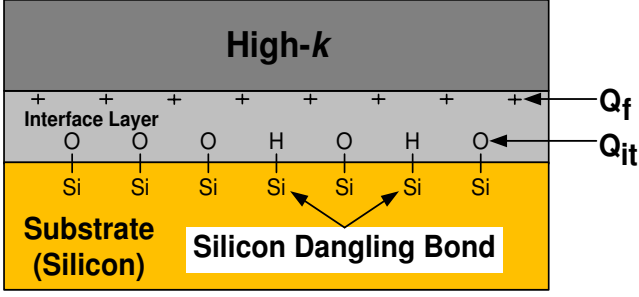


Fig. 1. Charges associated with High- k /Si interface. H ions are created during stress from Silicon dangling bonds.

discussion then turns to a rigorous comparison of simulation results after a brief qualitative description of write and read margin, and leakage power in Section IV. Section V draws the conclusions.

II. BTI Model Integrating Process, Voltage and Temperature Dependence

A BTI model is used to estimate the shift (increase) in threshold voltage (V_{th}) in a predicted 32 nm technology for High- k dielectric with metal gate [7], [8]. Threshold voltage shift is directly related to oxide and silicon interface traps as expressed by:

$$\Delta V_{th} = \frac{Q_{ss}}{C_{ox}} = \frac{q \times D_I}{C_{ox}} \quad (1)$$

where, Q_{ss} is the oxide charge per unit area at Oxide-Silicon interface, C_{ox} is gate oxide capacitance per unit area (ϵ_{ox}/T_{ox}), q is the electron charge, D_I is the final dose of impurity implants after all diffusion steps is followed during fabrication process. It is evident from Eq. (1) that minimizing threshold voltage variation can be obtained by introducing controlled amount of Q_{ss} during fabrication. Fig. 1 presents the charges found at semiconductor and insulator (High- k) interfaces. Q_f is fixed oxide charge and Q_{it} is interface trap charge. High temperature annealing at 900°C to 1000°C is used to minimize Q_f and low temperature annealing at 400°C to 500°C with 10% H_2 in N_2 is used to minimize Q_{it} . Every transistor (on wafer) undergoes these process steps, irrespective of N-MOS or P-MOS. Thus Hydrogen (H) is the main component that satisfies the Silicon (Si) dangling bonds initially. During, voltage stress hydrogen is replaced by majority charge from MOS-FET channel due to weakening of hydrogen-silicon ($H-Si$) bond at the interface and Hydrogen is released from Silicon bond. The replacement with majority charge carriers will shift (increase) the device threshold voltage, known as BTI effect (aging effect).

We have simplified the BTI model in [8] to highlight the voltage and temperature dependence of the BTI effect as follows:

$$\Delta V_{th} = K_v \cdot \beta^{0.25} \cdot t^{0.25} + \delta_v \quad (2)$$

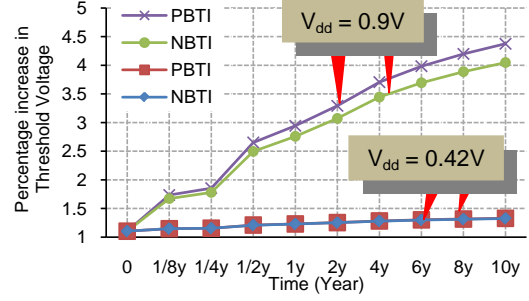


Fig. 2. Percentage increase in threshold voltage over life-time due to NBTI and PBTI.

Where:

$$K_v = A \cdot T_{ox} \cdot \sqrt{C_{ox}(V_{dd} - V_{th})} \cdot \exp\left(\frac{E_{ox}}{E_o}\right) \cdot \exp\left(-\frac{E_a}{kT}\right)$$

$$E_{ox} = \frac{(V_{dd} - V_{th})}{T_{ox}}$$

$$T_{ox} = \frac{3.9}{K} \cdot t_{hk}$$

where, K_v is the rate at which H^+ species are generated, β is percentage of time for device is under stress ($\beta=1$ for DC stress and $\beta<1$ for AC stress), and t is the total time. T_{ox} is the effective oxide thickness (EOT) which is smaller than the physical thickness of the dielectric in the case of high- k [10]. K is relative permittivity of the high- k material, t_{hk} is the thickness of high- k . C_{ox} is oxide capacitance per unit area, V_{dd} is supply voltage and V_{th} is threshold voltage. E_{ox} is the electric field in the oxide and E_a is activation energy. k and T are Boltzmann constant and temperature in Kelvin, respectively. Other parameters such as d_v , A , and E_o are 5 mV, 1.8 mV/nm/ $C^{0.5}$, and 2 MV/cm, respectively [8]. The dependence of BTI induced V_{th} shift to supply voltage (V_{dd}) and temperature (T) is clear from Eq. (2). Higher supply voltage and temperature results in more V_{th} shift [9].

Fig. 2 shows percentage increase in V_{th} over time due to PBTI and NBTI for N-MOS and P-MOS respectively, at two stress voltages of 0.9 V and 0.42 V at 100°C. 0.9 V is the nominal supply voltage and 0.42 V is chosen because the 8T and 10T will be biased at this supply voltage as will be explained in Section III. As evident from Eq. (2), the rate of aging depends on supply voltage. BTI induced V_{th} increase is higher at higher supply voltages.

III. Analysis of Aging Effects in SRAM Designs

Reliability is of utmost importance in various SRAM designs. For the first time, we have compared different SRAM designs in terms of their reliability against the aging effects in 32 nm CMOS process. Fig. 3(a) shows the schematic of 6T SRAM cell. The 6T cell is composed of a pair of cross-coupled inverters that provide the storage. The ac-

cess transistors, M5 and M6, provide read and write operations. The cell supply voltage is 0.9 V.

To understand the impact of transistor aging on stability of the 6T SRAM cell, consider the case when the cell is storing $Q='1'$ and $\bar{Q}='0'$ for a long period of time. In this situation, the transistors M1 and M4 are under stress and therefore aging is observed by increased threshold voltage. Increased threshold voltage of M1 and M4 in this case, reduces the level of read SNM [9]. This is primarily because of increased voltage noise at the \bar{Q} nodes during read operation due to increased threshold voltage of the pull-down transistor, M1, and the reduced trip point of the inverter M3-M4 due to increased threshold voltage of M4. The aging of the access transistors (M5, M6) can be neglected because they are “OFF” most of the time ($\beta \approx 0$), once we consider an SRAM array with a large number of cells. 8T and 10T SRAM cell designs improve the read SNM of the SRAM cell by introducing extra transistors to buffer the cell for read operation, and hence avoiding any disturbance to the cell during the read operation [3–4]. The 8T and 10T SRAM cells are shown in Fig. 3(b) and 3(c), respectively. Stability of the SRAM cell is increased by separating write and read bit lines. The additional two N-MOS transistors, M7 and M8, form a buffer for the cell during read operation, and hence, isolating the read bit line ($RdBL$) from the cell. In 8T SRAM bit-line leakage is not fully eliminated. In 10T design, the bitline leakage is reduced by adding two more transistors, M9 and M10, as shown in Fig. 3(c).

The 6T cell is simulated to measure read SNM without applying BTI (aging) effect at initial stress time ($t=0$) at the temperature of 100°C and supply voltage of 0.9 V. The initial SNM obtained for these conditions is 115 mV. The 8T and 10T cells show larger SNM than that of the 6T cell, when compared at the nominal supply voltage of 0.9 V. Therefore, we lower the supply voltage of the 8T and 10T cells to a point where their initial SNM becomes same as that of 6T cell at the nominal supply voltage. The 8T, 10T cell show same initial SNM of 115 mV at the scaled supply voltage of 0.42 V. Table I shows the measurements of the SRAM cells as the supply voltages that are adjusted for the same SNM of 115 mV, without aging effect. Equally balanced SNM at adjusted supply voltages is required for a fair comparison between the three SRAM designs. For the rest of the paper, the results of the 8T and 10T cells are reported for the scaled supply voltage of 0.42 V. Table II shows the numerical results of aging in different SRAM performance parameters for all the three SRAM cells. In applying aging to the cell transistors, we have considered the worst case scenario of aging for a given performance parameter. For example assuming the state of $Q='1'$ and $\bar{Q}='0'$ in the cell, the worst case aging for the SNM is when only M1 and M4 age (the cell never changes the state during lifetime). The worst case scenario for aging of access time is the same. In this state, the aged pull-down transistor, M1 in the case of the 6T, or M7 in the case of 8T and 10T, will results in increase of access time. Notice that we have neglected the aging of the access transistors

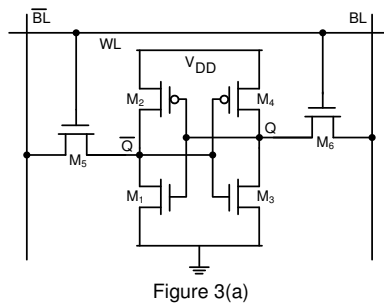


Figure 3(a)

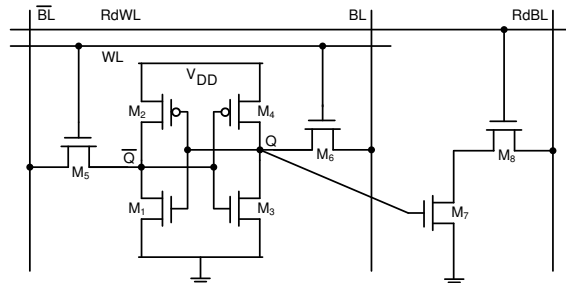


Figure 3(b)

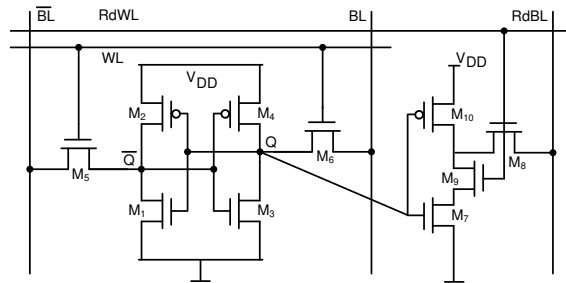


Figure 3(c)

Fig. 3. Schematic of (a) Six transistor (b) Eight transistor with separate read word line and read bit line with M7 and M8 [3] (c) Ten transistor with M9 and M10 to lower leakage power [4].

connection to the word-line (WL) due to very low stress probability once the cell is used in a large SRAM array. For the aging of write margin, the worst case scenario is when the cell after storing the same state for a long time is written to the opposite state and then is rewritten the same state back in the next cycle (second write). On the second write attempt, the write margin will be degraded due to the un-aged P-MOS (M2) pull-up transistor that keeps node \bar{Q} at ‘1’. Aging favors the leakage power as increased V_{th} results in less sub threshold leakage. Since the leakage of a large SRAM array is the sum of leakages of many individual cells which will be in different states, we have considered an average scenario of aging for each transistor of the cell ($\beta=0.5$) in order to estimate the impact of aging on leakage power of the cell.

From Table II, it is observed that initial SNM for all three SRAMs instantly drops to 113 mV at time zero. This is due to the instant increase in V_{th} upon power up which is modeled as the constant δV in Eq. (2). Fig. 4 shows the percentage of reduction in SNM of the SRAM cells at their respective supply voltages over time. It is clear that SNM degradation is less in the case of 8T and 10T SRAM cells

TABLE I
SUPPLY VOLTAGE ADJUSTMENT OF SRAM CELLS FOR SAME SNM = 115 mV

| Cell | With-out Aging effect at 100°C | | | |
|------|--------------------------------|------------------|---------------------|--------------------|
| | Supply Voltage (V) | Write Margin (V) | Access Time (n sec) | Leakage Power (nW) |
| 6T | 0.9 | 0.296 | 0.432 | 32.7 |
| 8T | 0.42 | 0.110 | 17.9 | 1.99 |
| 10T | 0.42 | 0.109 | 31.3 | 1.96 |

TABLE II
AGING OF SRAM PARAMETERS

| Year | Simulation results With-applied Aging effect at 100°C | | | | | | | | | | | |
|------|---|-------|-------|------------------|-------|-------|---------------------|------|------|--------------------|---------|---------|
| | Read SNM (V) | | | Write Margin (V) | | | Access Time (n sec) | | | Leakage Power (nW) | | |
| | SRAM cell | | | SRAM cell | | | SRAM cell | | | SRAM cell | | |
| | 6T | 8T | 10T | 6T | 8T | 10T | 6T | 8T | 10T | 6T | 8T | 10T |
| 0 | 0.113 | 0.113 | 0.113 | 0.295 | 0.109 | 0.108 | 0.433 | 18.8 | 32.3 | 32.6673 | 1.95103 | 1.95099 |
| 1/8 | 0.111 | 0.113 | 0.113 | 0.295 | 0.109 | 0.108 | 0.433 | 18.8 | 32.3 | 32.6655 | 1.95053 | 1.95049 |
| 1/4 | 0.111 | 0.113 | 0.113 | 0.295 | 0.109 | 0.108 | 0.433 | 18.8 | 32.3 | 32.6655 | 1.95053 | 1.95049 |
| 1/2 | 0.109 | 0.112 | 0.112 | 0.294 | 0.109 | 0.108 | 0.435 | 18.9 | 32.3 | 32.6655 | 1.95031 | 1.95027 |
| 1 | 0.109 | 0.112 | 0.112 | 0.294 | 0.109 | 0.108 | 0.435 | 18.9 | 32.3 | 32.6646 | 1.95019 | 1.95015 |
| 2 | 0.108 | 0.112 | 0.112 | 0.294 | 0.109 | 0.108 | 0.435 | 18.9 | 32.3 | 32.6646 | 1.95002 | 1.94998 |
| 4 | 0.107 | 0.112 | 0.112 | 0.294 | 0.109 | 0.108 | 0.435 | 18.9 | 32.4 | 32.6637 | 1.94981 | 1.94981 |
| 6 | 0.107 | 0.112 | 0.112 | 0.293 | 0.109 | 0.108 | 0.435 | 18.9 | 32.4 | 32.6637 | 1.94969 | 1.94965 |
| 8 | 0.106 | 0.112 | 0.112 | 0.293 | 0.109 | 0.108 | 0.435 | 18.9 | 32.4 | 32.6628 | 1.94960 | 1.94956 |
| 10 | 0.106 | 0.112 | 0.112 | 0.293 | 0.109 | 0.108 | 0.435 | 19.0 | 32.4 | 32.6628 | 1.94952 | 1.94948 |

compared to the 6T SRAM cell. It is observed that overall SNM reduction for the 8T and 10T cells is 4.26% which is less than the 6.09% SNM reduction observed for the 6T cell in 10-year life-time. The reduced impact of aging on the SNM of 8T and 10T cells is attributed to the lower operating supply voltage because the rate of aging is lower at low supply voltage as shown in Fig. 2 and Eq. 2.

IV. Effect of Aging on SRAM Performance Parameters

In this section, we explain the comparative impact of aging effects on the remaining SRAM performance parameters; namely, write margin, access time, and leakage power.

A. Write Margin

To consider the worst case of aging for the write margin, we measure the write margin for a cell that has been in a fixed state for a long time and then experiences a write to an opposite value and immediately followed by a second write operation to re-write the original value back to the cell. During the second write cycle, the write margin of the cell is reduced due to the pull-up action of the un-aged P-

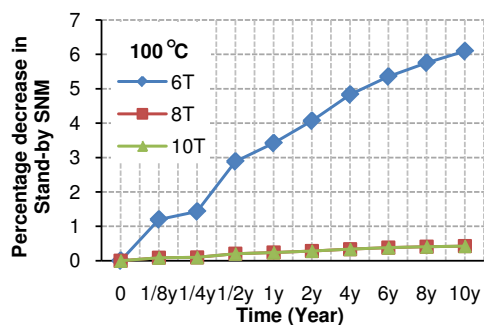


Fig. 4. Percentage decrease in Stand-by SNM. 8T, 10T have least change over 6T. Approximately 7% decrease in 6T device over 10 years of lifetime.

MOS which resists the change on the node storing '1'. The write margin is measured by applying a DC noise source to the bit-line that is at the zero level during the second write operation. The noise level is increased to a point where the write operation fails. This noise level is called write margin. As seen from the result Tables (I & II), 8T and 10T cells have nearly similar write margin because of isolation of read and write operations and therefore having identical write paths. Also, the write margin of the 8T and 10T is

relatively less compared to that of the 6T cell, because of lower operating supply voltage. However, the percentage of reduction in write margin caused by aging effects is less in the case of 8T and 10T cells, as shown in Fig. 5. It is observed that write margin reduction for the 6T cell is 0.63% over 10 years of life time, whereas, the write margin of the 8T and 10T cells reduce by 0.20% over the same life-time. The reduced impact of the transistor aging on the write margin of the 8T and 10T cells is attributed to their lower operating voltage.

B. Access Time

The access time is determined by the time it takes for the cell to develop a minimum required voltage drop on the bitline (~ 100 mV) [11]. In the 6T cell, the read path is via the access and the pull-down transistor (M1 and M5 in Fig. 3(a)). In the case of the 8T and 10T cell, the cell is buffered and hence the read path is via the access transistor and the buffer pull-down path (M7 and M8 in Fig 3(b) and M7, M8, and M9 in Fig. 3(b)). As mentioned earlier, the aging of the transistors (M5, M6, M8, and M9) connect to the word line is neglected due to their very low “ON” time ($\beta \approx 0$). The worst case scenario for the impact of the BTI aging on the access time is when the cell remains in a fixed state ($Q=‘1’$; $\bar{Q}=‘0’$) for a long time such that the transistors M1 and M7 are aged with a DC stress pattern ($\beta \approx 1$).

It is observed from Table II that 8T and 10T cells show longer access time which is due to lower operating supply voltage. 10T cell has the longest access time because of the extra transistors in the read path (M9 and M10 in Fig, 3(c)). Fig. 6 shows percentage increase in access time over the life-time. It is observed that the percentage degradation in access time is more in the case of 8T SRAM (1.03% over 10 years) compared to 10T and 6T cells (0.58% and 0.54%, respectively). The higher sensitivity of the access time of the 8T cell to the aging is due to the increase sensitivity of the read path to V_{th} at the low operating voltage. Reduced sensitivity of the access time to aging in the 10T cell compared to the 8T cell is because of having a longer read path in which only one transistor (M7) out of the 3 transistors (M7, M8, and M9) is aged. Nonetheless, the amount of change in the access time is quite small in all the SRAM cells.

C. Leakage Power

Leakage in the SRAM cell is mainly caused by the sub threshold leakage which occurs on the “OFF” transistors. Hence, the BTI induced V_{th} increase which happens on the ON transistors does not impact the leakage of the cell unless the cell changes state and the “ON” transistors become “OFF”. Leakage in a large SRAM arrays is the sum of the leakages of many identical cells in the array. It would be unrealistic to assume all the cells in a large SRAM array will not change state during the life-time. Hence, we

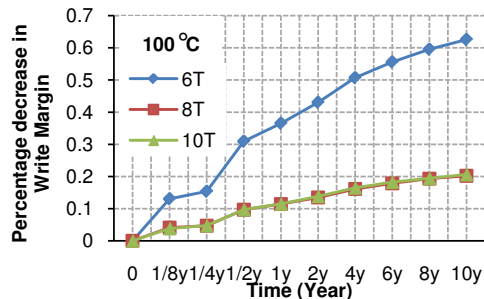


Fig. 5. 6T cell is operated in 0.9V, 8T and 10T cell in 0.42V. Hence, aging effects in 8T and 10T have minimum decrease in write margin for power scaled to obtain same SNM in Section III.

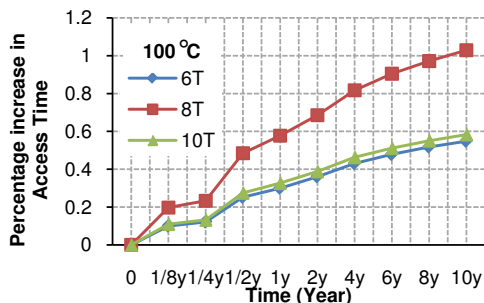


Fig. 6. Despite of increased read margin in 8T, 10T cell. Percentage increase is observed for 8T, 10T cell (negligible). 6T cell is more sensitive to variations in 32nm technology. The absolute values in Table II provide information about 6T sensitivity to read time increase.

assume a 50% stress probability ($\beta=0.5$) on all the transistors in the cell except those connected to the word-lines. Such increase in V_{th} of transistors results in reduction of the leakage of the SRAM cells on average over the lifetime. Table II presents simulated results of leakage power of the SRAM cells and the average reduction over life-time. It is observed that the 8T and 10T show less leakage power than the 6T cells, which is due to the lower operating supply voltage. 10T cell shows less leakage than the 8T cell which is due to the reduction in the bit-line leakage by introducing the extra transistors (M9 and M10). Fig. 7 presents the percentage of reduction in average leakage power over the life-time caused by aging effects. 6T cell experiences almost negligible reduction in the leakage power, while 8T cell and 10T cells exhibit 0.077% average reduction in their respective leakage power over a 10-year life-time.

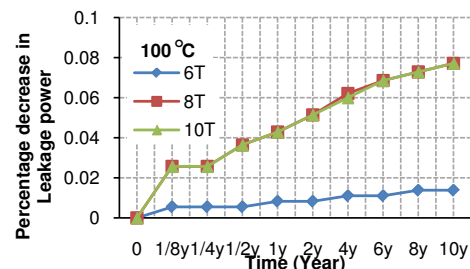


Fig. 7. Leakage power - percentage decrease is highest for 10T cell at 100°C. The absolute leakage power decrease in 6T is to its maximum and saturates at 0.9V.

V. Conclusion

A comparative analysis of performance of 6T, 8T, and 10T SRAM cells were conducted under BTI aging effects in a predictive 32 nm CMOS technology with High- k metal gate transistors. 8T and 10T cells enable lower supply voltage which provides advantages for reducing power consumption. In this study, we have shown that the lower operating supply voltage of the 8T and 10T cells is of advantage when considering the transistor aging effects. The 8T and 10T cells experience much less reduction of their SNM as a result of the transistor aging effects. The impact of the aging on write margin and access time is negligible; however, the 8T and 10T cells exhibit less reduction in write margin caused by aging. The reliability advantage of 8T and 10T SRAM cells make them an excellent choice for low power and reliable SRAM design in nano-scale technologies and in the presence of transistor aging effects.

ACKNOWLEDGMENT

The authors gratefully acknowledge Dr. Clark Nguyen for valuable discussions in High- k processes. The authors would like to acknowledge Synopsys Inc. for their hardware and EDA tool support through Charles Babbage university grant.

REFERENCES

- [1] International Technology Roadmap for Semiconductors. [Online]. Available: <http://www.itrs.net/>
- [2] C.-T. Chuang, S. Mukhopadhyay, J.-J. Kim, K. Kim, R. Rao, "High-performance SRAM in nanoscale CMOS: Design challenges and techniques," in *IEEE Int. Workshop., Memory Technology, Design and Testing*, Taipei, Taiwan, Dec. 3-5, 2007, pp. 4-12.
- [3] L. C Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in *Proc. IEEE Symp. on VLSI Technology Dig. of Tech. Papers*. pp. 128-129, June 2005.
- [4] B. H. Calhoun, A. Chandrakasan, "A 256kb Sub-threshold SRAM in 65nm CMOS," in *Tech. Dig., ISSCC 2006, San Francisco, CA*, Feb. 6-9, 2004, pp. 2592-2601.
- [5] S. Zafar, "Statistical mechanics based model for negative bias temperature instability induced degradation," *J. Appl. Phys.*, vol. 97, pp. 103709-103709-9, May 2005.
- [6] H. Yamauchi, "A Discussion on SRAM Circuit Design Trend in Deeper Nanometer-Scale Technologies," *IEEE Trans. Very Large Scale Integr. Syst.* vol. 18, no. 5, pp. 763-774, May 2010.
- [7] Y. C Cao, (2008, Sep 30) "A new set of predictive technology model for high performance applications, incorporating high- k /metal gate and stress effect," [Online]. Available: <http://www.eas.asu.edu/~ptm/>
- [8] R. Vattikonda, W. Wang, Y. K. Cao, "Modeling and minimization of PMOS NBTI effect for robust nanometer design," *Design Automation Conference, 2006 43rd ACM/IEEE*, vol., no., pp. 1047-105.
- [9] S. K. Krishnappa, H. Singh, H. Mahmoodi, "Incorporating Effects of Process, Voltage, and Temperature Variation in BTI Model for Circuit Design," in *Proc. IEEE Latin American Symp. on Circuits and Systems*, pp. 236-239, Feb. 2010.
- [10] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," *Rep. on Prog. Phys.*, vol 69, no. 2, pp. 327-396, Feb. 2006.
- [11] S. Mukhopadhyay, H. Mahmoodi, K. Roy, "Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS," *IEEE Trans. Computer-*