Data-Dependant Sense-Amplifier Flip-Flop for Low Power Applications

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ABSTRACT

In this paper, we present a new sense amplifier based flip-flop that exploits input data activity, to achieve reduced power consumption. The internal nodes of the proposed flip-flop are charged/discharged only when the input data changes state. Simulations show that the power consumption of proposed flip-flop is reduced by 20% to 70% compared to standard sense-amplifier flip-flop. An FIR-filter based on the proposed flip-flop, implemented in 45nm ST process, shows more than 42% improvement in power consumption (with 5% delay penalty) compared standard sense-amplifier flip-flops

Keywords:
Low-power, Flip-Flop, FIR filter, Data-Dependant Flip-Flop

1. INTRODUCTION

Ubiquitous elements of today's CMOS circuits are flip-flops (FF) which make up a major portion of the synchronous circuits. As a result, the structure of FF used in circuits has a large impact on the system power consumption. Moreover, the type of FF used determines the amount of clock load, which directly affects dynamic power consumption P_{DYN} of a circuit. Thus, it is prudent to come up with techniques to reduce the power consumption of FFs to reduce the overall system power.

Techniques to lower unnecessary internal node switching can be used to reduce the total power consumption, particularly for applications with lesser-input activities. It can be noted that the signal activity can be low in certain input bits (most significant bits, MSBs) of signal processing applications such as in image processing and video processing [1,2]. Unfortunately, conventional FFs do not take advantage of such low input activity and the power consumption due to such FFs can be large. Conditional-capturing flip-flop, presented in [3, 4], achieves improvement in power consumption for lower activities of inputs. However, the technique uses skewed inverters and extra circuitry causing significant area overhead. We propose a new Sense Amplifier FF (SAFF) in which the switching of the internal nodes is dependent on switching activity of the input data (Data-Dependent SAFF (DD-SAFF)). Hence, unnecessary transitions are eliminated during clock transitions when input data is unchanged. We show that the proposed FF has much lower power consumption (40%) compared to SAFF. However, the power savings with the proposed design comes at a cost of minor degradation (5%) in setup time and Clk-Q delay. By applying clock-gating, we modify DD-SAFF to further improve power consumption. We use clock gating to reduce the power consumption when flip-flop is in the idle mode (inputs are not changing). We applied the modified FF's to the design of counters to achieve improved power savings. To show the efficacy of the proposed DD-SAFF, we used it in several applications. We first implement a counter where the most significant bits (MSBs) are implemented using DD-SAFF, since they have lower switching activity compared to the least significant bits (LSBs). In addition, we applied the proposed FF to one of the most widely used DSP applications, an FIR filter in which FFs play a major role in total power consumption of the circuit.. Results show large improvement (25.7%-42%) compared to using conventional sense-amplifier based flip-flops.

The rest of the paper is organized as follows: in section 2 we discuss the operation of sense-amplifier flip-flop and present the proposed design. Section 3 present the results for DD-SAFF compared to SAFF [5], C^2MOS, and Transmission-gate flip-flops [6-7]. Section 4 shows the applications of proposed DD-SAFF in counters and FIR filter. We draw the conclusions in section 5.

2. SAFF-BASED DESIGN

Several low-power flip-flop architectures have been proposed in literature to decrease the power consumption of a system [5]. In this paper we focus on a sense-amplifier flip-flop (SAFF) that has lower power consumption compared to other conventional flip-flops. Moreover, it is suitable for dual-rail data-paths [8]. Easier integration of logic circuitry with flip-flops and reduced swing of the clock pulses are other advantages of this circuit [9]. SAFF incorporates a precharged sense amplifier in the first stage to generate a negative pulse, and a Set-Reset (SR) latch in the second stage to capture the pulse and hold the results [10, 11]. Since our proposed design is based on SAFF, let us first consider the operation of sense-amplifier flip-flop in more detail.

2.1. Sense-Amplifier Flip-Flop

The schematic of sense-amplifier flip-flop is shown in Fig.1. The circuit works as follows: when the clock is in precharge mode, the master stage nodes (S and R) are both charged to V_{DD} using two PMOS transistors (MP1 and MP2). When the rising edge of the clock arrives, S or R is discharged to ground depending on the value of input (D). In the case when D is high, three stacked NMOS transistors discharge node S to ground that causes output (Q) to charge to "1". Due to the cross-coupled inverters, R remains

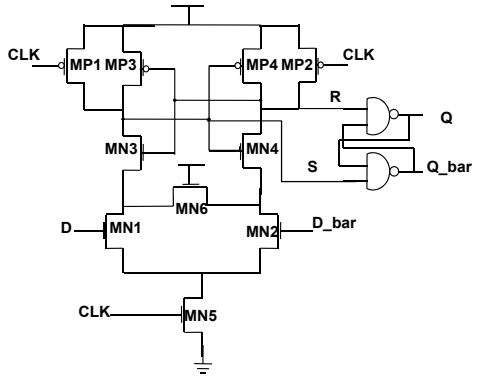

Fig.1. Sense-Amplifier Flip-Flop

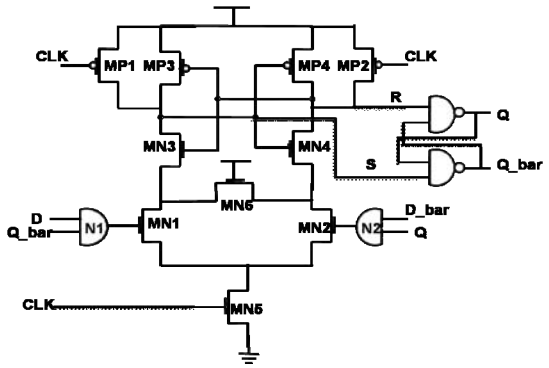

Fig.2. Data-Dependant FF (DD-SAFF)

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high. Note that SAFF comes with delay penalty. This is due to two reasons: the use of three stacked NMOS transistors and the low speed of the static output latch. In terms of power, SAFF outperforms its counterparts due to stacking effect and minimum sized design. However, it consumes unnecessary power even when the inputs do not change -- major internal nodes are precharged continuously when the clock is low. For instance let us consider a scenario in which D remains constant (e.g. at "1") for long period of time. In this case, S and R hold "0" and "1", respectively. When clock is low, internal nodes are precharged to V_{DD}. Thereafter, on rising edge of clock, S is discharged to ground. Consequently, internal nodes of SAFF charge/discharge, regardless of the input condition. Hence, the total power consumption of SAFF can be significantly reduced by avoiding such redundant internal switching.

2.2. Data-Dependant Sense-Amplifier Flip-Flop

Fig.2 shows how the proposed circuit utilizes data-dependency to lower power consumption. We have added two AND gates (N1 and N2) whose inputs are D and Q_bar (D_bar and Q for N2). The purpose of the AND gate is to avoid MN1 and MN2 from discharging the nodes whenever the new data and previous data are the same. The flip-flop works as follows: When clock is low, the internal nodes (S and R) are precharged to V_{DD} through precharge transistors. During the evaluation phase (rising edge of the clock), MN5 is turned ON. Based on the values of Q and Q_bar, the status of MN1 and MN2 are determined. Let us consider a scenario by assuming that the previous value for Q is "0". As a result, output value of gate N2 will be "0". MN2 is turned OFF and MN1 status is dependent on D. If D is "1", MN1 is turned ON. Therefore, the evaluation is done through MN3, MN1, and MN5. Accordingly, S is discharged to ground and Q is changed to "1". Though, if D is "0" (i.e. same as previous state of Q), both MN1 and MN2 are turned OFF and the S and the R values are unchanged. Consideration of data-dependence significantly reduces power consumption of DD-SAFF.

Conversely, when the prior value for Q is "1", MN1 is OFF and MN2 status is determined by input D. In the case that D is "1" (i.e. same as the previous state of Q), both MN1 and MN2 are turned OFF and the internal nodes (S and R) of the FF do not discharge. In case D is low, discharging of node R to ground is through MN4, MN2, and MN5. Consequently, for lower activity inputs, assuming D remains at "1" for a long period of time, nodes S and R remain unchanged at "1". Avoiding continuous charge/discharge during the evaluation phase, leads to significant reduction in power dissipation for applications where input data remains unchanged for long periods of time.

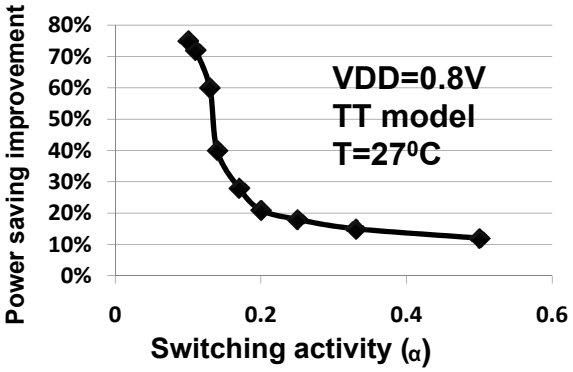


Fig.3. Power consumption improvement for DD-SAFF

Table.1. Power and delay for different topologies (VDD=0.8V, =1/3, Fan_out=4)

Topology	$T_{C\text{-}Q}$(ps)	Power(μW)	PDP (fJ)
C²MOS	37	3.1	114.7
SAFF	53	1.93	102.29
TGFF	50	1.097	54.85
DD-SAFF	53	1.19	63.07

Table.2. Energy saving percentage for 8-bit Counter compared to using conventional SAFF (VDD=0.8V)

Counter	8	16	32	64
power saving %	17.6%	28.4%	37.3%	47.1%

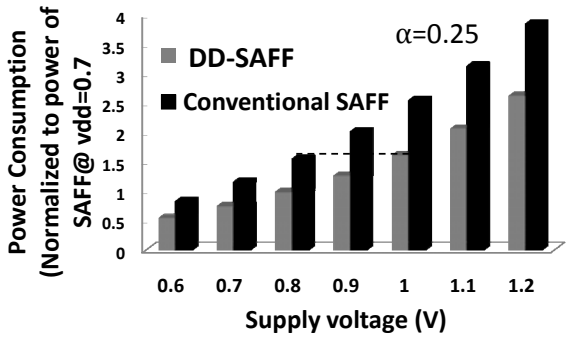


Fig.4. Power consumption for different supply voltages

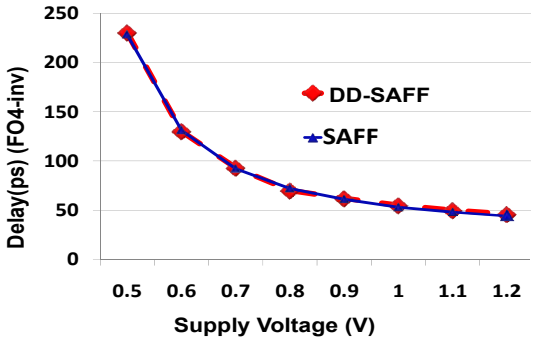


Fig.5. $T_{CLK\text{-}Q}$ delay for SAFF and DD-SAFF

3. SIMULATION RESULTS

To assess the performance of the proposed FF, we compared DD-SAFF with conventional SAFF in terms of power and delay. The power savings in DD-SAFF compared to conventional SAFF is strongly dependant on the input data activity. For different values of **α** (defined as $Tclk/T_{Data}$), it is observed that lower values of α leads to larger power savings (α=0.2 results in 2 times less power compared to SAFF). The worst case in terms of power consumption for DD-SAFF operation is when the clock and data frequency have the same activity (α=1). In this case, the power consumption for DD-SAFF deteriorates by 36% compared to a conventional SAFF (*f*=1GHZ, V_{DD}=0.8V). This is due to the extra AND gates used in DD-SAFF. Thus, DD-SAFF should be used judiciously in applications where the input data activity is low. Fig.3 illustrates the power savings (iso-delay) obtained by the proposed FF compared to conventional SAFF for different switching activities at V_{DD}=0.8V. As it` can be observed for lower α, power savings is significant (e.g. for α=0.1, around 70% improvement in power consumption).

Fig.4 illustrates the results for total power consumption of the data-dependant sense amplifier flip-flop (DD-SAFF) compared to conventional SAFF. To compare power consumption, circuits are simulated at different supply voltages. As shown, the power consumption of a DD-SAFF at V_{DD}=1V is approximately equal to that for SAFF at V_{DD}=0.8V. DD-SAFF is associated with some delay penalty as mentioned earlier.

DD-SAFF shows 5% delay degradation compared to conventional SAFF. However, by upsizing the evaluation NMOS transistors in DD-SAFF, delay degradation can be compensated, albeit at the cost of higher power consumption. Fig.5, illustrates the simulation results for delay of DD-SAFF compared to SAFF from V_{DD}=0.5V to V_{DD}=1.2V.

We have also compared the performance of proposed DD-SAFF with other energy efficient FF architectures and we have chosen power-delay product as the comparison metric. For low power applications, transmission-gate flip-flop (TGFF) has been proposed in [6-7]. On the other hand, C^2MOS flip-flop

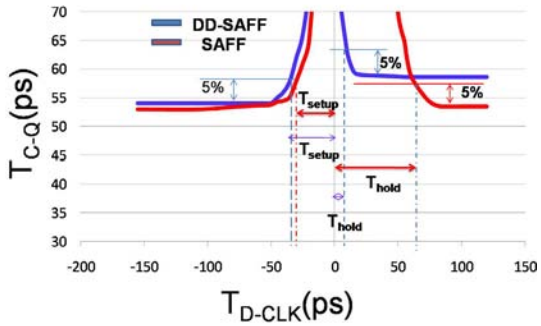


Fig.6. Setup and hold time for SAFF and DD-SAFF

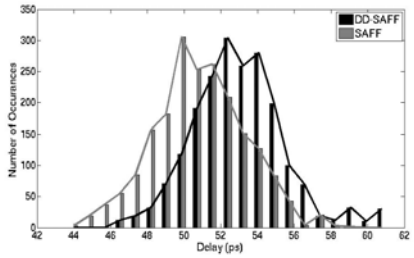
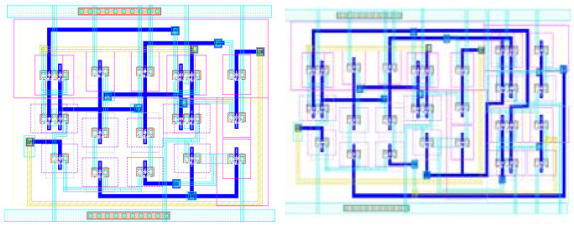


Fig.7. Monte-Carlo simulation for delay comparison

is a good choice for high-speed applications. All the three architectures have been simulated under iso-voltage (V_{DD}=0.8V) and iso-frequency (f=1GHz) conditions. Table 1 summarizes the performance results of our comparison study. As shown, the PDP of DD-SAFF is 38% and 44.6% better compared to conventional SAFF and C^2MOS FFs, respectively. Compared to the TGFF, the PDP results are comparable. However, TGFF suffers from poor data-to-output latency due to positive setup time. Moreover, it also requires two clock phases.

Another metric that can be used to benchmark FF's is the setup/hold timing values. As shown in Fig. 6, 5% increase in T_{C-Q} delay is chosen as the reference point to measure the setup and hold time [5, 12] in our



(a) (b)

Fig.8. Layout of (a) SAFF (b) DDSAFF

calculations. Although, setup time increases from 32ps to 35ps for DD-SAFF, hold time improves considerably from 60ps to 10ps.

In scaled CMOS technologies, the impact of process variations on the circuit performance can be substantial. Hence, we performed Monte-Carlo analysis (2000 trials) for both DD-SAFF and SAFF. It can be observed from Fig. 7 that for the DD-SAFF, standard deviation and mean of delay

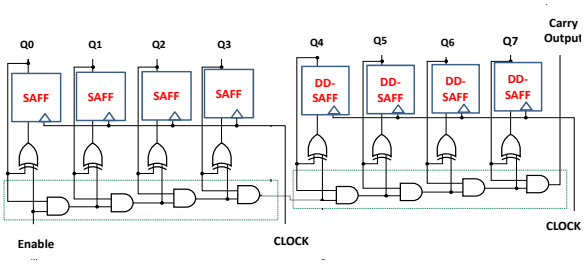


Fig.9. 8-bit counter

variation are 6.3ps and 52.9ps, respectively while for the SAFF are 6ps and 50.9ps. Thus, DD-SAFF has similar σ/μ compared to SAFF. In terms of area, our DD-SAFF design shows 25% area overhead compared to conventional SAFF. Fig.8 shows the layout of DD-SAFF and SAFF design.

We showed simulation results for the DD-SAFF compared to its counterparts in terms of delay, power, PDP, and setup/hold timing values. Our design showed significant improvement in power (as high as 70% for α=0.125). Furthermore, it gives more than 38% and 45% improvement in PDP compared to conventional SAFF and C^2MOS-FF, respectively.

4. APPLICATIONS

In this section, we utilize the DD-SAFF and PGDD-FF in different applications such as counters and FIR filter.

4.1. DD-Counter design

To prove the efficacy of the DD-SAFF design, we employed DD-SAFF in the implementation of an 8-bit synchronous counter, the topology of which is shown in Fig.9. Counters are suitable choices for demonstrating the application of the DD-SAFF, due to lower input activity in MSBs of the counter [13]. The operation of synchronous counter is as follows: new data values are evaluated every clock cycle and captured by related flip-flops. The switching activity of each bit in the counter is decreased by half compared to the preceding bit. Thus, in each clock cycle unnecessary transitions occur, especially for MSBs. Although for α=1, power consumption of DD-SAFF degrades by 36% (compared to conventional SAFF) but for lower input activity, power improves significantly. As a result, conventional SAFF can be used for sections of logic with α close to1, while for α<0.5 DD-SAFF can be used. Thus, for our implementation, conventional SAFF is used for LSBs and we use DD-SAFF for MSBs. As it is illustrated in Fig.9, for the 8-bit counter, four LSB bits are implemented using conventional SAFF while four MSB bits are implemented using DD-SAFF. Our simulation results indicate that the improvement in power is close to 17%. For larger counters (e.g. 16 bits, 32bits, 64 bits), the power consumption is reduced even further since more bits have lower data activity. The performance results for different counters are presented in Table.2

4.2. FIR Filter Design

Apart from counters, the proposed DD-SAFF has the potential for reducing the power consumption of popular DSP applications, such as FIR filters. Specifically, we obtained a synthesized Verilog netlist of a multiplier-less 8-bit FIR filter [14, 15] using Synopsys design compiler [16] and 45nm STM libs. Then we imported the netlist in Cadence and replaced the conventional flip-flops with the proposed FFs. Using HSPICE we have simulated the FIR filter and results are shown in Table 4. It can be observed that using our proposed FF, the power saving is 42.4% compared to conventional SAFF based FIR. On the other hand, compared to low power ST FF, DD-SAFF shows the power improvement of 25.7%. We believe that the proposed FF can be utilized to reduce power in a wide range of DSP systems.

In the following sub-section, a modified DD-SAFF, pulse-generator data-dependant flip-flop, is presented. It comes at the cost of area and power compared to DD-SAFF. However, when used in circuits like counters, where effective clock-gating can be used, considerable improvement in power dissipation can be achieved.

4.3. Pulse-Generator Data Dependant Flip-Flop

DD-SAFF can be modified to include clock-gating during idle periods when the input data is not changing. For DD-SAFF, if input data changes after evaluation, when clock is high, there is a contention between discharging path and the cross-coupled inverters to keep the data on the storage nodes. Using pulse generator data dependant flip-flop (PGDD-FF),

Table.3. Power saving for different counters (LSBs are implemented using conventional SAFF, @ VDD=0.8V)

X(-BIT Counter)	8	16	32
PGDD-FF power(μW)	1.94	2.56	3.25
SAFF power(μW)	2.63	4.297	7.674
P-SAFF	2.13	2.85	4.32
Power Improvement (PGDD-FF)	26.2%	40.4%	57.6%
Power Improvement (P-SAFF)	19.3%	33.6%	43.5%

Table.4. Power comparison of FIR-Filter

Flip-Flop type	POWER
SAFF	1.34mW
DD-SAFF	771 μW
ST-standard FF	1.0385mW

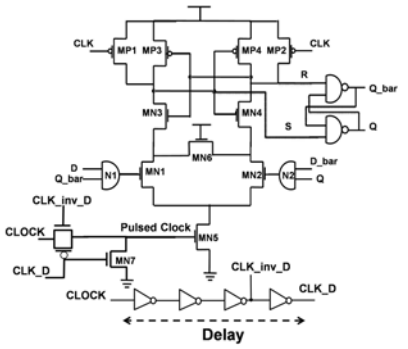


Fig.10. PGDD-FF topology

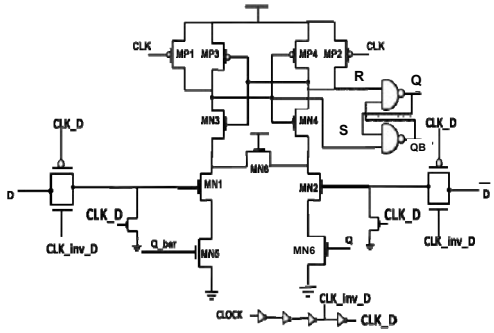


Fig.11. DD-SAFF using pulse-generator technique (P-DDFF)

the evaluation time is shortened resulting lower contention between cross-coupled inverters and the evaluation NMOS network. As shown in Fig.10, a narrow pulse is generated and applied to MN5 instead of applying the main clock. On rising edge of clock, the transmission gate of the pulse generator is ON. Then the output node (Pulsed_Clock) goes high. After a delay equal to $4\tau_{inv}$, (τ_{inv} is defined as delay of an inverter) CLK_D becomes high, the NMOS transistor turns ON and discharges the Pulsed_Clock node to ground. For the rest of clock period, Pulsed_Clock node remains at "0". As a result, evaluation occurs only for a time period of $4\tau_{inv}$ after the rising edge of clock. Though PGDD-FF consumes more power than DD-SAFF (as a single flip-flop in isolation) due to extra circuitry for pulse generation, but it yields significant improvement in power for various applications such as counters. For counter designs the pulse generation circuitry is shared between adjacent flip-flops and it shows less degradation in power due to added pulse generation circuitry.

Fig. 11 shows another SAFF using the pulse generation technique referred as pulsed-SAFF (P-SAFF). P-SAFF works as follows: when the output (Q) is holding "1", MN5 and MN6 are OFF and ON, respectively. In this case, at the primary time of evaluation ($4\tau_{inv}$), if the input data is "1", no discharging occurs at both storage nodes. But if D is "0", node R is discharge through MN2 and MN6. This avoids unnecessary transitions on the internal storage nodes when the input value (D) is unchanged. Pulse-generation technique can be used in applications in which the clocking circuitry is shared between adjacent flip-flops that. Note that PGDD-FF incurs 31% delay degradation compared to conventional SAFF.

In order to further improve power savings, we used PG-DDFF that has much shorter evaluation time. Moreover, the pulsed clock is shared between all adjacent FFs in a counter. Table 3 shows power savings of different counters implemented by PGDD-FF. Moreover, we have also evaluated counters wherein the MSBs use PG-DDFF and LSBs are implemented using conventional SAFF. Simulation results show 40% improvement for a 16-bit counter. As mentioned earlier, for larger counters, we can obtain further improvement in power saving as shown in Table. 3.

5. CONCLUSIONS

A new flip-flop is presented in STM 45nm technology for low power applications. We achieved significant improvement of power consumption for data with lower switching activity at a cost of 5% degradation in delay. Moreover, it gives 6X improvement in hold time with a minor degradation of setup time compared to conventional SAFF. To assess DD-SAFF, different counters were implemented using proposed DD-SAFF and PGDD-FF. Simulation results showed that the power improvement is 20% to 57% depending on the number of bits and input data activity. DD-SAFF was applied to an FIR filter and it showed more than 42% reduction in power consumption with 9% area overhead penalty compared to using SAFF. Consequently, the proposed design can help to reduce power consumption in designs where input data activities are low.

REFERENCES

[1] Lueder, E.; , "Generation of equivalent block parallel digital filters and algorithms by a linear transformation," *Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on* , vol., no., pp.495-498, 3-6 May 1993

[2] Jongsun P.; Woopyo J.; Mahmoodi, H.; Yongtao Wang; Choo, H.; Roy, K.; , "Computation sharing programmable FIR filter for low-power and high-performance applications," *Solid-State Circuits, IEEE Journal of* , vol.39, no.2, pp. 348- 357, Feb. 2004

[3] Bai-Sun K.; Sam-Soo K.; Young-Hyun J.; "Conditional-capture flip-flop for statistical power reduction," *Solid-State Circuits, IEEE Journal of*, vol.36, no.8, pp.1263-1271, Aug 2001

[4] Kong B. S.; Kim S. S.; Jun Y. H.; , "Conditional-capture flip-flop technique for statistical power reduction," *Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000 IEEE International*, vol., no., pp.290-291, 465, 2000

[5] Markovic, D.; Nikolic, B.; Brodersen, R.W.; , "Analysis and design of low-energy flip-flops," Low Power Electronics and Design, International Symposium on, 2001. , vol., no., pp.52-55, 2001

[10] Klass, F.; "*Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic*," in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 108–109, June 1998.

[11] Tschanz, J.; Narendra, S.; Zhanping Chen; Borkar, S.; Sachdev, M.; Vivek De; , "Comparative delay and energy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microprocessors ," *Low Power Electronics and Design, International Symposium on, 2001.* , vol., no., pp.147-152, 2001

[8] Matsui, M.; Hara, H.; Uetani, Y.; Lee-Sup Kim; Nagamatsu, T.; Watanabe, Y.; Chiba, A.; Matsuda, K.; Sakurai, T.; , "*A 200 MHz 13 mm^2 2-D DCT macrocell using sense-amplifying pipeline flip-flop scheme*," *Solid-State Circuits, IEEE Journal of* , vol.29, no.12, pp.1482-1490, Dec 1994

[9] Kawaguchi, H.; Sakurai, T.; "A Reduced Clock-swing Flip-flop (RCSFF) for 63% Clock Power Reduction," *VLSI Circuits, 1997. Digest of Technical Papers., 1997 Symposium on* , vol., no., pp.97-98, 12-14 Jun 1997

[10] Rabaey, J. M.; Chandrakasan, A.; and Nikolic, B.; "Digital Integrated Circuits A design Prespective , " second edition, Prentice Hall, 2002.

[11] Suzuki, Y.; Odagawa, K.; Abe, T.; , "Clocked CMOS calculator circuitry," *Solid-State Circuits, IEEE Journal of*, vol.8, no.6, pp. 462- 469, Dec 1973.

[12] Zyuban, V.; , "Optimization of scannable latches for low energy," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* , vol.11, no.5, pp. 778- 788, Oct. 2003

[13] Xanthopoulos, T.; Chandrakasan, A.P.; , "A low-power IDCT macrocell for MPEG-2 MP@ML exploiting data distribution properties for minimal activity," *Solid-State Circuits, IEEE Journal of* , vol.34, no.5, pp.693-703, May 1999

[14] Jongsun P.; Woopyo J.; Hunsoo C.; Mahmoodi-Meimand, H.; Yongtao W.; Roy, K.; , "High performance and low power FIR filter design based on sharing multiplication," *Low Power Electronics and Design, 2002. ISLPED '02. Proceedings of the 2002 International Symposium on* , vol., no., pp. 295- 300, 2002

[15] Mohapatra, D.; Karakonstantis, G.; and Roy, K.; "Significance Driven Computation: A Voltage-Scalable, Variation-Aware, Quality-Tuning Motion Estimator," *IEEE International Symposium on Low Power Electronics and Design*, 2009.

[16] Synopsys Design Compiler, www.synopsys.com