COMPARISON OF PERFORMANCE PARAMETERS OF SRAM DESIGNS IN 16nm CMOS AND CNTFET TECHNOLOGIES

Anuj Pushkarna, Sajna Raghavan and Hamid Mahmoodi
School of Engineering, San Francisco State University
San Francisco, CA, USA
Email: {anujp, sajju, mahmoodi}@sfsu.edu

Abstract: ***CMOS devices are scaling down to nano ranges resulting in increased process variations and short channel effects which not only affect the reliability of the device but also performance expectations. Carbon Nanotube Field Effect Transistor (CNTFET) is a very promising and superior technology for its applications to circuit design. In this paper we intend to evaluate and compare the performance parameters of a traditional 6T SRAM cell between a predictive 16nm Complementary Metal Oxide Semiconductor (CMOS) technology and CNTFET. The model used to simulate CNT transistor is a tentative model from the researchers of Stanford University, which is not yet practically implemented. Since the dimensions of MOSFETS are reduced aggressively, it is essential to know the potential of what both the technologies have to offer, with their least dimensions available. The SRAM design uses the smallest transistors possible and is also susceptible to reliability issues and process variations, making it an ideal benchmark circuit to compare the two technologies. Our simulations results show that CNTFET based SRAM design is a viable design to choose compared to its CMOS counterpart. The results show that there is a 52.7% increase in SNM of the memory cell. Meanwhile, the cell becomes 5% faster. These results clearly justify that CNTFET is more suitable for circuit design rather than MOSFETs, although both the models under consideration are predictive models. This comparative study would definitely help us choose better technology alternatives in near future.***

I. INTRODUCTION

Over recent years the scaling in CMOS technology has been very aggressive. With ultra-thin dimensions, the technology is facing many critical challenges and reliability issues. Aggressive scaling has resulted in augmented short channel effects, exponential rise in leakage currents, process variations, depressed gate control for transistors and hysterical power densities. Ultrathin CMOS technologies have been predicted and modeled for decades. Recently predicted models of order of 22nm and 16nm in Bulk CMOS have been suggested [6]. Moreover, Carbon nanotubes (CNT) have been identified with highest potential risk-benefit ratio for emerging logic applications such as nano field-effect transistors (nano-FETs). Meanwhile several major technology related questions still need to be addressed. In particular the possibility to obtain ballistic transport over several hundred nanometers at room temperature together with a very large Fermi velocity of around 10 cm/s allows for high-performance on-state characteristics. The CNTFETs also have a significantly smaller off current, which greatly reduces the power consumption in standby states.

Recently, S. Lin, in [2] proposed a SRAM cell de-sign comparison using 32nm CMOS and predicted CNTFET (20nm) based technologies. Characteristics of SRAM were investigated and quantified. These studies predict superior performance of CNTFET based SRAM when compared to conventional Si based MOSFET on the basis of Access time, Static Noise margin (SNM) [3] and Leakage power. The study lacked the comparison of models based on Temperature, which is one of the very critical and dominant environmental factors on performance. Very recently predicted model of 16nm High K metal gate [6] has substantially increased the choice of device models for circuit designing. It is essential to know the potential of what both the technologies have to offer, with their least dimensions available, i.e. for CMOS of 16nm and CNTFET model of 10nm. In our research we use the predicted model for CNTFET, proposed by re-searchers from Stanford University [1], which gave us the opportunity to use minimum channel length of CNTFET as 10nm.

The Static Random Access Memory (SRAM) is an ideal benchmark circuit to compare the two technologies. We use a traditional 6T SRAM cell structure to compare the two highlighted technologies, because the SRAM design is sensitive to transistor density (using smallest transistors possible) and reliability issues. We have used Hspice simulation to analyze and report the results of SRAM cell using each model.

The paper is organized as follows. Section II gives a short description about the CNTFET based model that is developed by the researchers from Stanford University [1]. Section III talks about the current-voltage (IV) characteristics of the CNTFET under temperature variation and comparison with CMOS. This section reflects some physical insight behind the CNTFET model that we have used. Section III describes the traditional 6T SRAM structure. This also underlines some important design constraints and parameters that were essential for the re-search and the results. Section V, and VI show our simulation results and the conclusion of our research.

II. CARBON NANOTUBE FIELD EFFECT TRAN-SISTORS DEVICE MODEL

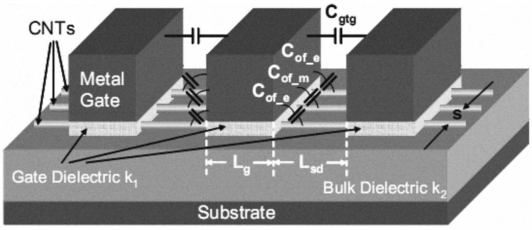

Figure 1: 3-D Structure of CNTFET [1]

The Figure 1 shows a 3-D device structure of Carbon Nanotube Field Effect Transistor (CNTFET) with multiple channels, high K metal gate and parasitic gate capacitances. There are three transistors fabricated along one Carbon Nano tube. As described in the Introduction, we use a circuit-compatible compact model for the intrinsic channel region of the MOSFET like single walled carbon nanotube field effect transistor (CNTFETs). This model can be used for wide range of diameters and other structural variables. In the model itself, the global device parameters of the transistor have been kept constant and were suggested not to be altered. The model has two variants:

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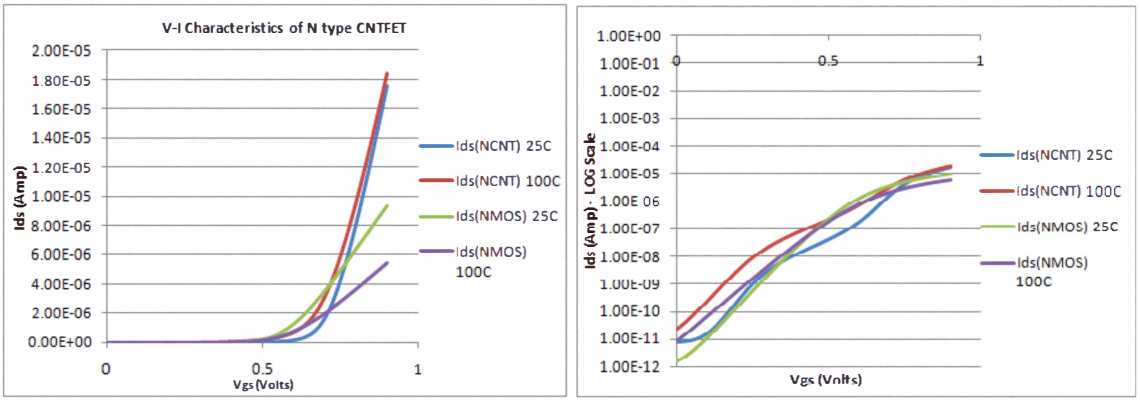

Figure 2: Ids- Vgs Characteristics of N type CNTFET in linear and Log scale. W=18nm, L=16nm for CMOS and Number of tubes = 2 for CNTFET

1. Standard model
2. Uniform model

Both the models allow multiple carbon nanotube under the same gate, the only difference being the way it treats the charge screening effects. In the standard model the charge screening effects between the multiple nanotubes; in the same device are modeled, where as in uniform model the charge screening effects are considered uniform. In our simulation we used the standard model, as it is the most accurate and the fastest when compared to the uniform model [1].

Table 1: Device parameters and process assumptions for simulations (CNTFET Model)

Variable Parameters	
Source/Drain Doping Level	0.59 eV - 0.75 eV (0.7% - 1.3%) Uniformly distributed*
CNT Diameter	1.2 nm - 1.8 nm Uniformly distributed*
Probability of a CNT to be Metallic	8% - 32%
Fixed Parameters	
Oxide Thickness (T_{ox})	4 nm
Gate Dielectric (Dielectric Constant:K_{ox})	HfO_2 (16)
CNT Pitch	4 nm
Power Supply	0.9V
Mean Free Path: Intrinsic CNT	200 nm
Mean Free Path: Doped CNT	15 nm
Gate/Source/Drain Length (CNT)	32 nm
Work Function: contact (Φ_M)	4.5 eV
Work Function: CNT (Φ_{CNT})	4.5 eV
Interconnect Capacitance	0.22 fF/μm

The model was designed for unipolar, MOSFET-like CNFET devices. It has a minimum channel length of 10 nm, but this model does not account for the various complex quantum mechanics which portray the sub-10nm regime. More than one CNT per device can be used and the screening effect by the parallel channels is also incorporated in to the device model. The Schottky barrier effect modeled requires that the doping level in the doped source and drain region be above the first conduction band of the carbon nanotube.

The precision of the Stanford model can be explained by the several non-idealities assimilated such as scattering, effects of the doped source/drain extension region, Schottky barrier resistance and inter-CNT charge screening effects. This model incorporates the quantum confinement on both the circumferential and axial directions, the acoustical/optical phonon scattering in the channel region, the screening effect by the parallel CNTs for CNFET with multiple CNTs and the intrinsic ac behavior which is given by a dynamic gate capacitance network. In MOSFET-like CNFET device the intrinsic semiconducting nanotube under the gate acts as the channel region. The heavily doped nanotube regions of the CNFET act as both source/drain extension region and the local interconnect between two adjacent devices. A high k dielectric is used as the gate oxide, to provide better gate control. As the gate bias is applied, the barrier height is modulated and delivers more on current. The quasi-1D device structure gives better gate electrostatics control over the gate region. Increasing the number of CNTs per device is the most effective way to improve the on current. The model utilizes a semiconducting nanotube, with a chirality vector (19, 0).

III. CNTFET CHARACTERISTICS

Based on Section II, it is important to know the characteristics of a single CNT based transistor. The basic characteristics in terms of the Current and Voltage across a single transistor can be studied in details from references [1], [2]. In our research, we specifically concentrate on the IV characteristics of CNTFET considering the temperature variations. Temperature definitely plays an important role in performance of both types of transistors considered. For a short channel Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) dependency of drain current on temperature primarily originates from the mobility and the threshold voltage. As temperature increases, the threshold voltage and career mobility both decrease and the net effect is that the drain current decreases.

The Figure 2 shows the I-V characteristics (Ids vs. Vgs) of a single N type CNTFET. In the plot we have com-pared the characteristics of an N type MOSFET (16nm channel length) and its CNTFET counterpart (10nm channel length). The main intent of the graph is to reflect the change in characteristics when temperature is changed from 25^{O}C to 100^{O}C. The gate voltage is applied by sweeping it from 0V to 0.9V (which signify the 'OFF' and 'ON' states). The part 'b' of the Figure 2 is the equivalent of part 'a' with current plotted in 'Log' scale. This would help us to understand the OFF state of the transistor, to reflect the leakage characteristics of the transistor. We have used a NMOSFET with W=18nm & L=16nm, whereas the N type CNTFET is used with 2 tubes in its channel. It is essential to compare these two transistor sizes, as the same dimensions are used for the access transistors of the SRAM cell. It is worthwhile to note that the 'ON' current at 100^{O}C in NCNFET is greater than 25^{O}C operation. However in case of NMOS, it is opposite. The 'ON' current is significantly less at 100^{O}C than 25^{O}C. This opposite temperature dependence is described below. The Stanford CNFET Model accounts for three types of scattering mechanisms in the intrinsic channel region:

1. Acoustic phonon scattering
2. Optical phonon scattering
3. Elastic scattering.

When the device is in the on state, the mean free path (MFP) is found to vary linearly with the diameter of the nano tube and inversely with the temperature. And as temperature increase, MFP reduces and sets off the above mentioned scattering mechanisms. Accordingly when there is increase in temperature, MFP reduces and the scattering process increases. The peak mobility varies inversely with the temperature [4], [5]. The overall increase in current in our simulation can be justified by the physical explanation that the mean free path (λ) is in general much longer than the channel length. The MFP of intrinsic CNT modeled for elastic scattering is ~ 200 nm, acoustic scattering ~ 500 nm, and optical phonon scattering ~ 15 nm [1]. The channel length of our simulated model is 10 nm which is very small compared to the MFPs. As such we can presume that there is less scattering process taking inside the intrinsic channel of the nanotube. It is imperative to note that due to less scattering, the mobility degradation of carriers does not take place and leads to the ballistic transport at high temperatures. Our simulation result implies that the scattering has a small effect on the source-drain current for a short channel CNTFET, when the mean free path is long. If a short mean free path were to exist in a CNTFET, the scattering would degrade the on current of CNTFETs terribly than it does for a typical MOSFET, owing to the difference between one dimensional transport in a CNT and two dimensional transports in a MOSFET channel.

Furthermore the CNTFET model we used for the simulation has limited treatment of temperature. This model handles the temperature dependence of phonon and acoustic scattering and Fermi levels. But the model does not account for the temperature dependence of the mean free path of the doped source/drain extension regions. Table 2 also helps us to picture the overall difference in characteristics of both N & P type transistors in 16nm CMOS and 10nm CNTFET. Since the CNT pitch (table 1) is taken to be 4nm in the Stanford's CNTFET model, it is legitimate to have 4-5 tubes in the CNT transistors to match the equivalent 18nm channel width used in N/P MOSFETs.

The results in Table 2 clearly show that for equal width, the CNT transistor delivers more ON current and ON current increases with temperature increase, as opposed to the CMOS transistor which shows less ON current at higher temperature. This explains CNT transistors showing much better Ion/Ioff ratio at high temperature compared to the CMOS counterpart.

Table 2: ON and OFF current readings for both N & P type transistors. W=18n, L=16n for CMOS and No. of tubes = 4 for CNTFET (Pitch of CNT-FET = 4nm).

Device		I_{ON}(Amp)		I_{OFF}(Amp)	
		25°C	100°C	25°C	100°C
N Type	CMOS	9.38µ	5.48µ	1.63p	8.7p
	CNT	34.07µ	35.7µ	8.37p	38.6p
P Type	CMOS	5.614µ	2.816µ	2.409p	8.739p
	CNT	34.07µ	35.74µ	9.598p	39.82p

IV. SRAM DESIGN

Figure 3 shows a traditional 6T SRAM design, where the four transistors M1, M2, M3 and M4 form two cross-coupled inverter and transistors M5 and M6 form access transistors. There are two stable states for the storage cell which denotes '0' and '1'. The access transistors M5 and M6 control access to the storage cell during the read and write operations. The word line WL in the figure controls the access transistors, which in turn decides whether the cell, should be connected to bit line (BL) or bit line bar (BLB). These are used for read and write operations. The selection of the W/L ratios of these transistors is very critical when it comes to the operation of the cell. It affects the reliability of the cell in terms of the read and write operations [7]. We have appropriately selected transistor size ratios for CMOS and CNTFET based SRAM cells. For CMOS based SRAM cell using 16nm predictive High K metal gate model, we used W=18nm, L=16nm for M1, M3, M2 and M4. W=27nm, L=16nm for M1 and M3. This selection was based on the research [7] by which the M1:M5 strength ratio should be approximately 1.5 (M3&M6) and 0.5 for M5:M2 ratio (M6&M4), for a reliable read and write operation.

In the model of CNTFET [1], the diameter of the nano tubes is taken constant, however the ratio of the access transistor compared to the pull up and pull down transistors can be quantified by the number of tubes in the channel [2]. By simulations we reckon that using M2, M4 with 1tube, M1, M3 with 3 tubes and M5, M6 with 2 tubes is most suitable. In the later parts of the paper, we also use these ratios to compare the temperature dependency of a single transistor from the models ([6] and [1]) to justify our results. We assume same bit line capacitance for both designs and ignore cross capacitance effects, as these effects will depend on the interconnect technology.

The need of CNTFET arises from the fact that the 6T SRAM design encounters a lot of problem during its operation in a very low power supply. Therefore, CNTFET can be a good solution, which provides more stability even during aggressive scaling. The performance parameters considered are: Static Noise Margin (SNM), Access Time, Write Margin and the Standby Power. More information of these performance parameters can be gathered from the references [3] and [7].

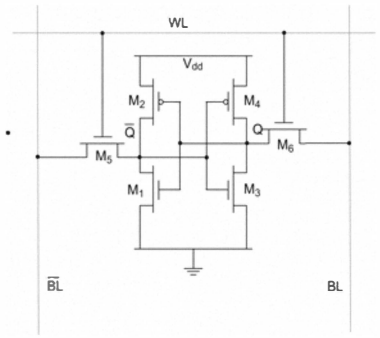

Figure 3: Traditional 6T SRAM cell structure in CMOS technology

V. SIMULATION RESULTS

We used HSPICE to simulate the structure of the SRAM designs implemented by using two different technology models. For CMOS Technology we used 16nm predictive technology model, and for CNTFET we used Stanford University CNTFET Model Package v221. This model has a minimum possible channel length of 10nm. We used this minimum channel length to synthesize the results for the CNFET based SRAM Cell. The transistor sizing for both CMOS and CNTFET based SRAM Cell is done as described earlier in section IV of the paper. On the basis of the CNTFET model, for an equivalent parameter of W (width) we are required to select the number of carbon nano tubes in the

transistor. The more the number of tubes, the larger is the equivalent W of the transistor. Based on the ratios described in section IV, we took the pull down transistor (NMOS) to have 3 tubes, the NMOS access transistor to have 2 tubes and the pull up PMOS transistor to have 1 carbon nanotube. Table 3 shows the results of the simulations done in the two different technologies. The supply voltage is set to be 0.9 Volts. Following are some points when we com-pare the performance parameters of both the designs.

Parameter variation when a 16nm (CMOS) is compared to 10nm (CNTFET) cell:

- SNM increases by 52.7%
- Access Time reduces by 4.5%
- Write Margin reduces by 43%

The resulting figures definitely show that there is a significant improvement in the essential performance of the SRAM Cell when designed with 10nm CNTFET model. It is also essential to observe the temperature dependence of the performance parameters for each design.

Table 3: Simulation Results for 6T SRAM Cell using 16nm CMOS & 10nm CNTFET technology models.

6T Cell for 16nm CMOS of SRAM		
Parameters	25°C	100°C
SNM (Volts)	0.117	0.105
Access Time (ns)	2.483	4.83
Write Margin (V)	0.2715	0.273
Power Standby (pw)	10.65	22.912

6T Cell for 10nm CNTFET of SRAM		
Parameters	25°C	100°C
SNM (Volts)	0.178	0.171
Access Time (ns)	2.389	1.627
Write Margin (V)	0.155	0.18
Power Standby (pw)	76.53	48.5

Variation in performance of CNTFET (10nm) SRAM as temperature increases from 25°C to 100°C is as follows:

- SNM reduces by 4.3%
- Access Time reduces by 31.3%
- Write Margin increases by 16%

Variation in performance of CMOS (16nm) SRAM as temperature increases from 25°C to 100°C is as follows:

- SNM reduces by 10%
- Access Time increases by 94.5%
- Write Margin increases by 8%

By this analysis we can deduce that the CNTFET based SRAM cell would be less susceptible to temperature variation for access time; SNM and more susceptible for the write margin and standby power. However, the main highlight of the analysis is that, when the temperature is increased from 25^{O}C to 100^{O}C, the access time of the CNTFET based SRAM cell reduces by about 31%. On the other hand it increases by 95% in case of CMOS based cell. This can be effectively explained by the opposite temperature dependence of the IV characteristics of an N type CNTFET as explained in Section III. This is primarily because the ON current in case of CNTFET increases at higher temperatures, which is just opposite to the CMOS behavior. Additionally, the logarithmic graph shown in Fig. 2 and the OFF current data shown in Table 2, justify the higher standby power in case of CNTFET SRAM. The results in Table 2 show the IOFF in case of NCNTFET is considerably higher as compared to NMOS transistor, resulting in more standby power for CNTFET SRAM. Eventually, the IOFF in case of both the CNTFET transistor types is high. We know that the write margin of the SRAM cell is sensitive to the strength (current drive) of the pull up transistor, which is a P type transistor in both the designs. From Table 2, we can deduce that the value of the ON current in case of the P type CNTFET is more as compared to its MOS type counterpart. Higher PMOS ON current makes the write action more difficult to happen through the competing combination of the access transistor, M5/M6, and P type transistor, M2/M4. Because of this, we can observe a reduction in write margin of 10nm CNTFET based SRAM cell by 43% compared to its CMOS counterpart. This results in a tradeoff between selections of the technology, as there is reduction in write margin and increase in standby power. These final observations tell us that there are tradeoffs involved when we compare the two technologies. Although the percentage improvement in access time and its improvement on higher temperatures give CNTFET model a lead, the CMOS based design gives much better results for leakage power. However, the improved access time and SNM for CNTFET SRAM can be traded off for reduction of standby power by lowering the supply voltage.

VI. CONCLUSION

Through this paper, we have contemplated the use of MOSFET like CNTFET for the traditional 6T SRAM design. The performance parameters of an SRAM cell were evaluated by using both the models; a CMOS based 16nm predictive model and a CNTFET model having a channel length of 10nm. Our results show a clear superiority of the CNT based SRAM in terms of SNM and access time. Moreover, the CNT based SRAM shows access time reduction with temperature increase which is opposite to the regular CMOS behavior (delay increase with temperature increase). This inverse temperature behavior in CNT is attributed to the physical electron transport mechanism inside the CNT transistor (ballistic transport). Our results show the promise of the CNT technology for future of technology scaling.

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