New SRAM Design Using Body Bias Technique for Ultra Low Power Applications

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Abstract

A new SRAM design is proposed. Body biasing improves the static noise margin (SNM) improved by at least 15% compared to the standard cells. Through using this technique, lowering supply voltage is possible. This SRAM cell is working under 0.3V supply voltage offering a SNM improvement of 22% for the read cycle. Write Margin is not affected due to using body biasing technique. 65nm ST models are used for simulations.
Keywords: SRAM, Static Noise Margin, Low power, 65nm

I. INTRODUCTION

Power reduction techniques are proposed to improve the battery life of applications such as laptop computers, personal digital assistants (PDAs), and portable communication devices. One of the most promising techniques to lower power consumption is supply voltage scaling. By scaling the supply voltage, the dynamic power is reduced quadratically. For wireless sensor network applications, due to lower frequency rate, the supply voltage may be reduced below the threshold voltage. This operation is referred as sub-threshold design that uses the sub-threshold current as drive current to evaluate the inputs[1,2]. Lowering the supply voltage reduces the sub-threshold current, exponentially. Due to the effect of Vth variation on sub-threshold current, working in this region causes more sensitivity to process variations. The effect of process variation, is more important in circuits such as memories and flip-flops, that causing data loss on storage nodes in FFs or memories. Due to minimum size transistors in SRAM memories, the sensitivity to inter-die as well as intra-die process variations is significant. Failure in SRAM such as Read and Write are caused by process variations in ultra low supply voltage applications [3].

For reliable Sub-threshold applications, different SRAM topologies have been proposed. A DTMOS technique is proposed in [3]. While 5T[4], 8T[5], and 10T[6] cells employ single ended reading, 6T and 7T[7] cells utilize differential read operation. 8T and 10T cells use separate read line to read data, so these designs improve Read SNM compared to 6T-SRAM cell. This design uses more area but works at lower supply voltages. Therefore, it decreases the power consumption. DTMOS cell afford more supply voltage scaling to decreases the power consumption for ultra low power applications. In addition, it improves the SNM in hold/read compared to 6T-SRAM cell. This circuit enables the SRAM to work properly with a supply voltage below 135mV for wireless applications. In this paper, as it is shown in Fig.1, a new SRAM cell is proposed to improve the SNM in hold/read mode compared to other proposed SRAM cells. The proposed design, employs more area compared to 6T-SRAM cell but it enables operation down to supply voltages of 100mV so it decreases the dynamic power consumption more and enables more supply voltage scaling for ultra low power applications, such as portable communication devices. For all designs, upsizing is used to work in sub-Vth region, properly. Anyway, upsizing method in sub-Vth has not significant effect on static noise margin (SNM) improvement as much as super-threshold design.

The paper is arranged as follows: Section I describes the proposed SRAM cells in details. Simulation results for proposed circuits are presented in section II including a compare to 10T, 6T, and DTMOS SRAM cells. Section III, is the conclusions.

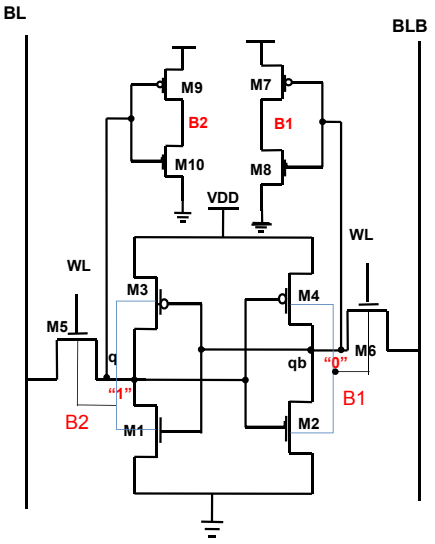

Fig.1. Proposed SRAM cell using Body-Biasing

II. PROPOSED SRAM DESIGN

Fig.2 shows the standard 6T-SRAM cell. In this circuit, storage nodes are specified by X, Y. Suppose that node X stores "0" and node Y stores "1". Due to low supply voltage, the reliability issue is important. As it was discussed earlier, the main leakage source in sub threshold region is sub threshold current. Ion/Ioff ratio in weak inversion is very low. So the effect of off current to flip the data on storage nodes is significant. So, by changing the threshold voltage, due to mismatch or process variations, the SRAM cell characteristics are changed significantly.

The effect of process variation and mismatch on 6T-SRAM cell in read cycle (WL="1") is shown in Fig.3. The effect of temperature on threshold voltage cannot be neglected.

In the proposed circuit, body-biasing technique is used to decrease the process variation effects on the SRAM cell. Fig.1 shows the new SRAM cell using body-biasing technique. Two inverters are added to the 6T-SRAM standard cell to control the bulk voltages of M1-M4 transistors. In this technique, the values of bulk voltage are

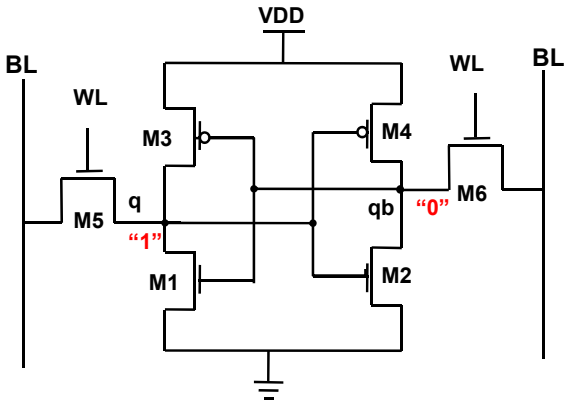

Fig.2. 6T-SRAM standard cell

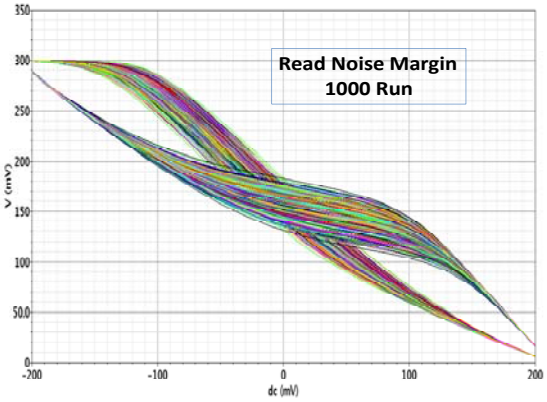

Fig.3.Butterfly curves (Monte Carlo Sim. 1000 Runs)

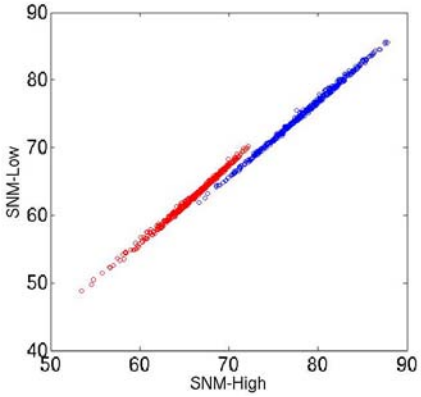

Fig.4. SNM-Low versus SNM high for 500 MC run

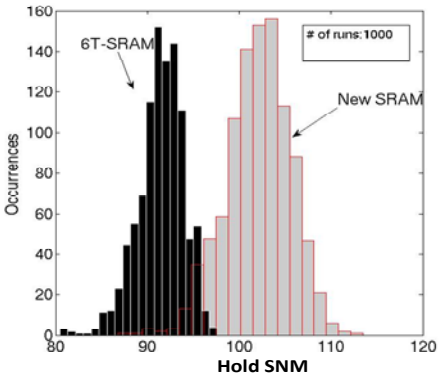

Fig.5.Hold SNM for 6T-SRAM and proposed SRAM

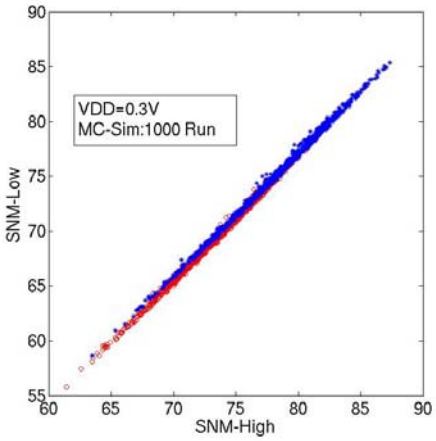

Fig.6.Using pass-transistor biasing for higher Write Margin

dependant to the values stored on the storage nodes. Suppose that "1" and "0" are stored on q and qb nodes, respectively. In this case, B2 and B1 are at "0" and "1" respectively. B2 node is connected to the bulks of M1 and M3. By connecting the bulk of M3 to "0", this helps to hold the q node in "1", so the static noise margin in read and hold is improved. At the same time, B1 is at "1", so it helps to hold the qb node at "0". So, the static noise margin is improved compared to 6T-SRAM standard cell. This improvement in SNM helps to scale supply voltage more. This SRAM cell works in Supply voltages less than 0.15V. Fig.4 shows the Monte-Carlo (MC) simulation for proposed circuit compared to SRAM standard cell. As it is illustrated, the SNM is improved by 15%- 22%. To improve the Read SNM even more, B2 is connected to the bulk of M5 and B1 is connected to the bulk of M6. In this case, the SNM is increased by at least 7% compared to the previous one. Fig.5 shows the MC-simulation in the hold mode for the 6T-SRAM cell and proposed SRAM cell. As it is shown, the Hold SNM is improved more than 30%. For 6T-SRAM cell, upsizing is used to enable it working at VDD=0.3V. If the 6T-SRAM standard cell specified for super-threshold is used, the SNM improvement will be significant. If we use body-biasing technique for pass transistors, SNM is improved around 7-10% compared to SRAM cell in Fig.1. Fig.6, shows the MC-simulations for both topologies illustrating the Read SNM improvement. To see the Write Margin of the proposed the SRAM cell, three possibilities of proposed circuits are shown. The first is the proposed SRAM cell in Fig.1, second and third are connecting bulks of pass NMOS transistors to B1 and B2 and vice versa. Fig.7, shows four topologies that are referred as PB1, PB2, PNB, and 6T-SRAM. While PB1 and PB2 are biased for NMOS transistors, PNB has no body-biasing for NMOS pass transistors. Fig.8, shows the simulation results for Write Margin for different temperature for different topologies in Fig.7. As illustrated, the Write margin is not degraded in PB1 but it is degraded in PB2 and PNB. The Write Margin is improved in PB1 by 4% for TT models. But for SF models, it is increased by more than 300%. For FS, FF, and SS the Write Margin is improved by 3%, 11% and 1% respectively. However, for PNB for TT models, the SNM in write mode is degraded by 15%. By using PB2 circuit, the Read SNM improvement is less than PB1 and PNB. The most improvement in Read SNM is while PB1 circuit is used,

but Write Margin is degraded more. Fig.9, shows the Read SNM of different topologies for TT model in VDD=0.3V. As it can be seen in this special case, the improvement in SNM for any topology is clear. The best design in this case for higher SNM is PNB, but in overall, the PB2 design is the optimal circuit to get the higher Read SNM. To see the effect of supply voltage on Read SNM for the proposed circuits compared to the 6T-SRAM cell, circuits are simulated from VDD=0.5V to VDD=0.2V. Fig.10 shows the Read SNM for PNB design compared to 6T-SRAM (upsized). As can be seen in this special case , the Read SNM improvement is around 20%. Comparing to standard 6T-SRAM cell the improvement is more than 50%. As shown in Fig.10, the largest improvement for Read SNM is for the PNB design compared to other topologies.

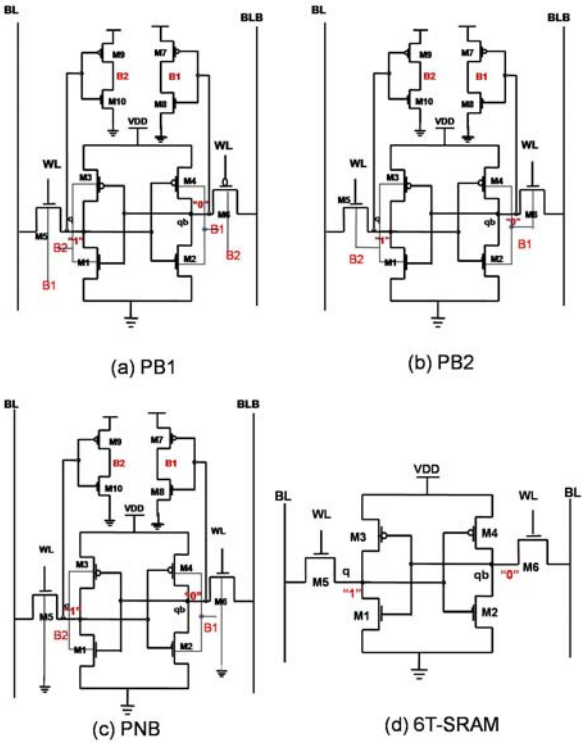

Fig.7. Different SRAM cell topologies

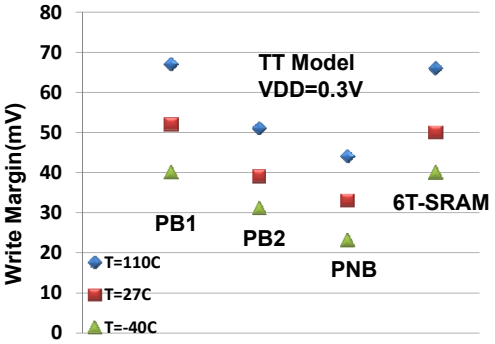

Fig.8. Write Margin for different SRAM topologies

Fig.11, shows the 10T-SRAM cell proposed in [6]. This design, uses single read line and separates the read line from write line. Therefore, it helps the read static noise margin in read and hold mode. However, the design uses VV_{DD} to supply cell in write mode to improve Write Margin. This scheme weakens PMOS transistors during the write mode to increase the Write Margin. However, this circuit fails to work in supply voltages lower than 300mV in write mode. Fig.12 shows the number of failures in read mode for different topologies in different supply voltages. As it can be seen, PB1 has a lower number of failures for read cycle. Therefore, the proposed circuit can work at supply voltages around 0.15V or even 100mV. Another circuit that has been proposed in [1] is illustrated in Fig.13. It is referred as DTMOS SRAM cell, and enables more scaling in supply voltage compared to 10T-SRAM cell to VDD=0.135V.

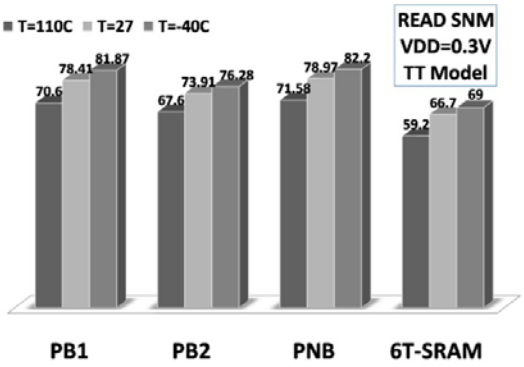

Fig.9. Read SNM for different SRAM topologies

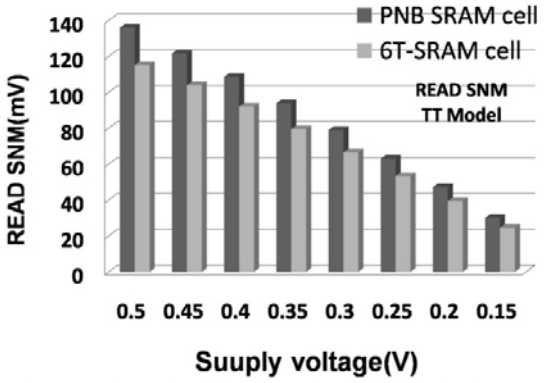

Fig.10. Read SNM for different supply voltages (Upsized 6T-SRAM)

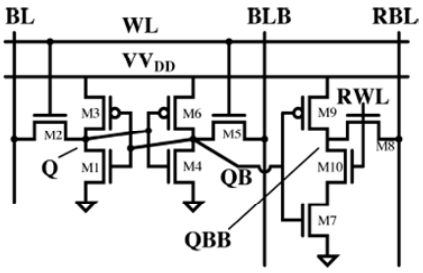

Fig.11. 10T-SRAM cell [6]

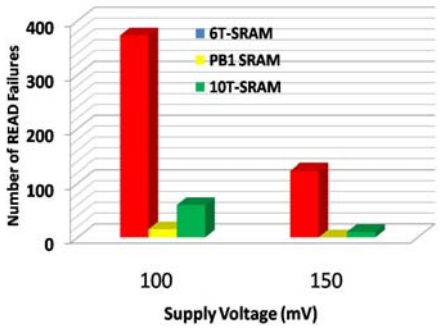

Fig.12. The number of failure in Read SNM

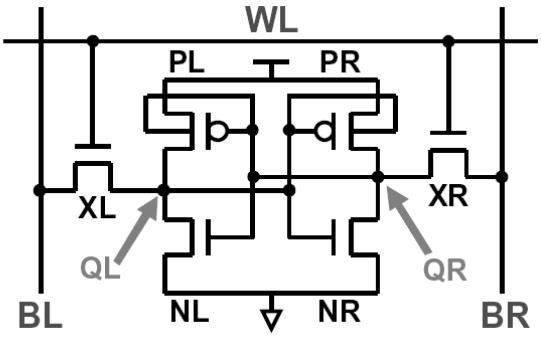

Fig.13. DTMOS-SRAM cell [1]

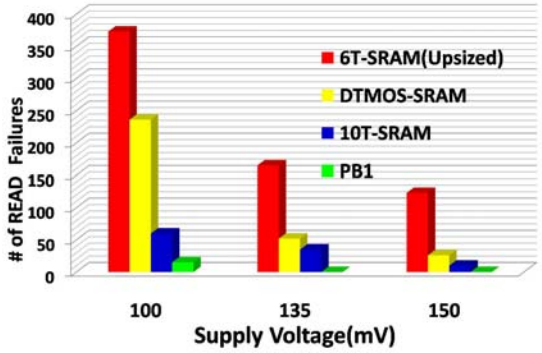

Fig.14. Read failure in different SRAM topologies

Fig.14, shows the proposed circuit works in voltages enough low such as 100mV with a very low failure percent. The PB1-SRAM cell works in VDD=0.1V with less than 10% number of failures in read cycle. By proposing new schemes for write cycle using body-biasing scaling supply voltages in such a very low voltage is possible.

III. CONCLUSIONS

New SRAM topologies based on body biasing technique were proposed. SNM in read/write/hold have been improved compared to other conventional SRAM cells. Using body-biasing technique in SRAM cells increases the area but improves the effect of upsizing on SNM and improves the SNM in read/hold/write modes. The SNM in read and hold mode by employing body-biasing technique is improved significantly and Write Margin is not degraded. The proposed circuits are using larger areas due to using separate N-Well but they can be a choice for ultra low power wireless applications that use lower capacity SRAM's.

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