Evaluation of Power Gating under Transistor Aging Effect Issues in 22nm CMOS Technology

Evaluation under Estimated Temperatures

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Abstract -**Power gating is an effective low-power design technique and is the most widely adopted leakage current reduction solution. In this project, we evaluate the effectiveness of power gating in 22 nm CMOS and analyze the impacts of the Positive/Negative Bias Temperature Instability (PBTI/NBTI) phenomenon on the power gating technique. We also estimate the actual temperatures of power gated circuits and simulate them under different temperatures. The results show that power gating can reduce the effect of PBTI/NBTI, effectively save power, and reduce temperature and delay in hospitable situations while it may not be a good choice in all cases.**

Index Terms – **Power gating; sleep; delay; power; temperature.**

I. INTRODUCTION

Power and reliability, two important metrics, which are intrinsically conflicting to each other, are always of our concern. Compared to traditional solutions to improve reliability or to reduce power, power-gating is a promising technology to overcome this conflict. It is the most widely adopted leakage reducing solution.

A. The Transistor Aging Effect

The transistor aging effect causes the performance of the transistor to degrade over time when it is working at elevated temperature [1]. It includes Positive Biased Temperature Instability (PBTI), which happens on NMOS, and Negative Biased Temperature Instability (NBTI), which happens on PMOS. From the physical point of view, PBTI and NBTI are due to the generation of traps at Si/SiO2 interface in positively biased NMOS and negatively biased PMOS, respectively. They result in progressive increase of the threshold voltages (Vt), which increases the delay and degrades the reliability of the circuit over time.

B. Power-gating Technology

Power gating is a coarse-grain generalization of the MTCMOS technique in which a header and/or footer transistor is inserted on the pull-up and/or pull-down network of a CMOS gate [2]. It is also called sleep transistor (ST). When the circuit is in stand-by mode, the ST turns off so that it reduces the leakage current that flows in the supply-ground path. We will use a footer-based implementation in this work, which is quite popular.

II. EXPERIMENTAL SETUP

A. PTM Models

In this work, we use 22nm High-K metal gate model provided by Predictive Technique Model (PTM) group [3]. We also use their Beta version model to predict NBTI/PBTI, the Vt shifts over time [4]. It includes the dependence of NBTI/PBTI on process and design parameters. For a particular transistor, BTI depends on the stress and recovery timing as shown in Fig 1, in which the signal is the gate voltage of a PMOS. When the Vgs is low (between t1 and t2), the transistor is under stress. β is the stress probability (between 0 and 1); T is the cycle time. βT is the total amount of time when the transistor is under stress. We use the following equations (1) and (2) to calculate Vt shift.

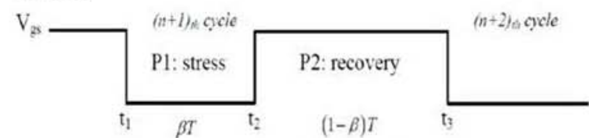

Figure 1. A sample input at the Gate of a PMOS transistor under consideration

$$\Delta V_{th} = K_v \cdot \beta^{0.25} \cdot T^{0.25} \cdot \left[\frac{1-\left(1-\sqrt{\eta(1-\beta)/n}\right)^{2n}}{1-\left(1-\sqrt{\eta(1-\beta)/n}\right)^{2}}\right]^{0.5} + \delta_v \tag{1}$$

$$K_v = A \cdot T_{ox} \cdot \sqrt{C_{ox}(V_{gs}-V_{th})} \cdot \exp\left(\frac{E_{ox}}{E_0}\right) \cdot \left[1-\frac{V_{ds}}{\alpha(V_{gs}-V_{th})}\right] \cdot \exp\left(-\frac{E_a}{kT}\right) \tag{2}$$

In the equations, T is the time; β is the stress probability; tox is effective oxide thickness; Vgs is gate to source voltage. The effects of temperate, voltage, and process on aging are captured via the temperature (T), Vgs, and Vt parameters.

B. Circuits under Study

The original circuit we use in this work is composed of four invertors in series, acting as a buffer, shown in Fig 2. Supply voltage and ground are directly connected to these inverters (no power gating).

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In the power gated circuit, we insert a sleep transistor between the virtual ground and actual ground (Fig. 3). For both original and power gated circuits, we define this 4-inverter structure circuit as one cell. Later when we do the temperature estimation, a parameter "cell size" will be involved. The value of cell size means how many of this 4-invertor structures are in series.

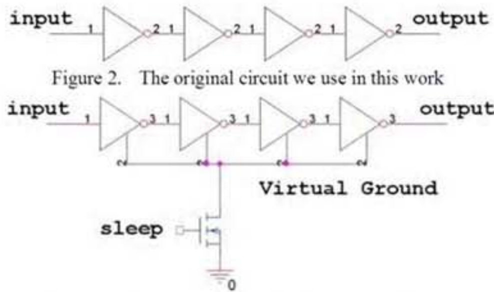

Figure 2. The original circuit we use in this work

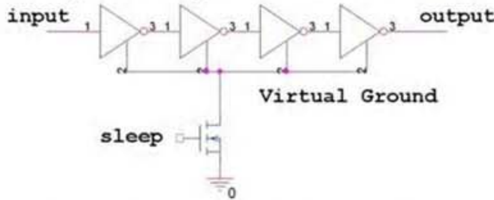

Figure 3. The power gated circuit we use in this work

We use 0.8V supply voltage (Vdd), a square wave input with 1GHz frequency, and a square wave sleep signal with 1MHz frequency. We assume that the input is idle and the sleep signal is low for 70% of the time.

With these assumptions, the stress probability β of all transistors in the original circuit is 0.5 because in both active mode and idle mode, half of the transistors are under stress. In the power gated circuit, when the sleep signal is low (70% of the time), the sleep transistor cuts off the path between the circuit and the ground. The voltage of the virtual ground is charged to around Vdd – Vt [5], where Vt is the threshold voltage of NMOS. After that, we can assume that all transistors in the circuit are not under stress, which makes β to be 0 for 70% of the time. When the circuit is in active mode (30% of the time), β is the same as the original circuit, which is 0.5. Therefore, for transistors in the power gated circuit, $\beta = 0 + 0.3 * 0.5 = 0.15$, and β for the sleep transistor is 0.3. With a much lower β, we expect a less impact of the aging effect on the power gated circuit than the original circuit.

C. Sleep Transistor Sizing

Without aging effects, at the same temperature, adding a sleep transistor will increase the delay. As the size of the sleep transistor goes up, the delay penalty goes down, as shown in Fig 4. Fig 4 is the delay penalty (y-axis) versus the size of the sleep transistor (x-axis). The values of x axis mean how many times the sleep transistor is bigger than the NMOS in the inverters.

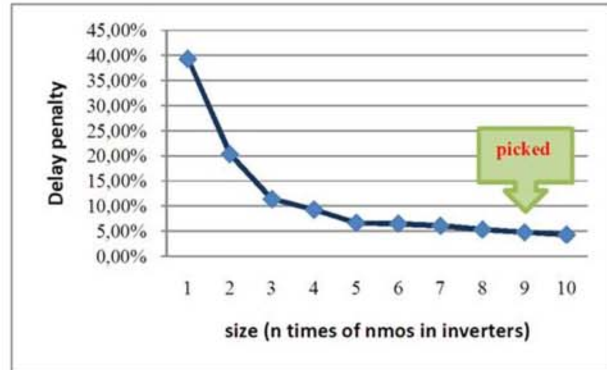

Figure 4. Delay penalty versus the size of the sleep transistor.

In this research, we chose the sleep transistor to be 9 times as big as the NMOS in the inverters so that at 100°C, the increased delay of the power gated circuit is about 4.8% as compared to the delay of the original circuit.

III. Experiments & Results

A. Evaluation at Worst Case Temperature (100°C)

Firstly, let us evaluate the circuits at worst case temperature (100°C). We estimate the aging effects, and find that the Vt shifts in the power gated circuit are less than they are in the original circuit. The difference becomes bigger over time because the stress probability β of the power gated circuit is much less than the original circuit.

When we compare the delay of the two circuits, we find that the power gated circuit always has higher delay within 2 years (Fig 5). The delay penalty goes down from around 5% to 2% (Fig 6). The power gated circuit suffers less from the aging effect, so as time goes up, it takes more and more advantages from the less Vt shift. As a result, the delay penalty of the power gated circuit reduces over time (Fig. 7).

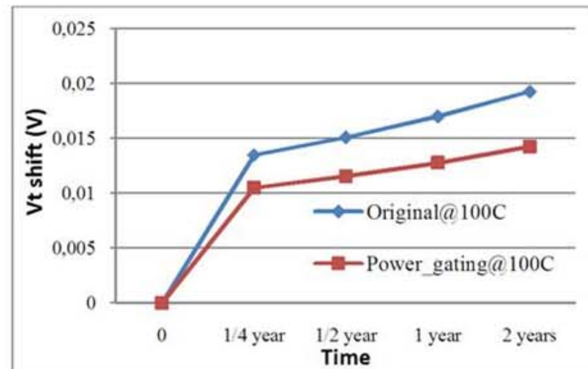

Figure 5. Comparison of the increased threshold voltages

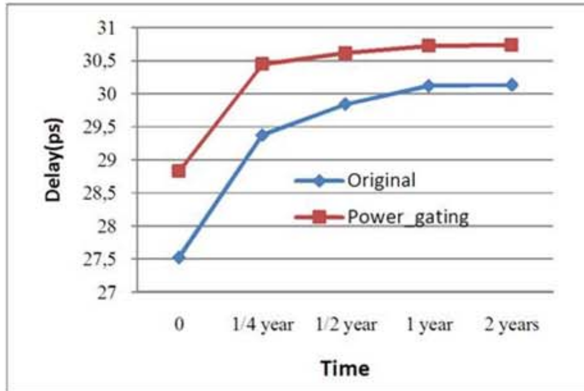

Figure 6. Delay increase of the two circuits over time

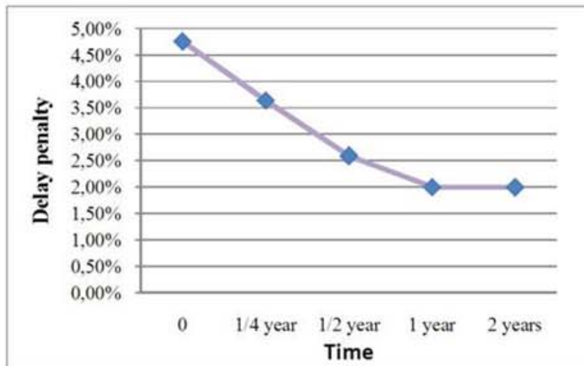

Figure 7. Delay penalty of power gated circuit over time

We can also see that the power gated circuit saves power by reducing the leakage current. The power benefit goes down from 16% to 12.5% over 2 years (Fig. 8). The reason for the reduced power benefit over time is that the original circuit is influenced more by the aging effect (higher Vt increase), which causes higher threshold voltage over time and helps reduce the leakage more.

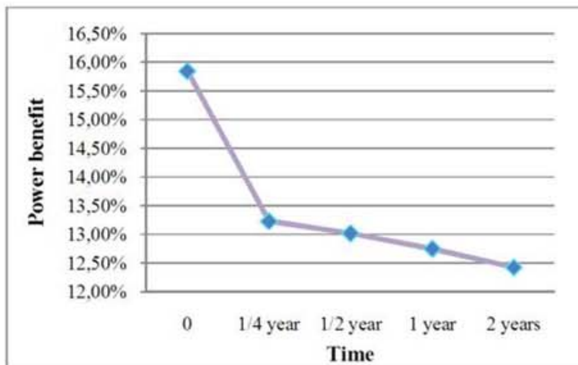

Figure 8. Power benefit

So far, the analysis was done at equal temperatures. However, given that the power gated circuit burns less power, its operating temperature should be lower, causing further less aging. In the next step we will use a temperature estimation methodology to come up with operating temperatures for the two circuits.

B. Evaluation at Estimated Temperatures

1) Temperature estimation

Since the power gated transistor can reduce leakage current and saves power, the power gated circuit is likely to work at a lower temperature than the original circuit. Therefore, we evaluate the two circuits at their estimated temperatures.

We find out a situation where the original circuit reaches 100°C. Then we put the power gated circuit into the same situation and estimate its temperature. We assume ambient temperature is 25°C and the thermal resistance is 50°C /W.

The method we estimate the temperature is shown in Fig 9. In this flow chart, we firstly make assumptions of room temperature, thermal resistance, and cell size (number of 4-inverter chains). Then we find out the average power of the original circuit from simulation with the ambient temperature T1. With the average power, we calculate the new temperature T2 using the following equation:

$$T2 = Ta + C * P * Rs \qquad (3)$$

Where Ta is the ambient temperature; C is the cell size; P is the average power of one cell; Rs is the thermal resistance.

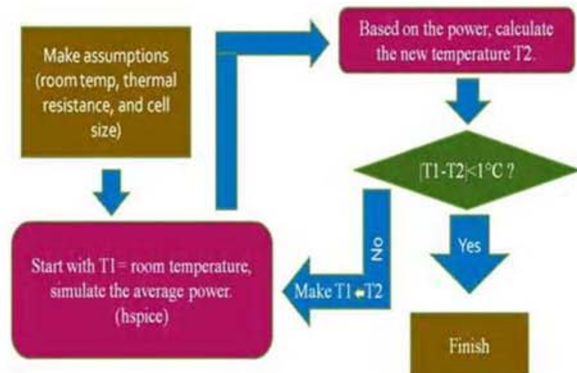

Figure 9. Temperature estimation flow chart

If the difference between T2 and T1 is more than 1°C, we replace T1 with T2 and do the iteration. T1 and T2 will get closer after each iteration and the difference will eventually become less than 1°C. That is the final temperature of the circuit. We play with the cell size and find out that the original circuit will reach 100°C with about 9 million cells while the power gated circuit with 9 million cells will reach 89.1°C, which is about 11°C cooler than the original circuit.

2) Aging effect comparison

We compare the aging effect again at the estimated temperatures for both circuits (Fig 10). The new plot at the bottom is the Vt shift of the power gated circuit at the estimated temperature of 89°C. Working at 89°C, the power gated circuit reduces the impact of the aging effect a little more than it did at 100°C.

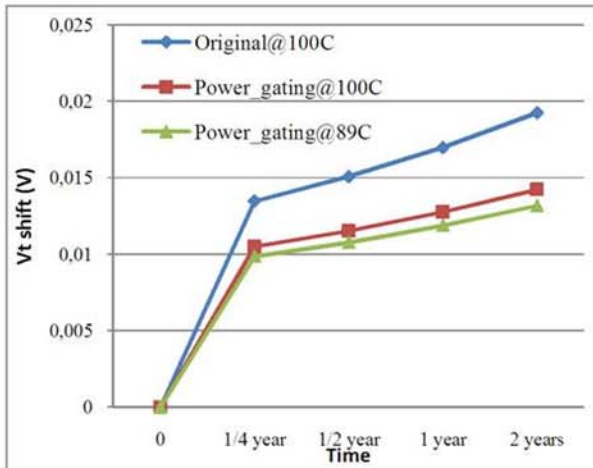

Figure 10. Vt shift comparison

3) Delay and power comparisons at different temperatures

From the simulation, we find out that the power gated circuit has a lower delay than the original circuit (Fig 11), and the benefit is going up over time (Fig 12). The delay of the power gated circuit has a less degradation than before because of the lower Vt shift.

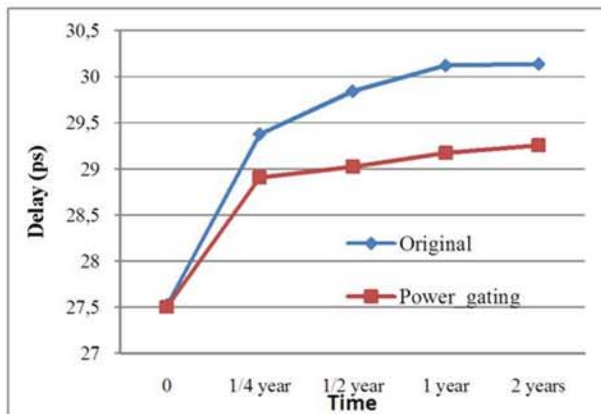

Figure 11. Delay comparison at estimated temperatures

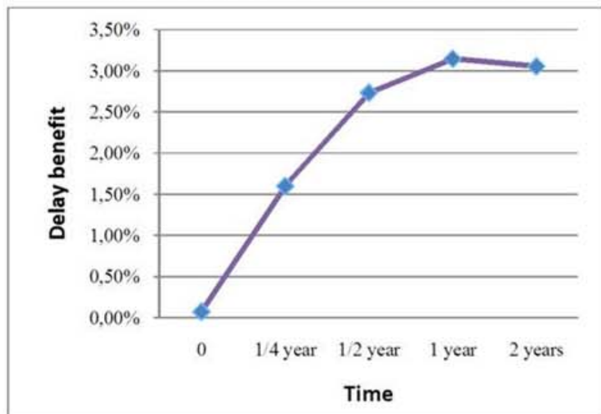

Figure 12. Delay benefit of power gated circuit

Compared to the evaluation at the same temperature before, we see that the delay of the power gated circuit changes from a higher value than the original circuit (at time zero) to lower value than the original circuit over time. The difference of the Vt shift of the power gated circuit is not much between different temperatures (100°C and 89°C), but the result of the delay of these two cases are significant. We conclude that the reduced aging effect contributes to reducing the delay and a lower deviation of the delay over time, but the main reason of the lower delay is the lower temperature for the power gated circuit(11°C cooler in this case).

The power benefit curve (Fig 13) does not change much from the evaluation at the same temperature because the impact of the aging effect changes very little, so does the leakage current which determines the power.

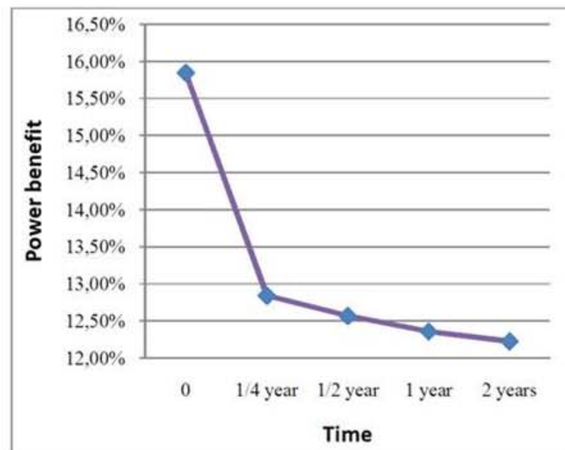

Figure 13. Power benefit at estimated temperatures

C. Analysis of Worst Case Activity Scenario

The main purpose of the power-gating *technology* is to reduce the leakage current when the circuit is in sleep mode so as to save power. It also lowers the stress probability β of the transistors in order to reduce the aging effect. We can imagine that the worst case is the case when the circuit never enters the sleep mode (always active).

In this worst case, the β of the transistors in both circuits are the same (0.5). After the temperature prediction, we find that both circuits almost have the same temperature, and 3.1 million cells will make both circuits reach 100°C.

At 100°C, the power gated circuit now has a higher delay than the original circuit as shown in Fig 14. The delay penalty is going up from 5% to 12% over time (Fig 15). The reason is that now both circuits do not enter sleep mode, not only the power gated circuit does not have the aging effect advantage any more, but the sleep transistor is always under stress and suffers considerably from the aging effect over time as well.

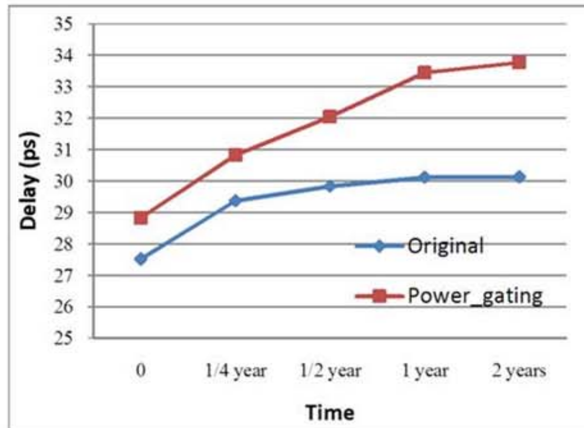

Figure 14. Delay comparison in the worst case

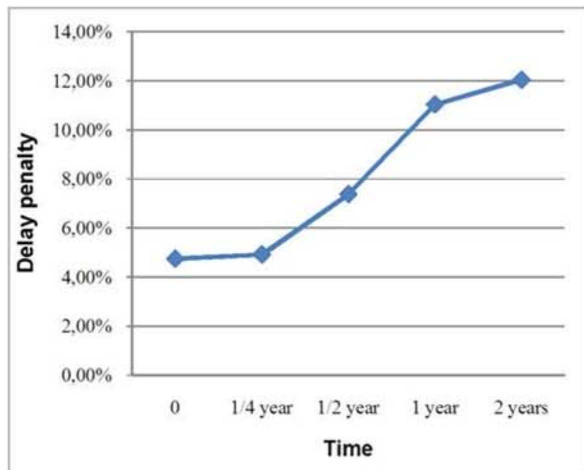

Figure 15. Delay penalty in the worst case

When we compare the power for the worst case (Fig 16), we see that the power benefit is significantly reduced to only 2-3% since the power gated circuit does not enter the sleep mode. The power benefit is almost negligible in this worst case.

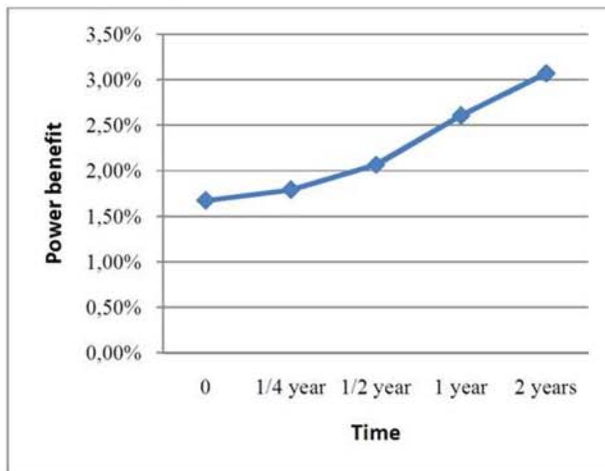

Figure 16. Power benefit in the worst case

IV. Conclusions

We evaluated the reliability and power consumption benefits of power gated circuits in 22nm technology under the effects of NBTI/PBTI. We found that power-gating can improve the reliability and save a lot of power as long as there is enough time that the circuit is allowed to enter sleep mode. In this work, with 70% sleeping time, the power gated circuit reduced delay by 3% and reduced power consumption by 12-16%. The main reason of the lower delay was that the sleep transistor reduced the leakage current and power so that the whole circuit could work at a lower temperature. Power-gating reduced the impact of transistor aging effects, which also contributed to lowering the delay.

Although the amount of deduced delay is not very impressive, the degradation of delay over time of the power gated circuit is much less than that of the non-power gated circuit. Even when the power gated circuit did not have a lower temperature to achieve a delay benefit and had a higher delay, it still had much lower delay degradation over time, which can be already considered in design and can help improve the reliability over time.

On the other hand, the benefit of power-gating degrades if the circuit does not enter sleep mode enough. In the worst case when the circuit never enters the sleep mode, the power benefit was negligible and the delay increased even faster. If this situation is likely to happen to the circuit, there is no point to apply power-gating technology in the first place.

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