Leakage in Nanometer Scale CMOS Circuits

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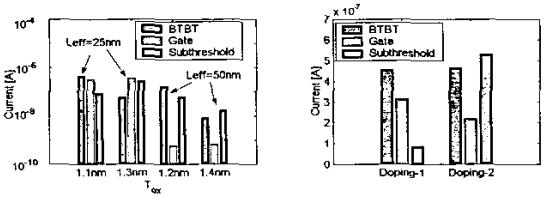
ABSTRACT

High leakage current in deep sub-micron regimes is a significant contributor to the power dissipation of CMOS circuits as the CMOS technology scales down. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low power applications. This paper explores transistor leakage mechanisms and device and circuit techniques to reduce leakage power consumption.

1. Introduction

For over 30 years CMOS devices have been continuously scaled to achieve higher density, better performance, and lower power consumption. With each technology generation, transistor delay times have decreased by more than 30%, resulting in a doubling of microprocessor performance every two years. To limit power consumption, the supply voltage (V_{DD}) has been scaled down. This necessitates a corresponding reduction in threshold voltage (V_{th}) to maintain a high drive current and achieve the performance improvement. However, scaling the threshold voltage results in a substantial increase in subthreshold leakage current [1]. When scaling the channel lengths, it is also necessary to scale the gate oxide thickness nearly proportionally to maintain a reasonable immunity to the short channel effect. The short-channel effect (SCE) is the decrease in gate threshold voltage as channel length is reduced. The thin gate oxides and the resultant high electric fields across the gate oxides enable considerable current to flow through the gate of the transistor. This gate current violates the classical assumption of infinite input impedance of MOS transistors and adversely affects circuit performance. Other leakage components such as band-to-band tunneling (BTBT) and drain-induced barrier lowering (DIBL) have a strong dependence on the device doping profile.

The total leakage current I_{OFF} is influenced by the threshold voltage, channel physical dimensions, channel/surface doping profile, drain/source junction depth, gate oxide thickness, and V_{DD}. Fig. 1 shows variation of different leakage components with (a) technology generation and oxide thickness; and (b) doping profile. The magnitudes of each of these components depend strongly on the device geometry (namely, channel length, oxide thickness and transistor width) and the doping profiles as shown in Fig. 1. In devices with thicker oxides,



(a) (b)

Fig. 1: Variation of different leakage components with (a) technology generation and oxide thickness; and (b) doping profile. "Doping-1" has a different halo profile than "Doping-2"

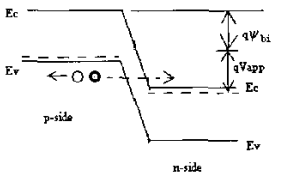


Fig. 2: Band-to-band tunneling in reversed bias p-n junction.

subthreshold and/or BTBT leakage is the dominant component. However, gate leakage becomes dominant in devices with thinner oxides. Moreover, the change in the doping profile changes the relative magnitude of subthreshold current and BTBT. A doping profile with higher halo doping reduces subthreshold current but increases BTBT. A significant reduction in BTBT can be achieved by reducing halo doping, however, that increases the subthreshold current.

The leakage contributions from all of these sources must be taken into consideration in future digital designs to fully benefit from the new high-resolution lithographic techniques that permit continued CMOS scaling. This paper highlights several important leakage mechanisms and suggests device and circuit techniques to reduce leakage power consumption.

2. Leakage Components

Understanding the different components of leakage current is a necessary prerequisite to developing techniques to effectively reduce the off-state leakage.

2.1. Band-to-Band Tunneling (BTBT) Current

In the presence of a high electric field (> 10^6 V/cm) electrons will tunnel across a reverse biased p-n junction. A significant current can arise as electrons tunnel from the valence band of the p-region to the conduction band of the

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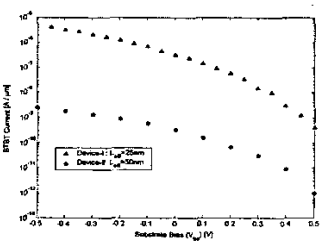

Fig. 3: Variation of BTBT leakage with substrate bias. Simulated result from MEDICI using 25nm and 50nm effective length devices from [3].

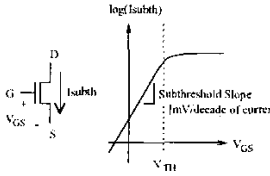

Fig. 4: Subthreshold leakage in NMOS transistor.

n-region, as shown in Fig. 2 [2]. As evident in figure 2, tunneling occurs when the total voltage drop across the junction is greater than the semiconductor band-gap. Since silicon is an indirect band gap semiconductor the BTBT current in silicon involves the emission or absorption of phonons.

In an NMOS device when the drain or source is biased at a potential higher than that of the substrate, BTBT current flows through the drain-substrate or source-substrate junction. If both *n*- and *p*-regions are heavily doped, which is the case for scaled MOSFETs using heavily doped shallow junctions and halo doping for better SCE, BTBT significantly increases and becomes a major contributor to the total off-state current. Fig. 3 shows the simulated BTBT current from 25nm effective length devices [3] using MEDICI [4]. Substantial increases in BTBT current are observed at high reverse biases. Reducing substrate doping near the substrate-drain/source junction is an effective way to reduce the BTBT current. However, this increases the SCE leading to considerable increase in the subthreshold current. Although there are not any reported circuit techniques specifically targeted at reducing BTBT, forward substrate biasing can be used to reduce BTBT in a MOSFET (since electric field reduces with reduction in the reverse bias across the junction).

2.2 Subthreshold Leakage

Subthreshold leakage is the weak inversion conduction current that flows between the source and the drain of a MOS transistor when gate voltage is below V_{th} [5]. In contrast to the strong inversion region in which drift current dominates, subthreshold conduction is dominated by diffusion current. In a similar manner to charge transport across the base of a bipolar transistor, carriers move by diffusion along the surface. Weak inversion typically dominates modern device off-state leakage due to the low V_{th}.

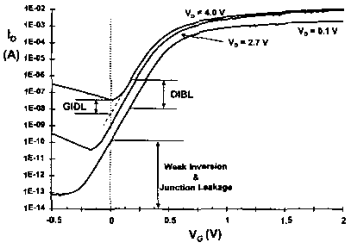

Fig. 5: n-channel I_D vs. V_G showing DIBL, GIDL, weak inversion, and pn junction reverse bias leakage components [6].

Subthreshold current is exponentially related to the gate voltage as illustrated in Fig. 4. The inverse of the slope of the $\log_{10}(I_{ds})$ versus V_{gs} characteristic is called the subthreshold slope (S_t) [5]. Subthreshold slope indicates how effectively the transistor can be turned off when V_{gs} is decreased below V_{th} thus it is desirable to minimize S_t. Typical values of S_t for a bulk CMOS process range from 70mV/decade to 120mV/decade.

2.2.1 Drain-Induced Barrier Lowering (DIBL)

In long-channel devices, the subthreshold current is independent of the drain voltage for V_{DS} larger than few v_T. In short channel devices, subthreshold current at high drain bias can be significantly higher than at low drain biases due to DIBL. DIBL occurs when the depletion region of the drain interacts with that of the source near the channel surface. When a high drain voltage is applied to a short channel device, it lowers the potential barrier height and the source then injects carriers at the channel surface independent of the gate voltage. The surface DIBL typically occurs before the deep bulk punchthrough. Although DIBL lowers V_{th}, DIBL does not change the subthreshold slope (S_t) in the ideal case. Fig. 5 illustrates the DIBL effect as it moves the I_D-V_G curve up and to the left as the drain voltage increases. Devices with shorter channels experience a stronger DIBL effect and thus have severely reduced threshold voltages at high drain biases. Increased surface and channel doping and shallower source/drain junction depths reduce the DIBL effect on the subthreshold leakage current [5,7].

2.2.2 Body Effect

Reverse biasing the well to source junction of a MOSFET transistor widens the bulk depletion region and increases the threshold voltage [8]. Fig. 6 shows a reduction in *n*-channel drain current when the well-to-source voltage

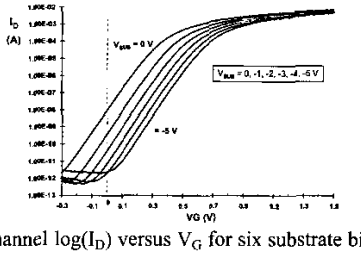

Fig. 6: n-channel $\log(I_D)$ versus V_G for six substrate biases on a 0.35 μm logic process technology (V_D = 2.7 V) [6].

is back biased from 0 to -5 V (the back bias is the well voltage) [6]. The subthreshold slope, S_t, is virtually unchanged with the applied substrate (well) biases. Figure 6 shows that increasing the reverse substrate bias decreases I_{OFF} by shifting the I-V curve to the right and increases V_{th}. The subthreshold leakage of an MOS device including the weak inversion current, DIBL, and the body effect, can be modeled as [9]:

$$I_{subth} = A \times e^{\frac{1}{mv_T}(V_G - V_S - V_{th0} - \gamma' \times V_S + \eta \times V_{DS})} \times \left(1 - e^{\frac{-V_{DS}}{v_T}}\right) \quad (1)$$

where

$$A = \mu_0 C'_{ox} \frac{W}{L_{eff}} (v_T)^2 e^{1.8} e^{\frac{-\Delta V_{th}}{\eta v_T}} \quad (2)$$

V_{th0} is the zero bias threshold voltage, and $v_T=KT/q$ is the thermal voltage. The body effect for small values of source to bulk voltages is linear and is represented by the term $\gamma' V_S$ in (1), where γ' is the linearized body effect coefficient. η is the DIBL coefficient, C_{ox} is the gate oxide capacitance, μ_0 is the zero bias mobility, and m is the subthreshold swing coefficient of the transistor. ΔV_{TH} is a term introduced to account for transistor-to-transistor leakage variations.

2.2.3. Subthreshold Modification by Quantization

In scaled devices, due to a high electric field at the surface (E_s) and high substrate doping, the quantization of inversion-layer electron energy modulates V_{th}. Quantum-mechanical behavior of the electrons increases V_{th}, thereby reducing the subthreshold current since more band bending is required to populate the lowest sub-band, which is at an energy higher than the bottom of the conduction band. When E_s is larger than 10^6 V/cm, electrons occupy only the lowest sub-band. In that case, the quantization effect can be modeled as an increase in threshold voltage by an amount ΔV_{QM}, given by [2]:

$$\Delta V_{QM} = \left(1 + \frac{3t_{ox}}{X_d}\right)\left(\frac{\Sigma_0}{q} - \frac{kT}{q}\ln\left(\frac{8\pi q m_d E_s}{h^2 N_C}\right)\right) \quad (3)$$

where, Σ_0 is the lowest sub-band energy [2], N_C is the effective conduction band density of states, m_x is the quantization effective mass of electron and m_d is the density of states effective mass of electron.

3.1. Tunneling Into and Through Gate Oxide

Thin gate oxides coupled with the consequent high electric fields across the oxides result in gate oxide tunneling current. Electrons tunnel from the substrate to the gate and also from the gate to the substrate through the gate oxide. There are two different mechanisms of tunneling between substrate and gate poly-silicon, namely, (I) Fowler-Nordheim (FN) tunneling and (II) direct tunneling. Gate leakage in scaled devices is mainly derived from direct tunneling.

In thin oxide layers (less than 3-4 nm), electrons from the inverted silicon surface tunnel directly to the gate through the forbidden energy gap of the SiO_2 layer [2] (as shown in Fig. 7) instead of tunneling into the conduction

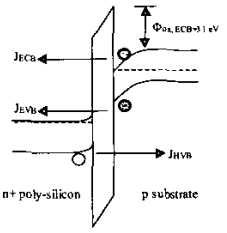

Fig. 7: Mechanisms of direct tunneling of electrons.

band of SiO_2 as in FN tunneling. In the case of direct tunneling, electrons tunnel through a trapezoidal potential barrier instead of a triangular potential barrier. Thus direct tunneling occurs at $V_{ox}<\phi_{ox}$ [10]. The equation governing the direct tunneling current density is given by [10]:

$$J_{DT} = AE_{ox}^2 \exp\left\{-B\left[1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)^{3/2}\right]\Big/E_{ox}\right\}$$
$$A = \frac{q^3}{16\pi^2 \hbar \phi_{ox}} \text{ and } B = \frac{4\sqrt{2m^*}\phi_{ox}^{3/2}}{3\hbar q}. \quad (4)$$

Fig. 8 shows the variation of the direct tunneling current density with V_{ox} using (4). Potential drop across the oxide is given by:

$$V_{gs} = V_{fb} + V_{ox} + \phi_s + V_{poly} \quad (5)$$

where V_{gs} is the applied gate bias; ϕ_s is the surface potential; and V_{poly} is the potential drop across the poly-silicon depletion region.

Three major mechanisms contribute to direct tunneling in MOS devices, namely, Electron tunneling from Conduction Band (ECB), Electron tunneling from Valence Band (EVB), and Hole tunneling from Valance Band (HVB) [11-12] (Fig. 9). The gate direct tunneling current can be divided into five major components, namely, parasitic leakage current through gate-to-S/D extension overlap region (I_{gso} and I_{gdo}); gate to channel current (I_{gc}), part of which goes to the source (I_{gcs}) and the rest goes to the drain (I_{gcd}); and the gate to the substrate leakage current (I_{gb}) (Fig. 9) [11-12]. The modeling of each of the components can be found in [11-12]. In NMOS, ECB controls the gate to channel tunneling current in inversion, whereas gate to body tunneling is controlled by EVB in depletion-inversion and ECB in accumulation. In PMOS, HVB controls the gate to channel leakage in inversion,

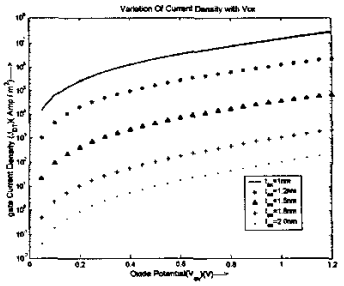

Fig. 8: simulated direct tunneling current

whereas gate to body leakage is controlled by VBET in depletion-inversion and CBET in accumulation [11-12]. Since the barrier height for HVB (4.5 eV) is considerably higher than the barrier height for ECB (3.1 eV), the tunneling current associated with HVB is much less than the current associated with ECB. This results in lower gate leakage current in PMOS than in NMOS [13].

The emission of electron from Si to SiO_2 causes a build up of image charge at the oxide side of the Si/SiO_2 interface, which results in a reduction in the barrier height at the Si/SiO_2 interface from ϕ_{ox}=3.1eV by an amount $\Delta\phi$ given by:

$$\Delta\phi = \sqrt{\frac{q^3 E_{ox}}{4\pi\varepsilon_{ox}}} \qquad (6)$$

where ε_{ox} is the permittivity of SiO_2. This is called the image-force-induced-barrier lowering effect [2]. Since it modulates the ϕ_{ox}, it also modulates the gate tunneling current since the tunneling exponentially depends on ϕ_{ox}.

Until a suitable high-κ dielectric material that will allow a physically thicker oxide to be used without sacrificing short channel effect immunity becomes readily available, gate leakage current will be a concern. Other than new dielectrics, there are not many reported techniques for the reduction of gate leakage in MOSFETs. However, the multiple oxide thickness technique used to reduce subthreshold leakage can also be effectively used to reduce the gate leakage. In the multiple oxide technique transistors in the non-critical paths have a higher oxide thickness, therefore the gate tunneling current through them is considerably less and the total leakage through the circuit is significantly reduced [14]. However, as mentioned earlier the increased oxide thickness has to be accompanied by a longer gate length to reduce the SCE.

3. Leakage Reduction Techniques

Significant reduction in leakage current is obtained through applying a combination of process and circuit-level techniques. At the process level, controlling the physical device dimensions (length, oxide thickness, junction depth, etc) and the device doping profiles leads to a reduction in leakage current. At the circuit level, controlling the voltages on the four terminals of each device (drain, gate, source, and substrate) can effectively adjust the threshold voltage and leakage current of the transistors.

3.1. Channel Engineering for Leakage Reduction

The goal of channel engineering is to minimize the off-state leakage current while maximizing the linear and saturation drive currents. By changing the device doping profile in the channel region, the distribution of electric field and potential contours is altered, which affects different components of the current. Super Steep Retrograde Wells (SSRW) and halo implants have been used as a means to scale the channel length and increase the transistor drive current without causing an increase in the off-state leakage current [16]. Fig. 10 is a schematic

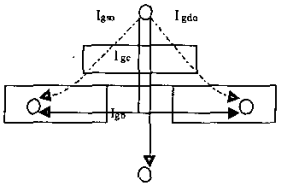

Fig. 9: Components of Tunneling current [11-12].

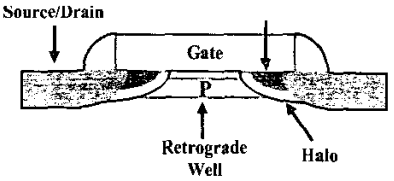

Fig. 10: Graphical representation of different aspects of well engineering [15].

representation of a device with a retrograde well and halo implants [15]. In a retrograde structure, there is vertically non-uniform doping with a low doping concentration near the surface channel and a more highly doped subsurface region. This results in higher surface channel mobility by minimizing impurity scattering in the channel while improving SEC immunity and preventing punchthrough. Halo doping is a laterally non-uniform channel profile that was introduced below the 0.25 μm technology node to provide another way to control the dependence of threshold voltage on channel length. The doping near the two edges of the channel is increased by the injection of point defects during sidewall oxidation, which gather doping impurities from the substrate. The halos act to reduce charge sharing effects from the source and drain fields, reducing the width of the depletion region in the drain-substrate and source-substrate regions. As the channel length is reduced, these highly doped regions consume a larger fraction of the total channel width, reducing the depletion width and guarding against the normal threshold voltage degradation caused by channel length reduction. Thus, the threshold dependance on channel length is weakened as shown in Fig. 11. The off-current sensitivity to channel length variation is thereby reduced.

3.2. Leakage Reduction Using Transistor Stacks

The "stacking effect" is the reduction in subthreshold current observed when multiple transistors connected in series (in a stack) are turned off. The stacking effect can be easily explained by considering the two input NAND gate

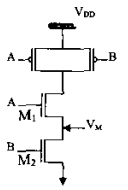

Fig. 12: Stacking effect in 2-input NAND gate.

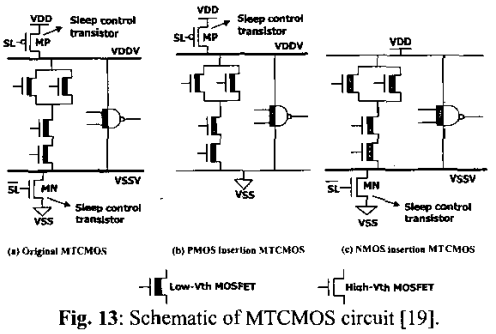

Fig. 13: Schematic of MTCMOS circuit [19].

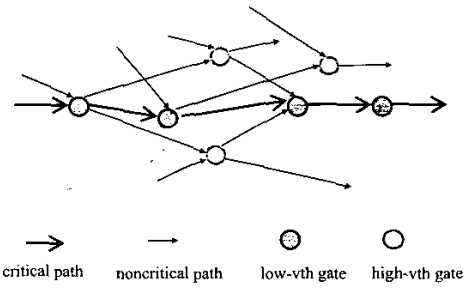

Fig. 14: Dual V_{th} CMOS circuit.

shown in Fig. 12. When both M_1 and M_2 are turned off, the voltage at the intermediate node (V_M) is slightly positive due to the non-zero drain leakage current [17]. With a positive source potential, V_M, the gate to source voltage of M1 (V_{gs1}) is negative, and hence the subthreshold current reduces substantially. Moreover, since $V_M > 0$, the body to source potential (V_{bs1}) of M_1 is negative, resulting in an increase in the threshold voltage of M_1 due to the body effect, which also reduces the subthreshold leakage. In addition, with $V_M > 0$, the drain to source potential (V_{ds1}) of M_1 decreases thereby raising the threshold voltage of M_1 by reducing the DIBL and thus reducing the subthreshold leakage.

As a result of the stacking effect, subthreshold leakage through a logic gate depends on the applied input vector and the total leakage current of a circuit is dependent on the states of the primary inputs [18]. Exhaustively searching all 2^n combinations of primary input values would lead to finding the minimum leakage state, but the exponential complexity limits exhaustive searching to circuits with a small number of primary inputs. For large circuits, a random search based technique can be used to find good input combinations.

3.3. Multiple V_{th} Designs

By providing both low and high threshold transistors is a single chip, multiple-threshold CMOS technologies address the leakage problem while still achieving high performance. Multiple threshold voltages can be achieved by multiple channel doping profiles, multiple oxide thicknesses, multiple channel lengths or multiple body biases.

3.3.1. Multi-Threshold-Voltage CMOS (MTCMOS)

Multi-Threshold-Voltage CMOS (MTCMOS) reduces the leakage by inserting high threshold sleep control devices in series to low-V_{th} circuitry [19]. Fig. 13(a) shows the schematic of a MTCMOS circuit. In the active mode, the sleep control signal SL is set low and the high-V_{th} sleep control transistors (MP and MN) are turned on. Since the on resistances of MP and MN are low, VDDV and VSSV act like power supply lines. In the standby mode, SL is set high, the high threshold sleep control transistors MN and MP are turned off, resulting in low leakage current. In fact, leakage can be effectively controlled using only PMOS or NMOS sleep transistors as shown in Fig. 13 (b) and (c),

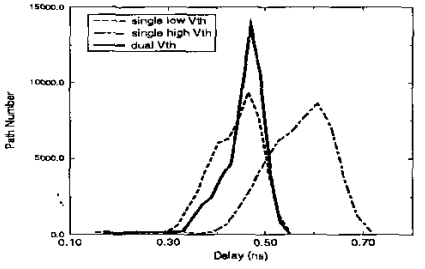

Fig. 15: Path distribution of dual V_{th} and single V_{th} CMOS.

respectively. Since an NMOS device of a given width has a smaller on-resistance than a PMOS of the same width, the NMOS scheme can be realized with smaller transistors and is therefore preferable [20].

3.3.2. Dual Threshold CMOS

In logic circuits, it is possible to reduce the leakage current by assigning higher threshold voltages to devices in non-critical paths, while maintaining performance with low V_{th} transistors in the critical paths [21]. This technique does not require any additional transistors and both high performance and low power can be achieved simultaneously. Fig. 14 illustrates the concept of dual-V_{th} circuits. Fig. 15 shows the path delay distributions of dual V_{th} and single V_{th} CMOS for a 32-bit adder. Dual V_{th} CMOS has the same critical delay as the single low V_{th} CMOS circuit, but transistors in non-critical paths can be assigned a high V_{th} to reduce leakage power. Dual threshold CMOS is a good technique for leakage power reduction during both standby and active modes of operation without adding delay or area overhead.

3.4. Dynamic V_{th} Design

Dynamic threshold voltage scaling is a technique to adjust the active leakage power based on the desired frequency of operation. The frequency is dynamically adjusted through the back-gate bias in response to the workload of a system. When the workload decreases, the threshold voltage is increased and less power is consumed. A block diagram of the Dynamic V_{th} Scaling (DVTS) Scheme and its feedback loop is presented in Fig. 16 [22]. A clock speed scheduler, which is embedded in the operating system, determines the (reference) clock

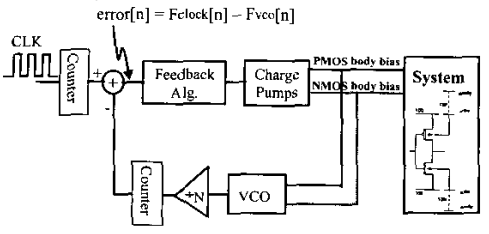

Fig. 16: Schematic of DVTS hardware [22].

frequency at run-time. The DVTS controller adjusts the PMOS and NMOS body bias so that the oscillator frequency of the VCO tracks the given reference clock frequency. The error signal, which is the difference between the reference clock frequency and the oscillator frequency, is fed into the feedback controller. The continuous feedback loop also compensates for variation in temperature and supply voltage.

4. Conclusion

As CMOS devices continue to scale, leakage becomes an even more important contributor to the total power consumption. In current technologies, subthreshold and gate leakage are the dominant sources of leakage and are expected to increase with technology scaling. In advanced devices, band-to-band tunneling is also likely to be a concern. To manage these leakage currents it will be necessary to consider leakage management at both the process technology and circuit levels. At the process technology level, well engineering techniques such as retrograde and halo doping are used to reduce leakage and improve short channel characteristics. At the circuit level, transistor stacking, multiple V_{th}, and dynamic V_{th} techniques can effectively reduce the leakage current in high performance logic and memory designs.

5. Acknowledgements

This research was funded by the SRC, GSRC, Intel, and IBM.

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