Analysis of SRAM Reliability under Combined Effect of NBTI, Process and Temperature Variations in Nano-Scale CMOS

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Abstract*— As dimensions of MOS devices have been scaled down, new reliability problems are coming into effect. One of these emerging reliability issues is aging effects which result in device performance degradation over time. NBTI (Negative biased temperature instability) is a well known aging phenomenon which is a limiting factor for future scaling of devices. NBTI results in the generation of trapped charges which cause V_t (threshold voltage) degradation of PMOS. It is observed that a sharp V_t shift occurs in just a few seconds after turning on the MOSFET. In nano-scale CMOS technologies, process (threshold voltage) and temperature variations are also crucial reliability concerns. On the other hand, NBTI itself is dependent on temperature and threshold voltage. In this paper, the combined effect of NBTI, process and temperature variations on the reliability of the 6T SRAM (Static Random Access Memory) in 32nm CMOS technology is analyzed. It is observed that: (1) V_t abruptly increases initially and afterwards V_t shift is very small, even for prolonged time; (2) Low V_t transistors age faster than high V_t transistors; and (3) NBTI V_t degradation is more significant at higher temperature. Along with these observations, we also quantified our results in terms of number of faulty cells in SRAM array. It is observed that: (1) number of faulty cells rises over time (8.2% rise in faulty cells for the inter-die nominal V_t chip over 2 years) due to SNM degradation; (2) rise in the number of faulty cells over time due to write failures under NBTI effect is practically negligible; (3) Leakage (in the worst case condition) and access time are not impacted by NBTI.

I. INTRODUCTION

Ultra thin dimension CMOS technology is facing many critical challenges. NBTI or aging effect is a critical reliability issue which has come into picture with continuous scaling of transistors. Under NBTI, due to trapping of charges, V_t of PMOS goes up and PMOS becomes slower over time. Moreover, with scaling of the MOSFET, the manufacturing process control degrades causing many parameters to experience some degree of variability. Threshold voltage is one of the critical parameters which experiences variability due to process variations. This variability is basically of two types: Inter-die (die to die) variation and Intra-die (within die) variation. These variations are caused by many reasons like variations in channel length, channel width, channel doping, oxide thickness, line-edge roughness, and random dopant fluctuations. To account for inter die V_t variations, we considered three different chips: low V_t chip (V_t=0.35V), nominal V_t chip (V_t=0.4V), high V_t chip (V_t=0.45V). The temperature of the chip varies due to work load and work environment. To account for temperature change, we considered two temperature levels: room temperature (25°C) and worst case temperature (100°C).

The effect of NBTI aging on SRAM reliability has been studied [1, 6, 7, 8]. In [1, 6, 7, 8] the behavior of NBTI and its impact on the 6T SRAM cell has studied in different technologies (70nm [1], 32nm [6], 35nm [7], 70nm and 90nm [8]). However, the results from these papers show the impact of NBTI alone on the SRAM without considering the variations in threshold and temperature. Hence the combined effect of NBTI aging with temperature and process variations has not been researched. Given the strong dependence of NBTI on temperature and threshold voltage, the impact of NBTI can be greatly different under variations in threshold voltage and temperature. In this work, we analyze and report the combined effect of NBTI, threshold voltage and temperature variations on the SRAM reliability, in terms of Static Noise Margin (SNM) and write margin, of the 6-Transistor SRAM cell in 32nm CMOS process. HSPICE simulation tool and the predictive 32nm model [4], are used to analyze the reliability of SRAM under the combined effect of NBTI, the process and temperature variations. Our results show that:

1) Low V_t transistors age faster than high V_t transistors and NBTI V_t degradation is more significant at higher temperature.
2) SNM degrades under NBTI effect in the worse case; however, the write margin degradation is particularly insignificant. At higher temperature, degradation due to NBTI is more significant in the case of low V_t transistors as compare to high V_t transistors.
3) Low V_t SRAM chips show more number of faulty cells over time as compared to high Vt SRAM chips.
4) Leakage (in the worst case condition) and access time are not impacted by NBTI.

The remainder of this paper is organized as follows. Section 2 briefly describes the modeling of NBTI under the process and temperature variations. Section 3 explains the effect of NBTI on the SRAM. Section 4 shows the combined effect of NBTI, process variation and temperature variation on the performance metrics of the SRAM: SNM (Static Noise

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Margin), write margin. We also quantified our results in terms of number of faulty cells after 1/8 years, 1/4 years, 1/2 years, 1 year and 2 year. Finally, Section 5 concludes the paper.

II. Model of NBTI under Temperature and Process Variations

A comprehensive model for NBTI Vt shift is given in [2, 3]. In our research, we simplified the models given in [2, 3] for the DC stress condition and for V_{ds}=0 (as is the case for the PMOS of SRAM cell that is affected by NBTI (PL in Fig. 2)) and came up with the following model

$$\Delta V_t = (1+m)K_v t^{0.25} + \delta_v$$
$$K_v = A \cdot t_{ox} \cdot \sqrt{C_{ox}(V_{gs}-V_t)} \cdot \exp\left(E_{ox}/E_o\right) \cdot \exp\left(-E_a/KT\right) \quad (1)$$

where t_{ox} is the oxide thickness, E_{ox} is the electric field across the oxide ($(V_{gs}-V_t)/t_{ox}$). A, E_a, E_0, δ_v , m and K are constants [2,3], and t is stress time in seconds. This model shows the dependence of V_t shift on temperature (T) and process (threshold voltage) variation (V_t).

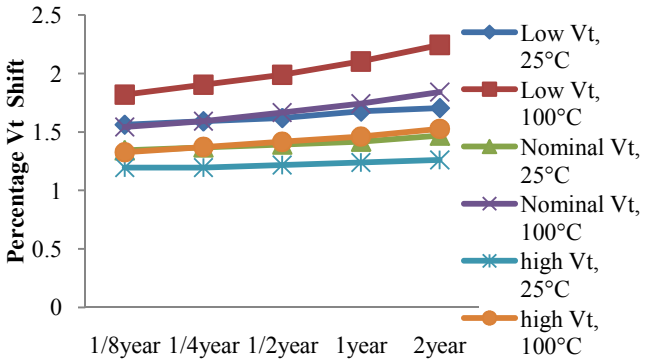

Fig. 1: V_t shift for the three technology corners: Low Vt transistors, Nominal Vt transistors, High Vt transistors at room temperature (25°C) and worst case temperature (100°C).

Fig. 1 shows the percentage of V_t shift in three process corners: Low V_t transistors, Nominal V_t transistors and High V_t transistors at two temperatures: room temperature (25°C) and worst case (100°C). These results show that V_t shift is greater at high temperature and at low V_t. This is due to the dependence of K_v factor in Eq. 1 on the temperature and threshold voltage.

III. Impact of NBTI on SRAM

Fig. 2 shows the schematic diagram of the 6T SRAM cell. It has two pull up PMOS and two pull down NMOS transistors to form two cross coupled inverters and two NMOS access transistors to access the SRAM cell during Read and Write operations.

In Fig. 2, the 'ON' PMOS PL is under stress and experiences the NBTI V_t shift. This V_t shift can cause the change in the performance metrics of the SRAM: SNM (Static Noise Margin), Write Margin, Access time and Leakage. Among these performance metrics, SNM (Static Noise Margin) degrades over time under stressed conditions. The reason is, under the stress conditions, the trip point of the left inverter becomes low due to the increased V_t of PL, and hence the cell can be more easily flipped during the read operation.

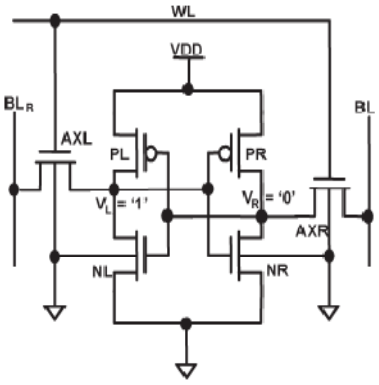

Fig. 2: Schematic diagram of SRAM where pull up PMOS PL is stressed.

Write margin improve over time for the first write cycle because slower PL will help the discharging of the node '1'. However, for second write cycle to write the initial state back to the cell, write margin degrades because the other pull up transistor PR has not been stressed (has low V_t) which is not helpful in the discharging of '1'. Moreover, the inverter PL-NL trip point has reduced which makes the second write more difficult. Leakage is not impacted by NBTI because leakage is decided by the current flowing through the OFF transistor which is not affected by NBTI. Access time is not impacted by NBTI because it is determined by discharging of BL through NMOS access transistors and NMOS pull down transistors which are not impacted by NBTI.

IV. Combined Effect of NBTI, Process and Temperature Variation

Although the individual effect of NBTI has been studied and verified by many researchers [1, 6, 7, 8], in reality, not only aging effect degrades the reliability of SRAM, temperature and process variations also play crucial roles. Moreover, as observed in the previous section, NBTI is dependent on the temperature and V_t process parameter. In this work, we analyzed the combined effect of NBTI, the process and temperature variation on the reliability of SRAM cell, in terms of Static Noise Margin (SNM), write margin and leakage of 6T SRAM cell in the 32nm CMOS process. Three types of chips are considered to incorporate the effect of inter die variations: Low V_t, Nominal V_t and High V_t transistors. For intra die process variations, which are mostly caused by random dopant fluctuations, we applied random values of V_t to all 6 transistors of SRAM and for many SRAM cells in a chip.

SNM is affected by the static process variations and the environmental variations such as temperature as well as aging effects such as NBTI. In this work, the combined effect of NBTI, temperature and process variations on the SNM over the life-time of the SRAM is analyzed. Fig. 3 shows the SNM degradations of low V_t, nominal V_t and high V_t transistors for room temperature (25°C) and worst case temperature (100°C). The results show that SNM degradation is more significant at higher temperature for all process corners. At room temperature, SNM degradation is negligible at different process corners (less than 1%), however, at higher temperature, SNM degradation is more in case of low V_t cells as compared to high V_t cells. Hence, it can be concluded that SRAM chips that are shifted to low V_t process corners will experience faster SNM degradation as a result of NBTI compared to the chips that are shifted to high V_t corners.

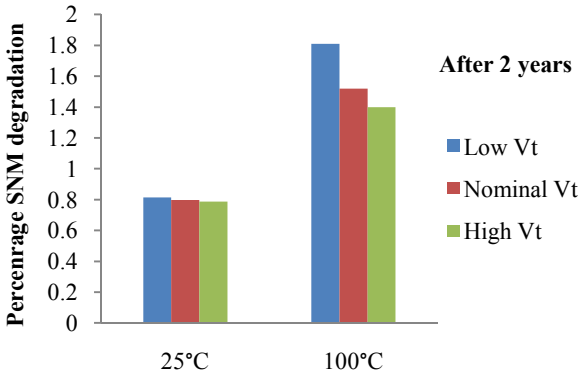

Fig. 3: SNM degradation after 2 years. SNM degradation is considerably higher in low V_t cell and at high temperature.

In reality, V_t variation has a statistical nature showing some average and some standard deviation which result in statistical variations in SNM. Hence, a more realistic SNM measurement is the SNM statistical distribution which can be obtained using the Monte Carlo simulations. Fig. 4 shows the intra-die statistical variation of the SNM degradation for low inter-die V_t chip at 100°C. It clearly shows that the SNM distribution shifts towards lower values. From the statistical SNM distribution and by setting a target SNM (45mV), we can estimate the percentage of faulty cells. Table 1 shows the percentage of faulty cells for all three inter-die process corners: low V_t, nominal V_t, and high V_t transistors at 100°C. Fig. 5 shows the percentage rise of faulty cells due to the SNM degradation for low inter-die V_t technology corner at 25°C and 100°C. It is observed that the number of faulty cells increases (8.2% over 2 years) only at the high temperature. Even though SNM degrades slightly at 25°C, this degradation does not cause any new failures.

In write operation of SRAM cell, while writing a "0" to a cell storing "1," the node V_L gets discharged through BL_B to a low value (V_{WR}) determined by the voltage division between the PMOS *PL* and the access transistor *AXL*. If V_L cannot be reduced below the trip point of the inverter *PR*−*NR* within the time when the word-line is high (T_{WL}) then a write failure occurs.

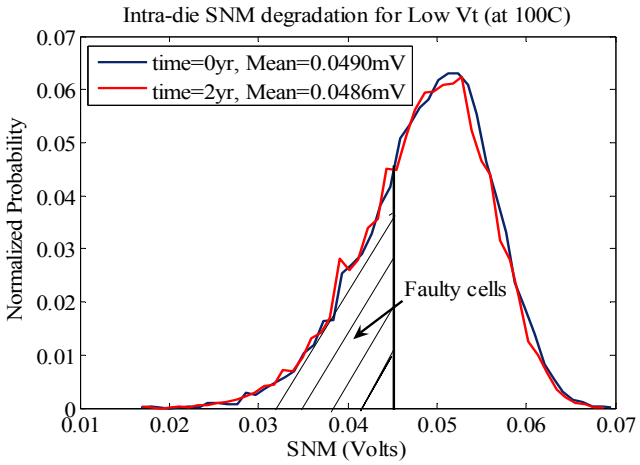

TABLE I. PERCENTAGE OF FAULTY CELLS DUE TO SNM DEGRADATION AGING AND PROCESS VARIATIONS AT 100°C

Faulty cells (%)	0yr	1/8yr	1/4yr	1/2yr	1yr	2yr
Low Vt	26.56	28.26	28.37	28.52	28.63	28.74
Nominal Vt	1.49	1.68	1.69	1.7	1.71	1.71
High Vt	0.09	0.1	0.1	0.1	0.1	0.1

Fig. 4: Statistical distribution of SNM due to intra-die Vt variations for the low inter-die V_t chip at time 0 and after 2 years. Number of faulty cells increase over time as SNM distribution shifts to left.

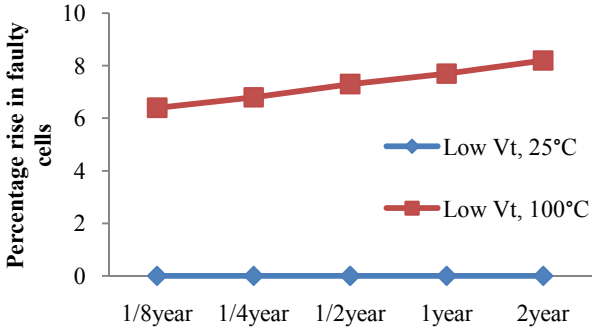

Fig. 5: Percentage rise of faulty cells due to SNM degradation increases over time at 25°C and 100°C. It is observed that number of faulty increase (8.2% over 2years) only at the high temperature.

The discharging current (I_L) at node *L* is the difference in the ON currents of the access transistor *AXL* (I_{AXL}) and the PMOS *PL* (I_{PL}) (i.e., $I_L = I_{AXL} - I_{PL}$) [6]. PMOS becomes slower due to NBTI, I_{PL} goes down. So write margin improves in first write cycle but write margin degrades under NBTI effect in the worse case which is the second write cycle to write the original state back to the cell.

For the second write cycle SRAM, pull up transistor *PR* is not aged and *PL* is aged, making it slow which is not helpful in the discharging of '1' from node V_R. Moreover, decreased *PL* strength reduces the trip voltage of the inverter *NL-PL* which makes the pull up operation at node VR slightly harder, thereby causing slight decrease in write margin. However, this write margin decrease is insignificant as shown in Fig. 6. Write margin degradation is practically negligible and does not cause any new write failures over time. Table 2 shows the number of faulty cells for all three process corners: low V_t, nominal V_t, and high V_t chips at 100°C. It is observed that low V_t chips show very few faulty cells as compared to high V_t chips. The reason is that high ON current at low V_t cells helps the fast charging and discharging of nodes which results in a faster write operation, hence resulting in less number of write failures. However, it is observed that there is no significant increase in number of write failures over time.

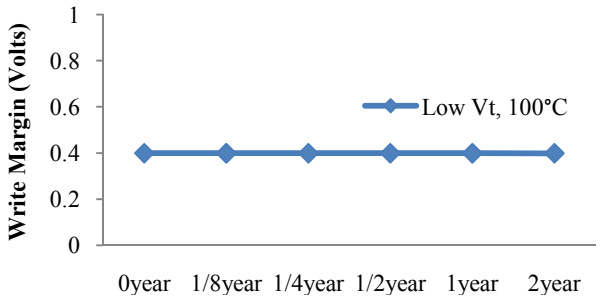

Fig. 6: Write margin slightly degrades over time. However, this degradation of write margin is practically negligible.

TABLE II. PERCENTAGE OF FAULTY CELLS DUE TO WRITE MARGIN DEGRADATION UNDER AGING AND PROCESS VARIATIONS AT 100°C (FOR TARGET WRITE MARGIN OF 0.3V)

Faulty cells (%)	0yr	1/8yr	1/4yr	1/2yr	1yr	2yr
Low Vt	0	0	0	0	0	0
Nominal Vt	0.1	0.1	0.1	0.1	0.1	0.1
High Vt	2.9	2.9	2.9	2.9	2.9	2.9

Leakage power is defined as the power consumption during the OFF state and is determined by the current flowing through OFF MOS transistors. Since the OFF transistor is not affected by the NBTI, leakage is not impacted by NBTI. For the worse case, where cell will remain in the initial state over lifetime, leakage does not change over time. Fig. 7 shows the leakage current for the low V_t SRAM cell at 100°C over time. It is observed that leakage does not change over time. This observation however is valid for the worst case situation where the cell state does not change over the lifetime. If the cell state changes, there will be some leakage reduction over time due to increased V_t.

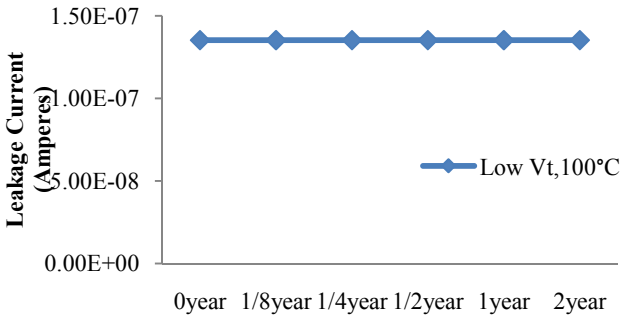

Fig. 7: SRAM cell leakage current for low V_t inter-die chip over time. NBTI does not impact leakage current.

V. CONCLUSION

In this paper, the combined effect of the NBTI, process (V_t) and temperature variations is discussed. It is observed that low V_t transistors age at faster rate than high V_t transistors and NBTI V_t degradation rate is more significant at higher temperature. As a result, low V_t SRAM chip shows more increase in number of faulty cells over time as compared to the high Vt SRAM chip because SNM degradation due to NBTI is more significant in the case of low V_t transistors as compare to high V_t transistors. However at room temperature, NBTI does not cause any new cell failure due to SNM degradation because at the room temperature, SNM degradation is practically insignificant. It is observed that write margin slightly degrades under NBTI effect in the worse case which is the second write cycle. However, the overall degradation in write margin is practically negligible. Leakage (in the worst case condition) and access time are not impacted by the NBTI effect.

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