Incorporating Effects of Process, Voltage, and Temperature Variation in BTI Model for Circuit Design

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***Abstract*— Bias Temperature Instability (BTI) is a major reliability issue in Nano-scale CMOS circuits. BTI effect results in the threshold voltage increase of MOS devices over time. Given the Process, Voltage, and Temperature (PVT) dependence of BTI effect, and the significant amount of PVT variations in Nano-scale CMOS, we propose a method of combining the effects of PVT variations and the BTI effect for circuit analysis. We investigate the PVT dependence of BTI effect on a ring oscillator circuit as a test bench for logic circuits and an SRAM cell as a test bench for memory circuits. The results show that low threshold voltage circuits at high temperature experiences the worst impact of aging effects. However, the bias dependence of the impact of aging effects on circuits may vary from circuit to circuit and from metric to metric depending how the sensitivity of the circuit to BTI threshold voltage shift at different biasing changes.**

Keywords- Aging effects; Nano-scale CMOS; Process variations; Voltage variations; Temperature variations

I. INTRODUCTION

As dimensions of MOS devices have been scaled down, new reliability problems are coming into effect. One of these emerging reliability issues is aging effects which result in device performance degradation over time. Aging effect results threshold voltage (ΔV_{th}) degradation of transistor due to interface charge trap generated during device "ON" state. Aging effect has two components: negative bias temperature instability (NBTI) which results in degradation of PMOS, and positive bias temperature instability (PBTI) which results in degradation of NMOS [1, 2, 3]. NBTI is modeled by considering hydrogen (H^+) as diffusing elements in interfacial layer based on a reaction-diffusion model [1, 2]. Observations made in [1], [2], and [4] provide details of PBTI in high-k dielectric. In Nano-scale CMOS technologies, process (threshold voltage) and temperature variations are also crucial reliability concerns. On the other hand, NBTI itself is dependent on temperature and threshold voltage (ΔV_t). In this work, we analyzed the combined effect of transistor aging, process and temperature variations at two supply voltage levels for a five stage ring oscillator (RO) circuit and a six transistor (6T) static random access memory (SRAM) cell in 32nm CMOS technology using Predictive Technology Model (PTM) [5] with simulations performed in SPICE. To account for inter die V_t variations, we considered three different chips: lowV_t chip, nominal V_t chip, and high V_t chip. The temperature of the chip varies due to work load and work environment. To account for temperature change, we considered two temperature levels: room temperature (25°C) and worst case temperature (100°C).

The remainder of this paper is organized as follows. Section II describes the BTI model used for 32nm circuit simulation. In section III, RO simulation results are explained based on observations obtained in delay, dynamic and static power with various circuit conditions. Section IV shows the combined effect of transistor aging, process variation and temperature variation on the performance metrics of SRAM: SNM (Static Noise Margin), write margin and access time, at two supply voltage level. Finally, Section V concludes the paper.

II. BTI MODEL INCORPORATING EFFECTS OF TEMPERATURE VOLTAGE AND PROCESS VARIATIONS

A comprehensive model for BTI threshold voltage shift is given in [1-3]. In our research, we simplified the model in [3] to calculate BTI induced V_t degradation as follows:

$$\Delta V_t = K_v \cdot \beta^{0.25} \cdot t^{0.25} + \delta_v \tag{1}$$

Where,

$$K_v = A \cdot T_{ox} \cdot \sqrt{C_{ox}(V_{gs} - V_{th})} \cdot \exp\left(\frac{E_{ox}}{E_o}\right) \cdot \left[1 - \frac{V_{ds}}{\alpha(V_{gs} - V_{th})}\right] \cdot \exp\left(-\frac{E_a}{kT}\right)$$

$$E_{ox} = (V_{gs} - V_{th})/T_{ox};\ T_{ox} = EOT = (3.9/K) \cdot t_{hk}$$

Where, K_v is the rate at which H^+ species are generated, β is the percentage of the time the device is under stress, and t is the total time. T_{ox} is the effective oxide thickness *(EOT)* which is smaller than the physical thickness of the dielectric in the case of high-K dielectric, where K is relative permittivity of the high-k dielectric, t_{hk} is the thickness of high-k. C_{ox} is oxide capacitance per unit area, V_{gs} is gate voltage, V_{th} is threshold voltage, E_{ox} electric field in the oxide, V_{ds} is drain to source voltage, E_a is activation energy, k and T are Boltzmann constant and temperature in Kelvin, respectively. Other parameters such as δ_v, A, E_o, α are obtained from [3]. Based on the models, the increase in V_t is similar to V_{gs} decreases by the same amount. This model captures the effects of PVT parameters *(V_{th}, V_{gs},* and *T)*. According to the model, the value of ΔV_t should be higher at low V_{th} corner, and with high temperature and high voltage conditions. This is verified by results in Fig. 1 which shows percentage of NBTI induced V_{th} shift over time for a low V_t PMOS at two temperature (25°C and 100°C) and two stress voltages (0.5V and 1V).

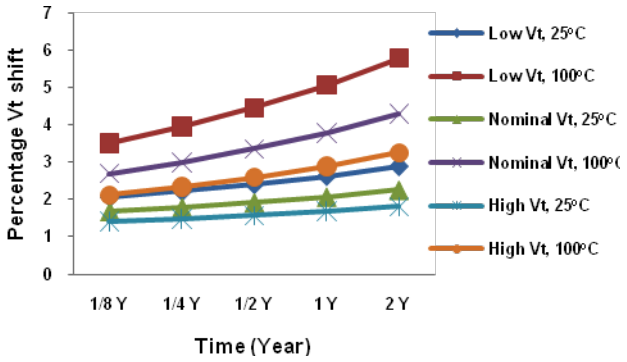

Figure 1. Percentage of NBTI induced Vt shift in high-k dielectric 32nm PMOS for three technology corners: Low, Nominal, and High Vt at room (25°C) and worse case temperature (100°C)

III. Combined Effect of Aging Effect, Process and Temperature Variation on Ring Oscillator Circuit

To observe the combined effect of BTI with **P**rocess, **V**oltage, and **T**emperature (PVT) variations; while considering PVT dependence of BTI, SPICE simulations are performed on a ring oscillator (inverter chain) circuit in a predictive 32nm technology (Fig. 2). V_{th} values vs. time are estimated from the model (Eq. 1) and then plugged into the circuit for simulation. We consider two supply voltages: low supply voltage of 0.5V and high supply voltage of 1V. Die-to-die process variations are represented by considering three values of threshold voltage: nominal, low (nominal-50mV), and high (nominal+50mV) threshold voltage. Two cases of temperature are considered: low temperature (25°C) and high temperature (100°C). Under each PVT condition, V_{th} values over time are estimated using Eq. 1 and then applied to a five stage RO (inverter chain) to observe the impact on circuit parameters (delay and power). The input of the circuit is connected to a 1GHz pulse for delay and power characterization.

To analyze impact of aging effect on circuit delay at different V_{th} corners, a comparison of percentage of delay increase over time is made at 25°C and 1V supply (Fig. 3). The results show the low V_{th} circuit experiences percentage delay increase over time. Fig. 4 shows the percentage delay increase over a 2-year life time for low V_t RO cell at two temperatures (25°C and 100°C) and two supply voltages (0.5V and 1V). The results show that the impact of BTI aging effect on circuit delay is enhanced at higher supply voltage and higher temperature. This is attributed to the increased V_{th} shift at higher voltage and temperature conditions (Eq. 1).

The increased V_{th} due to BTI is expected to reduce the circuit power due to reduction in leakage power as V_{th} increases. This expectation is verified by results in Fig. 5. Fig. 5 (a) shows percentage reduction in active mode power at different conditions of supply voltage and temperature. Fig. 5 (b) shows the percentage of reduction in standby (leakage) power. The results show that the leakage power reduction is more significant at high voltage and high temperature conditions. This is attributed to the exponential dependence of sub-threshold leakage to V_{th} and higher amounts of V_{th} shift at high voltage and temperature conditions. The switching power is not affected by aging effects as it is not V_{th} dependent. Hence, the change in the active power (Fig. 5(a)) is only due to the change in the leakage power portion of the total active power.

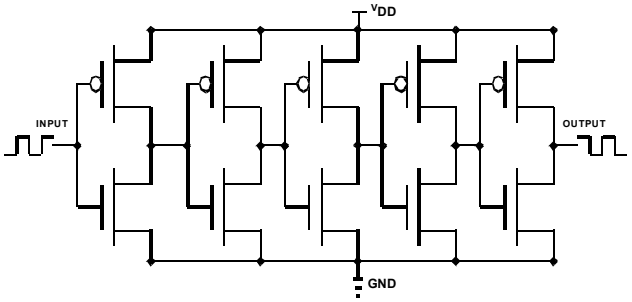

Figure 2. Five stage ring oscillator (inverter chain) test bench.

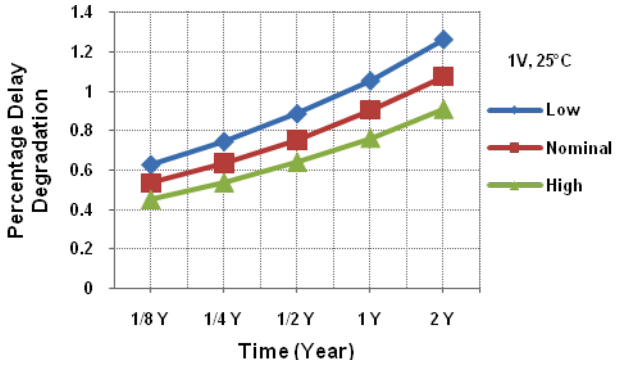

Figure 3. Ring Oscillator circuit degradation over time for three threshold voltage corners: low, nominal, high V_t. Low V_t circuit shows more degradation compared to high V_t circuit.

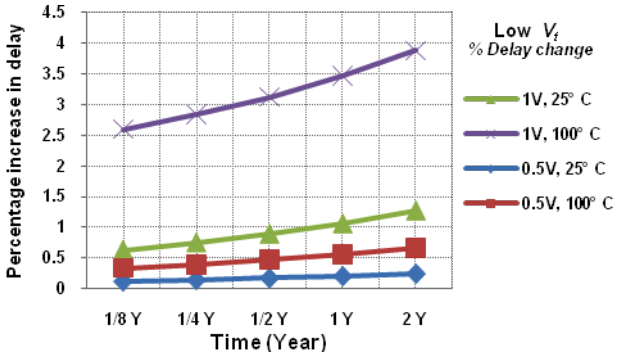

Figure 4. Delay degradation over two years. The circuit experiences more delay increase under high voltage and high temperature conditions.

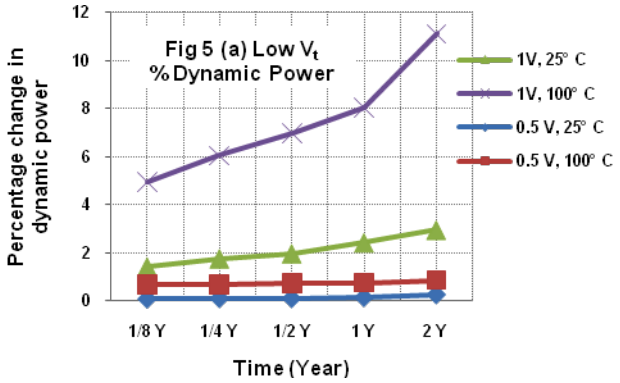

Figure 5(a). Impact of BTI on circuit power: percentage of active mode power reduction over time. Reduction at high voltage and high temperature condition.

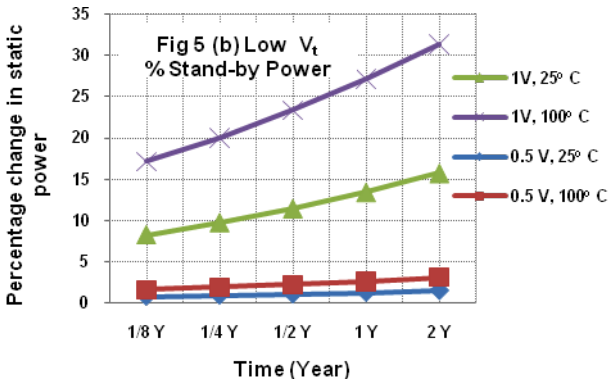

Figure 5(b). Impact of BTI on circuit power: percentage of standby (leakage) power reduction. More change is observed for high temperature and high voltage condition.

IV. Combined Effect of Aging Effect, Process and Temperature Variation on SRAM Circuit

Although the effect of time dependent V_t degradation on SRAM cell with high-k dielectrics due to NBTI (in case of PMOS) and PBTI (in case of NMOS) has been studied and verified by many researchers [6], [7], [8], in this work, we analyzed the combined effect of aging effect (NBTI and PBTI), the Process (V_{th}), Voltage, and Temperature variations on the reliability of SRAM cell, in terms of Static Noise Margin (SNM), write margin and access time of 6T SRAM cell (shown in Fig. 6) in 32nm CMOS process. In this work, we considered two types of SRAM chips:-low voltage SRAM cell (0.5V) and high voltage SRAM cell (1V). Even though at low supply voltage, stress induced V_t shift will be less (Eq. 1), but the sensitivity of the cell to V_{th} variation will be more. So by using two supply voltage levels, we observed that the sensitivity of cell to variations has dominance over stress induced V_t degradation over time in case of access time, whereas in case of write operation stress induced V_t degradation is more crucial. In case of SNM, initially low voltage SRAM cell shows more degradation as compared to high voltage SRAM cell. Over long time, high voltage SRAM cell shows more SNM degradation.

Fig. 7 shows the percentage degradation of SNM of low V_t, SRAM cell for two temperatures, one room temperature (25°C) and second high temperature (100°C) with two supply voltages – low voltage SRAM cell (0.5V) and high voltage SRAM cell (1V). SNM degrades over time due to stress induced V_t mismatch. Initially, SNM degradation is more in case of low voltage SRAM cell as compared to high voltage SRAM cell because low voltage SRAM cell is more sensitive to variations as compared to high voltage SRAM cell. However, over prolonged time, V_t shift is considerably more in case of high supply voltage as compared to low supply voltage. As per simulation results obtained, it is evident that high voltage SRAM cell shows more SNM degradation for long periods of time. To integrate the inter-die V_t variation, three types of cells: low, nominal, and high V_t have been considered in this work. Fig. 8 shows the SNM degradation for low, nominal, and high V_t cells. It can be observed that low SNM degradation as compared to high V_t because low V_t cell experience greater V_t shift over time as compared to high V_t cell.

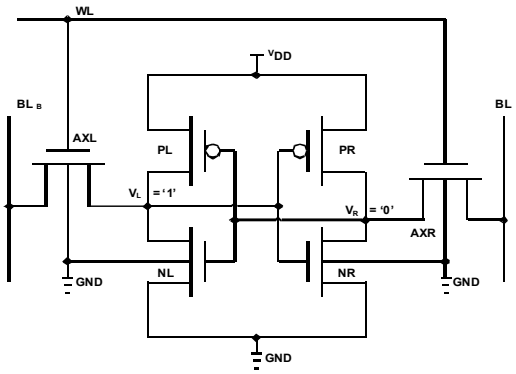

Figure 6. Schematic diagram of six transistor (6T) SRAM cell with pull up PMOS *PL* (under NBTI) and pull down NMOS *NR* (under PBTI) stressed.

In this work, we observe the write margin of SRAM cell for worse case which is the second write cycle (when V_R=1 and V_L=0) to write the original state back to the cell. For the second write cycle SRAM, the pull up transistor *PL* and the pull down transistor *NR* are aged. The aged *PL* is not helpful in the discharging operation of the node V_R=1, but it makes the pull up operation at node V_L harder. Moreover aged *NL* impedes the discharging of '1' at node V_R, and hence the write margin degrades over time. Fig. 9 shows the percentage degradation of write margin with low V_t SRAM cell for two temperatures: room temperature (25° C) and high temperature (100° C) and at two supply voltages: low voltage SRAM (0.5V) and high voltage SRAM (1V). It is observed that write margin degradation is more in case of high voltage SRAM cell (4.4% degradation in write margin) as compared to low voltage SRAM cell and degradation is more significant at higher temperature. Hence, it can be concluded that high voltage SRAM will experience faster SNM degradation as a result of high stress induced V_t variations as compared to the low voltage SRAM cell.

The cell access time is defined as the time required producing a pre specified voltage difference ($\Delta MIN \approx 0.1 V_{DD}$) between two bit-lines (bit-differential) [9]. The access time is determined by discharging of *BL* through NMOS access transistors and NMOS pull down transistors. For the worse case, Transistors *PL* and *NR* degrade under the PBTI aging effect. Aged *NR* makes discharging of *BL* harder which causes access time degradation in the SRAM cell. Fig. 10 shows percentage degradation of access time in low V_t cell considering two temperatures: room temperature (25°C) and worst case temperature (100°C) with two supply voltage: low voltage SRAM (0.5V) and high voltage SRAM (1V). The results show that access time degradation is more significant at higher temperature regardless of supply voltage and access time

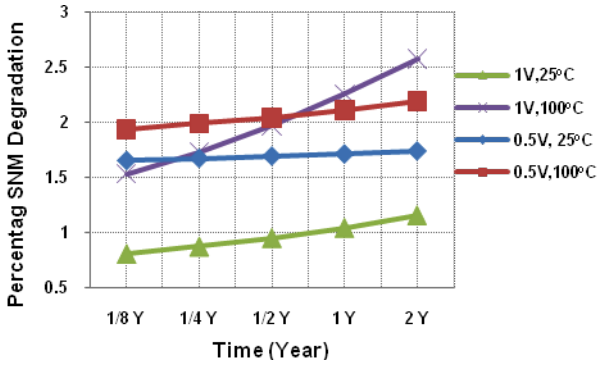

Figure 7. SNM degradation over two years. Initially SNM degradation is considerably higher in low voltage SRAM cell and at high temperature. Over long period of time, high voltage and high temperature SRAM cell shows more SNM degradation.

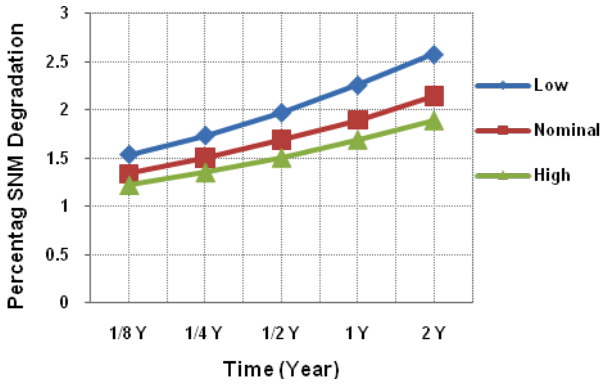

Figure 8. SNM degradation over time for the three technology corner 6T SRAM cell: low, nominal, high V_t. Low V_t cell show more SNM degradation as compared to high V_t.

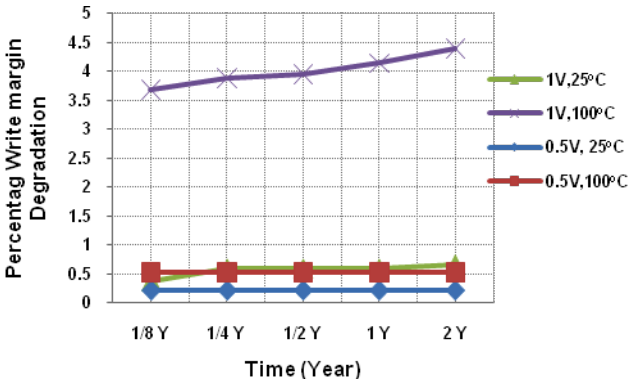

Figure 9. Write margin degrades over time and degradation is considerably higher in high voltage SRAM cell and at high temperature.

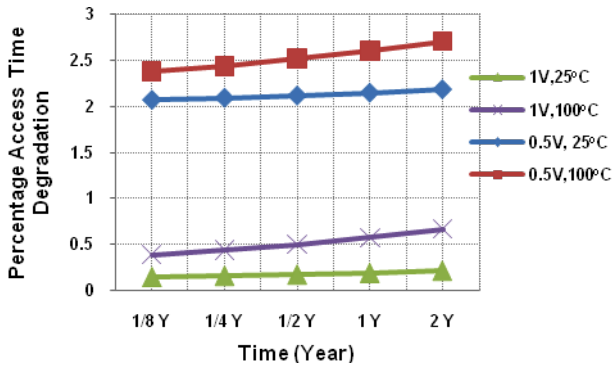

Figure 10. SRAM cell access time degradation for low V_t inter-die chip over time. Access time degradation is considerably higher in low voltage SRAM cell and at high temperature.

degradation is more in case of low voltage SRAM with 2.7% degradation in read current compared to high voltage SRAM cell. Hence, it can be concluded that low voltage SRAM will experience faster access time degradation as a result of high sensitivity towards variations as compared to high voltage SRAM. Leakage power is defined as the power consumption during the "OFF" state and determined by the current flowing through "OFF" MOS transistors. Since for the worse case, the pull up transistor *PL* and pull down transistor *NR* remains under stress and experience V_t degradation. The "OFF" transistor (*PR* and *NL*) are not affected by BTI. Thus, leakage is not impacted by the aging effects.

V. CONCLUSION

This paper analyzed circuit reliability for combinational circuits (ring oscillator) and 6T SRAM cell in 32nm CMOS process, considering PVT dependence of NBTI and PBTI aging effects. We analyzed how the BTI model can be PBTI used to capture the combined effect of PVT variations and BTI aging effects on circuit reliability analysis. The BTI induced threshold voltage shift is higher at low $V_{th,}$ high temperature, and high voltage conditions, however, the resulting impact on circuit parameters (delay, power, SNM, etc) may not be maximum in the high voltage corner due to reduced circuit sensitivity to the V_t variation at high supply voltage. Such a behavior was observed in the case of access time of SRAM cell where the low voltage cell shows more aging induced access time degradation than the high voltage cell. Future work include, finding an optimal minimum supply voltage for Nano-scaled devices which shows minimum aging impact on logic and memory circuits.

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