Full-Custom Design Project for Digital VLSI and IC Design Courses using Synopsys Generic 90nm CMOS Library

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ABSTRACT

We have developed a full-custom IC design flow based on Synopsys custom design tools and the recently released Synopsys 90nm generic library. The developed design flow can be used for teaching VLSI and digital IC design courses. We have also developed a full-custom design project that was used as a course project in teaching "Digital VLSI Design" course at San Francisco State University. The design project is to design a 4-bit ripple carry adder in a full custom fashion from schematic to layout in the generic 90nm CMOS technology. The developed design flow and the course project provide a very effective hands-on approach to teaching digital IC design and VLSI design in advanced CMOS technologies. The team project was conducted in a competition based format providing great enthusiasm and motivation among the students, enhancing their learning experience. The competition was to achieve the best design quality defined as the product of following design metrics: propagation delay, power dissipation, and layout area for the 4-bit ripple carry adder. The winning team achieved a delay of 82.2ps, power dissipation of 30.7 μW, and layout area of 112.8 μm^2 for the 4-bit adder.

1. Introduction

One of the most effective methods of teaching is the hands-on method. This is especially true in engineering, which involves a lot of design practices and design skills which can only be truly learned by doing [1]. VLSI Design is no exception. VLSI Design involves a great deal of skills involving layout design and transistor sizing and optimization and understanding design trade-offs. Hence, the most effective method for learning VLSI design concepts is by doing a design project which involves different aspects of design from schematic to layout.

Given the rapid progress of industry in scaling of CMOS technology towards nano-scale regimes, the VLSI teaching at universities needs to be constantly updated to reflect these rapid industry developments. For most universities, access to modern CMOS technologies can be very cumbersome due to legal issues and also not convenient for industries due to intellectual property issues. In order to facilitate access of universities to a modern CMOS process for teaching purposes, Synopsys Inc. offers a generic 90nm library that resembles an actual CMOS manufacturing process [2]. This new library enables students to gain the experience of design in an advanced CMOS technology and using Synopsys modern EDA tools. This library provides a technology kit, digital standard cell library, I/O standard cell library, memories, and Phase Locked Loop (PLL).

At San Francisco State University (SFSU) School of engineering, we offer a course on "Digital VLSI Design" with the objective of teaching students the analysis and design of Very Large Scale Integrated (VLSI) Circuits. The course begins with the fundamentals of digital IC design and small circuits such as inverter and basic logic gates and then progresses towards more complex circuits such as arithmetic units and memory. The skills learned in this course will prepare students to do real-world design tasks or do research in various areas of VLSI and circuit design. In order to achieve this course objective, we need the following components: 1) a full-custom design flow using modern EDA tools 2) modern CMOS process design kit and library and 3) a design project that touches different aspects of custom IC design from schematic to layout.

In this paper, we describe our development of these three components through collaboration with Synopsys Inc. We believe this model can be used by other universities in teaching digital IC design and VLSI design courses. The developed tutorials are also provided online for reference [3].

The remainder of the paper is organized as follows. In section 2, the custom design flow using Synopsys custom design tools is described. In section 3, a description of the Synopsys 90nm generic library is provided. Section 4 describes the design course project. The implementation and result of the design project are drawn in section 5. Finally section 6 concludes the paper.

2. Full-Custom Design Flow using Synopsys Custom Design Tools

The Synopsys tools used for this project are integrated in the Synopsys custom design environment, which makes using them in a flow convenient and efficient. Fig. 1 shows our custom design flow and the tools used in each stage.

Since these tools are industry grade and very powerful, at first glance they can seem intimidating to students who are not yet trained in using these tools because of all the settings and options available to the end user. We have developed a tutorial which students can use as

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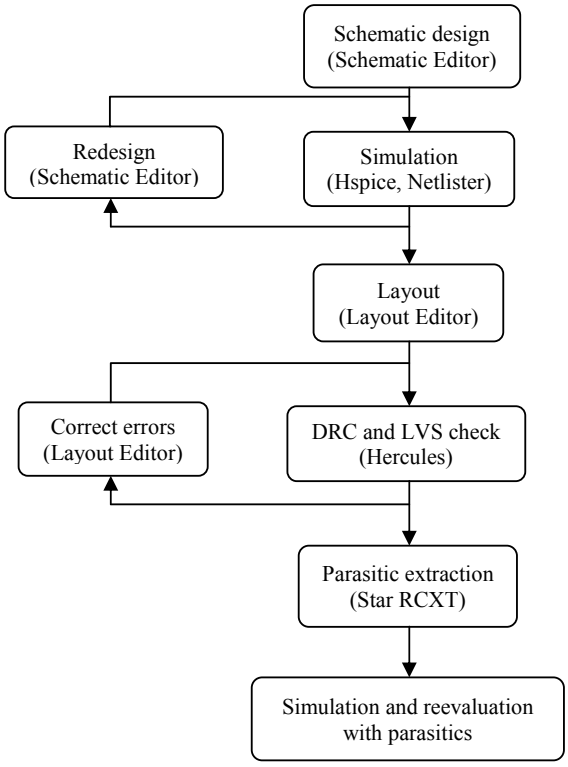

Fig. 1: Custom design flow chart

a self study guide to learn the design flow and design tools [3]. Our tutorial manual not only guides the user through the design flow for using these tools, but also how to set up the tools, which is essentially the same for the class design project as it is for the tutorial examples.

3. Synopsys 90nm CMOS Generic Library

Synopsys is providing a 90nm CMOS generic library for university users [2] that will enable students easy access to an advanced CMOS technology for practicing design in modern CMOS using modern EDA tools. This generic library is free from Intellectual Property (IP) restrictions. IP restrictions typically make it hard for universities to access real industrial process kits. The generic library is optimized for low power design and use with Synopsys EDA tools. Even though this library is not designed for fabrication, it provides all the elements of a real foundry based library, hence allowing students to gain experience of designing in an advanced CMOS technology. The contents of the 90nm generic library includes a technology kit, digital standard cell library, I/O standard cell library, memories, and phase locked loop. In our project development, we are only interested in the technology kit component of the library because our design flow is a full-custom IC design flow and our project is also a full-custom design project. However, we plan to extend the use of this library and Synopsys EDA tools to other courses which involve ASIC design and use of the other components of the library such as standard cell library. The technology kit includes a data book and user guide, symbols, .lib, DRC and LVS decks, generic SPICE models, and runset files.

4. Course Design Project: 4-Bit Ripple Carry Adder

To provide students with the opportunity for a hands-on experience with full-custom design in 90nm CMOS, we defined a course project that students implement throughout the course. The following considerations are made in defining the project: 1) it has to be a hierarchical design (gate-level to transistor level) 2) it has to be modestly complex and yet manageable as a full-custom course design project. A 4-bit ripple carry adder (Fig. 2) is a suitable design project. It is hierarchical and manageable as full-custom design course project. The building block of the design is a 24-transistor mirror Full Adder circuit (Fig. 3) [4]. The design optimization starts with the schematic design of the full adder and optimization for power and delay. Given that the critical path in the ripple carry adder is well defined (carry propagation path), the design effort needs to be spent on reducing the carry propagation delay of the full adder (C_i to $/C_o$ delay). The optimization goal for the ripple carry adders is to obtain the least delay, power, and layout area simultaneously. To quantify the optimization metric in the form of a single measurable quantity, the product of these three metrics (power, delay, and area) is used as an optimization metric. When designing the schematic of the full-adder, the design effort is spent on minimizing the power and delay product (PDP), where delay is the carry propagation delay and power is the power dissipation of the full adder operating at a target frequency of 1 GHz for this project. The carry propagation path of the full adder is composed of the pull down network of MN_1, MN_2, and MN_3, and the pull up network of MP_1, MP_2, and MP_3 (Fig. 3). Hence, the rest of the transistors are given minimum size dimensions (W/L=120nm/100nm) and the design optimization effort is spent on transistors MN_1, MN_2, MN_3, MP_1, MP_2, and MP_3. Given the symmetry of the design, MN_2 and MN_3 are given same size and also MP_2 and MP_3. Hence, the number of design parameters is reduced to the sizing of two NMOS transistor and two PMOS transistors. The optimization is performed to minimize the power delay product of the full adder. The optimization should be performed with proper loading of the full adder carry output ($/C_o$). For proper loading, two identical Full Adders (FA) need to be cascaded where the second FA acts as the load of the first FA.

Once the full adder schematic design is optimized, then the layout of the full adder is designed using the custom layout tool. For layout, the stick diagram shown in Fig. 4 is used. When performing layout, the design goal is to minimize layout area by minimizing spacing and wire dimensions. Design Rule Check (DRC) is performed on

the layout to remove any design rule violations (Fig. 1). The Layout Versus Schematic (LVS) check is also performed to ensure the layout matches the schematic.
Once the design of the full adder is finished (both schematic and layout) then a symbol view for the full-adder schematic is created. This allows hierarchical design where in the next level a new schematic view is created for the 4-bit ripple carry adder and four instances of the FA symbol are placed and cascaded to form the four-bit adder. Similarly the layout of the four-bit adder is obtained by creating four instances of a FA layout and cascading them. Finally, DRC and LVS need to be performed on the four-bit adder design for verification. The last step is to extract parasitics from the layout of the 4-bit adder and add the parasitics to the schematic of the 4-bit adder for post layout simulation. The post layout simulation is performed to obtain the 4-bit adder carry propagation delay and the power consumption which will be used to assess the quality of the design as will be discussed in the next section.

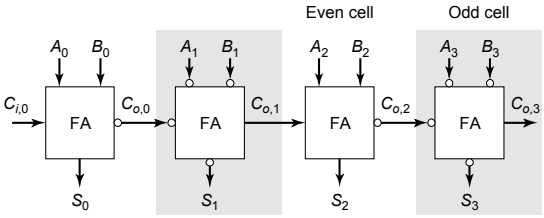

Fig. 2: 4-bit ripple carry adder [4]

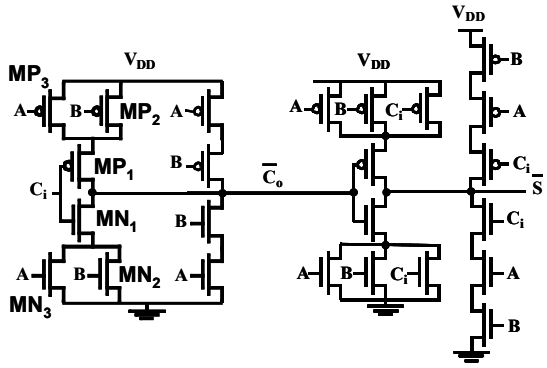

Fig. 3: Mirror full adder schematic [4]

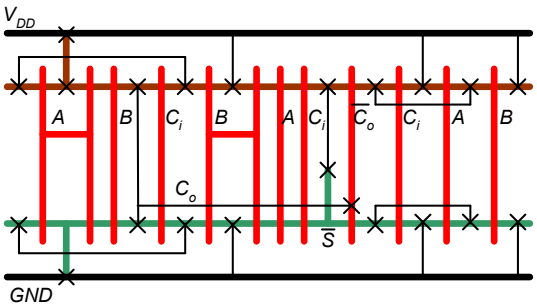

Fig. 4: Stick diagram for layout of mirror full adder [4]

5. Design Project Implementation and Results

Students were grouped in groups of no more than 3 students. The design specification, design goal, and competition format was given to students early in the semester. The competition was to achieve the best design quality defined as the product of propagation delay, power dissipation, and layout area for the 4-bit ripple carry adder. The design competition is to minimize this product quantity. The reward for winning the competition was a grade of 'A' in the class regardless of the scores the winning team members received on other assignments and tests. The grading policy for the course was as follows: 30% for mid-term exam, 30% for final exam, 30% for the course project, and 10% for homework assignments.
Students were provided with the design flow and CAD tool tutorials [3]. In order to facilitate the successful completion of the project by all groups, two tutorial lab sessions and one help session were scheduled during the semester. The first tutorial session covered logging into the server, setting up a work environment and creating and simulating a transistor level design. The second session focused on creating the layout and running DRC and LVS checks. The open help session was provided to help students who were having difficulties in the project to help them with their specific issues. By providing this level of support, we ensured that all project groups managed to finish their project in time and submit their results on time for evaluation on the final day of the class.
The project results were submitted by each group before the final day of the class. Results were organized and summarized by the professor when students met for the final session of the class. After ranking the results in terms of the defined quality metric (product of delay, power, and area for the 4-bit adder), the group in first place was required to demonstrate their project and defend their results before their classmates. If the student audience could identify any mistake in the measurements of the presenter team, they would be disqualified from getting the winning project title. This proved to be an effective method of judging the competition, as classmates pointed out that the group in first place made the mistake of measuring the power from the wrong source and measured the time delay for three adder stages when the other groups measured it for the full four stages. The group in second place was then allowed to defend their design and results successfully and was subsequently declared the winners of the competition. The winning team achieved a delay of 82.2ps, power dissipation of 30.7 μW, and layout area of 112.8 μm^2 which produced the least product of power, delay, and area. Table 1 summarizes all the results obtained for the four-bit adder by different teams. Fig. 5 plots the quality metric measurement of different groups for a relative comparison of performance of different project groups.

Table 1: Measurement results of group projects

Group	Delay (pS)	Power (μW)	Area (μm^2)	Quality product (Normalized to best design)
1	82.2	30.7	112.8	1.00
2	91.8	25.3	146.6	1.20
3	116.4	28.2	112.0	1.29
4	163.9	23.4	101.6	1.37
5	112.3	28.0	128.9	1.42
6	175.2	28.6	122.6	2.16
7	125.1	28.2	272.6	3.37
8	130.5	27.0	458.4	5.67
9	123.5	25.9	1682.2	18.90
10	618.1	26.1	47527.6	2695.58

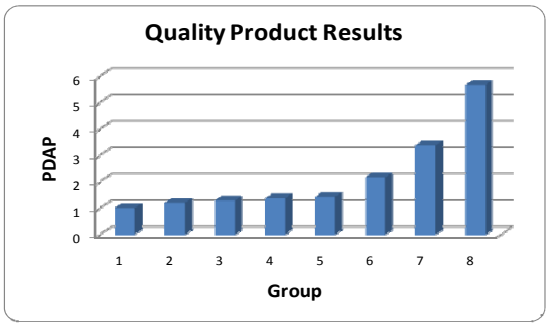

Fig. 5: Quality product results by group (normalized to best design, PDAP=Power Delay Area Product)

The winning design was also compared to other published adder designs in 90nm CMOS technology [5]. A relative comparison is shown in Fig. 6. The green design is the winning mirror adder design optimized for minimum Power Delay Area Product (PDAP) from the class design competition, the red design is a mirror adder optimized for minimum power, and the blue design is a domino adder optimized for minimum delay. This is not a perfect comparison for two reasons. First, the three adders are not all of the same logic style and optimized for the same metrics. Second, the published designs were simulated using a Cadence library. However, a comparison still shows interesting results. For example, the domino adder is typically the preferred logic style for fast arithmetic circuits. However, the winning mirror adder from our class competition actually had a shorter delay while also maintaining a smaller PDP. The comparison in Fig. 6 shows that the quality of the class designs is high, and the top designs are competitive with published designs.

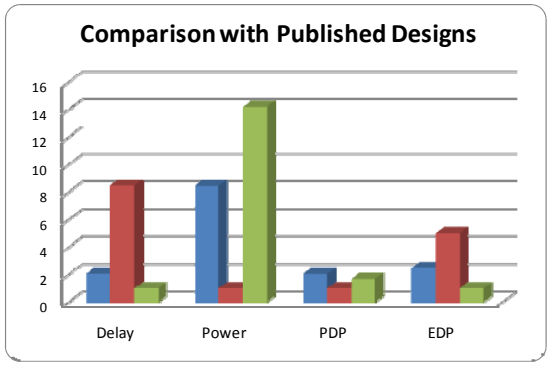

Fig. 6: Quality product results by group (normalized to best design in Delay, Power, Power Delay Product (PDP) and Energy Delay Product (EDP)

The advantage of this project competition format was that students were quite motivated and enthusiastic about working on the project. This helped their learning process. At the end most students appreciated the experience and expressed that they learned a great deal by doing the project.

6. Conclusions

In this paper, we presented a full-custom design project using a generic 90nm CMOS library and Synopsys custom design tools. The proposed design project can be used as a hands-on teaching method in courses on digital IC design and VLSI design courses in advanced CMOS technologies. The proposed course project is a 4-bit ripple carry adder design from schematic to layout in a full-custom fashion. This project captures the basic principles involved in design and optimization of digital integrated circuits and involves the design trade offs of power, delay, and area. Students formed project teams and the project was implemented in a competitive format with the goal of minimizing the product of power, delay, and area for the 4-bit adder. This competitive format improved the learning experience of the students and the students produced high quality designs.

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