Adaptive Supply Voltage Circuit Using Body Bias Technique

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Abstract–**In this paper a new circuit design technique using forward body biasing is presented. This technique may be employed in different circuits (e.g. logic gates, SRAM, high fan-in circuits). The advantages of this technique are reduced power dissipation and increased speed for domino logic circuits. Furthermore this technique is used to control the SRAM supply voltage, where the benefit is increased write margin. The simulation results show a significant decrease in power dissipation especially in high fan-in logic circuits.**

Index Terms–**SRAM, high fan-in, write margin, low power**

I. Introduction

MOSFET scaling deep into the sub-100nm regime has resulted in substantially greater leakage power consumption (Gate leakage and Subthreshold leakage) compared to a few generations ago [1]. One common technique for reducing power is to reduce the supply voltage, but the cost of lower supply voltage is lower performance. The problem of performance degradation can ameliorate by scaling the threshold voltage. As a result of lowering threshold voltage, the static power consumption increases [2]-[3].

A constant substrate biasing technique can also be used with a standard CMOS architecture to improve MOSFET performance. Indeed, forward body biasing reduces the threshold voltage V_T and thus increases the device speed, whereas reverse body biasing can be used to control the off-state leakage current for low power applications where static power dissipation is a major concern [4]. Chips with higher leakage tend to be faster, hence it is possible to apply reverse body bias to reduce leakage and reduce frequency. Similarly, slow chips can benefit from forward body bias to improve their speed at the expense of a moderate increase in leakage power. Similarly, adaptive supply voltage, used in conjunction with body bias can tighten the distribution [5]-[6]. It has been shown that, Forward Body Bias (FBB) is the most effective way to reduce both active and leakage power, while improving the performance of circuits in sub-100 nm technologies [7], [8], [9]. In this paper, the FBB technique is scrutinized in 65nm technology to see the effects on CMOS circuits for different supply voltages. In this analysis, constant bulk voltages that are appropriate for a circuit to have the highest speed are specified. In this paper two techniques are proposed for high speed and lower leakage logic circuits. This technique is utilized to implement a variable supply voltage mechanism depending on the input signals states. Furthermore, SRAMs comprise a significant percentage of the total area and total power for many digital chips [2]. SRAM leakage can dominate the total chip leakage, and switching highly capacitive bitlines and wordlines is costly in terms of energy [10], [11]. In this paper a new technique reducing the leakage is utilized for SRAM design which uses an adaptive supply voltage. This technique allows for further downscaling of the supply voltage.

The rest of this paper is organized as follows: Section II, describes forward body bias effect on devices in 65nm CMOS technology. Section III presents a new power supply topology based on body bias technique. This technique is employed in a domino logic circuit to show the beneficial effects of this technique. Section IV presents a new method to supply the 6T-SRAM cell improving the write speed. This technique enables

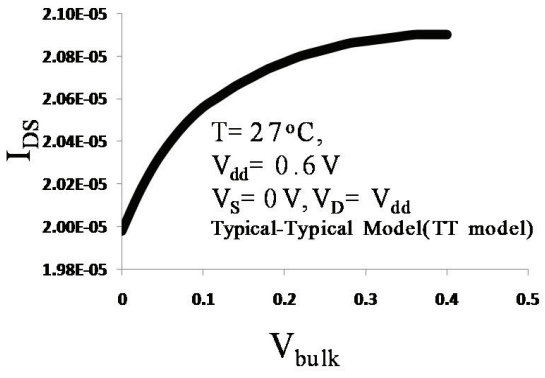

Fig.1. Drain current versus Bulk voltage

designers to use a lower supply voltage for SRAM design without any write margin degradation. In section V the conclusions are presented.

II. Forward Body Biasing Technique

In this chapter the effect of FBB technique is investigated for 65nm CMOS technology in corners. By utilizing this technique in NMOS devices, the threshold voltage decreases and as a result the drain current increases which in turn improves the speed of the circuit. Therefore, the highest speed of the NMOS is when the bulk is connected to VDD. In the case of a PMOS, when the bulk voltage is connected to ground, the threshold voltage decreases and the current through the PMOS device increases. The limitation however is that the forward bias amount must be small enough to preventing the junction diodes from turning on. This limits the forward bias range to be below the PN diode built-in potential, giving an acceptable forward bias range of about 500mV. Forward bias has been shown not only to improve performance, but to also reduce short channel effects [12]. In 65nm CMOS technology, FBB technique has a different effect on NMOS and PMOS devices. Fig.1 shows the drain current versus bulk voltage. As illustrated, the maximum current is not while the bulk is connected to ground. The maximum current is while the bulk is connected to a higher voltage which is in contrast with FBB technique's normal behaviour.

In general for PMOS devices, when the bulk voltage increases, due to higher threshold voltage the drain current decreases. Fig.2 describes drain to source current versus bulk voltage in which, until bulk voltage is equal to Vbulk=50mV, the current increases afterwards it decreases by increasing the bulk voltage. As illustrated the maximum current is when the bulk voltage is Vbulk =59mV. Therefore the bulk voltage can be connected to this constant voltage to have a maximum current in the device. Table.1 shows the bulk voltage amount in which the current of circuit is at maximum.

As illustrated in Table 1, the FBB technique has different behaviors in some cases. This technique is somehow dependent to transistors sizing in some cases. Table 1, shows one example of this dependency. By increasing the PMOS size, the waveforms are changed. For higher W/L ratios, by increasing the bulk voltage the current decreases but for minimum size devices the opposite happens; the current increases by increasing the bulk voltage. Table 2, shows the effect of body bias on a NMOS device in 65nm CMOS technology. As it can be seen the effect of body bias at higher supply voltages, is different from lower supply voltages. At high supply voltage (e.g. VDD=0.9V), the maximum current does not occur at higher bulk voltages. It strongly depends on NMOS sizing.

For instance, in the SS corner for supply voltage equal to 0.9V, and T=27^{O}C for minimum sized transistor, maximum current occurs when the bulk voltage is connected to Vbulk=237mV, but by upsizing NMOS transistor, this voltage increases to VDD. As a result, for high size NMOS transistor, the FBB technique has a normal effect (i.e. higher bulk voltage gives higher drive current), but for lower size, this normal behavior is changed.

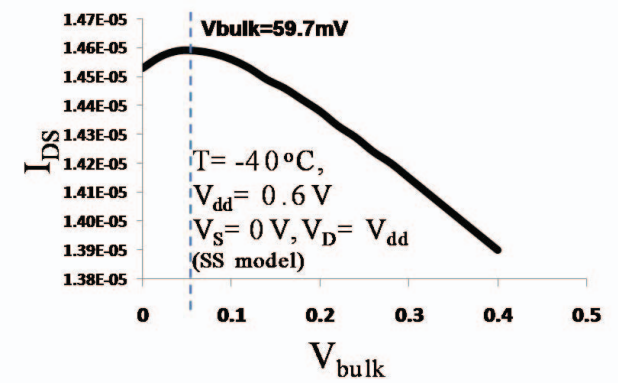

Fig.2. Drain current versus Bulk voltage

TABLE I. The Bulk Voltage Of PMOS In Which The Drain Current Is Maximum,For 65nm Technology(FBB)

Supply voltage	SS models			TT models			FF models		
Temp.	-40	27	110	-40	27	110	-40	27	110
0.9V	0.55	0	0	VDD*	0	0	0	0	0
0.8V	0.4	0.5	0	VDD	VDD	0	VDD	0	0
0.6V	80m*	90m*	98m*	0.5	0.4	0.37	VDD	VDD	0
0.4V	0	0	0	0	0	0	VDD#	VDD#	0
0.3V	0	0	0	0	0	0	0	0	0

* The minimum current is not at V_{bulk}=0

The optimum point is changed by increased W due to lower Narrow width effect

TABLE II. The Bulk Voltage Of NMOS In Which The Drain Current Is Maximum,For 65nm Technology(FBB)

Table2. The bulk voltage of NMOS in which the drain current is maximum									
Supply voltage	SS models			TT models			FF models		
Temp.	-40	27	110	-40	27	110	-40	27	110
0.9V	0	0	0	0	0	0*	199m#	237#	254#
0.8V	0	0	0	112m	186m	239m	469m	468m	464m
0.7V	0	0	0	0.5	VDD	VDD	VDD	VDD	VDD
0.4V	268m	366m	377m	0	VDD	VDD	VDD	VDD	VDD

* The minimum current is not at V_{bulk}=0

The optimum point is changed by increased W due to lower Narrow width effect

III. Adaptive Supply Voltage Circuit

The application of aggressive circuit design techniques which only focus on enhancing circuit speed without considering power is no longer an acceptable approach in most high complexity digital systems. The power consumed in high performance integrated circuits has increased to levels that impose a limiting factor on the system performance and functionality [13], [14]. Compared to a typical static gate, a domino logic gate operates at a higher speed and occupies less area while implementing the same function [15]. However, deep submicrometer (DSM) domino logic circuits utilizing low power supply and threshold voltages have decreased noise margins [13]. Fig.3. shows the proposed domino logic circuit using the adaptive supply voltage circuitry.

This circuit was designed to work at very low supply voltages (lower than Vdd=0.4V), so the drive current of NMOS transistors decreases significantly which in turn degrades the performance of the circuit. For footed domino logic circuit (Fig.3. with constant supply voltage), NMOS devices are upsized to overcome the performance degradation that in turn increases the area overhead and also dissipates more power. To illustrate how this adaptive supply voltage circuit works, Fig.4 is constructive. As it can be seen when Clk is low (Clk_bar="1", Precharge phase), the supply voltage node is connected to VDD. In evaluation mode (Clk_bar="0"), When all inputs are zero (idle mode), the supply voltage decreases to mitigate the power dissipation, but lowered supply voltage deteriorates the reliability and sensitivity to input noise because of reduced on-current through the PMOS keeper transistor to hold the dynamic node state. To overcome this problem in our design, the NMOS devices in the evaluation network are downsized. In ultra low supply voltages the current through NMOS transistor is lower than PMOS transistor in the same conditions. Also because of lowered supply voltage the DIBL is reduced significantly so the leakage current of NMOS transistor in idle mode is decreased significantly, but when at least one of the input signals is high, the supply voltage decreases to a level lower than Vdd/2 increasing the speed of evaluation. Also, lowering the supply voltage in this phase mitigates the contention between PMOS keeper transistor and NMOS evaluation network to hold the state of the dynamic node. This circuit is appropriate for OR-gates with less than four inputs. To use it for higher fan-in OR gates, three signals of all inputs to the adaptive supply voltage circuit might be used. Efficiency of this technique is strongly dependant of the input signals. When at least one of the selected input signals (applied signals to ASV) is at high level, the effect of ASV technique on reducing power consumption and improved speed is distinct. However, when all randomly selected signals applied to ASV circuit are zero, this circuit increases the area overhead and also the power consumption, but this degradation in power consumption is not significant. High fan-in gates are prone to failure due to very low Ion/Ioff ratio. For 2-input domino AND gate, due to three stacked NMOS transistors the probability of failure is very high. To avoid the failure NMOS transistors must be upsized significantly, that increases the area

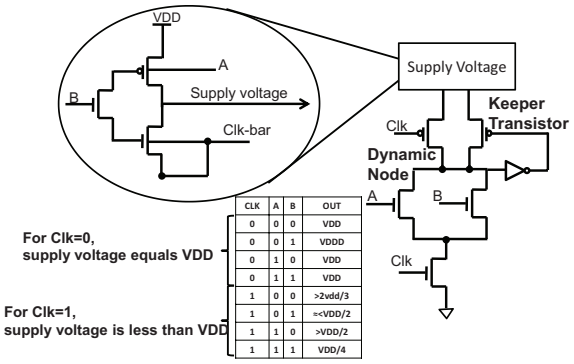

Fig.3. Proposed domino logic circuit

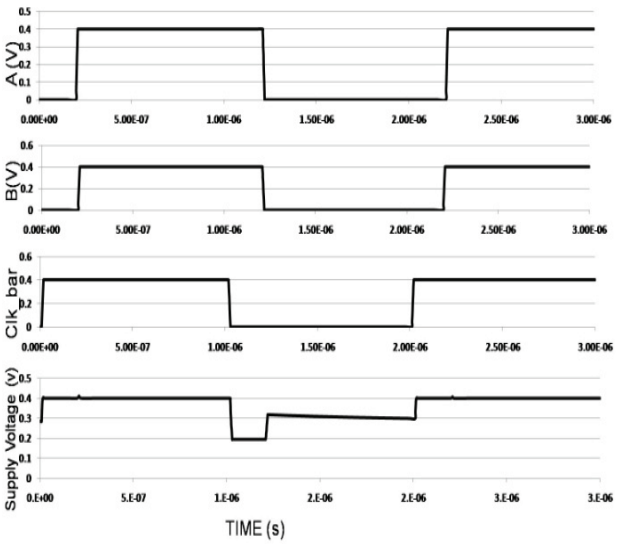

Fig.4. Waveforms of ASV circuit

TABLE III. POWER CONSUMPTION COMPARANCE (nW)

	FF			TT			SS			FS			SF		
	-40ºC	27ºC	110ºC	-40ºC	27ºC	110ºC	-40ºC	27ºC	110ºC	-40ºC	27ºC	110ºC	-40ºC	27ºC	110ºC
FDL	4.2	30.5	211	1.96	7.54	57.9	2.57	2.57	19.5	1.27	3.02	30.2	21.7	105	364
New Logic	8	39.5	156	1.53	9	49.4	0.51	2.65	17.5	0.82	4.4	26.7	0.73	3.7	26.3

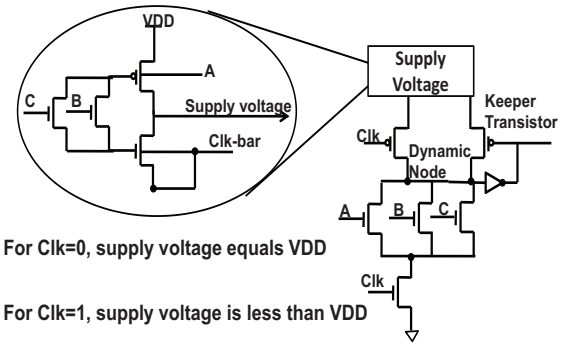

Fig.5. 3-inputs OR-Gate topology

overhead, but by applying this technique to the AND gate, when all inputs are high (A=1,B=1,Clk_bar=0), the supply voltage node is at the lowest rate which lets the evaluation network to discharge the dynamic node without any significant contention between the evaluation network and the PMOS keeper transistor. For higher fan-in (4-inputs OR-gate), two input signals are applied to the ASV circuit randomly. The probability that A or B is high, is 0.5. Then due to the significant effect of the ASV circuit to mitigate the power dissipation and also increasing the speed, this circuit is useful. This probability is lowered for higher fan-in. For wireless

network applications, using low fan-in gates (Fan-in=2) is usual. Therefore, in this case our proposed circuit has a higher speed and lower power dissipation.

Table 3 shows the results for power consumption of a 2-input OR gate for footed domino logic circuit employing the new logic circuit using adaptive supply voltage technique. As the results show, the power consumption decreases significantly while the new logic uses more transistors. Also, this technique enables domino logic circuit to work at ultra low supply voltages (subthreshold region), due to decreased contention between PMOS and NMOS transistors at the primary time of the evaluation phase. The delay of the proposed circuit does not increase in the same supply voltage (with the same size). In some cases the speed of domino logic using this technique increases. For higher fan-in gates, we can add NMOS transistor in parallel with input B in ASV circuit. The topology of 3-inputs domino OR-gate is illustrated in Fig.5.

IV. Write Cycle Improved SRAM Design

In this chapter we propose an adaptive circuit using body biasing effect to increase the write cycle speed of the SRAM circuit. Fig.6 shows the schematic of the proposed topology used in a SRAM design. Proper write operation depends on sizing the access NMOS to win the scaled fight with the PMOS inside the bitcell to write a "0". For a successful write, the bitcell becomes monostable, forcing the internal voltages to the correct values. If the cell retains bistability then the write does not occur, and the SNM is positive on the cell's butterfly plot. Thus, a negative SNM indicates a successful write (monostability in the cell) [10]. For ultra low voltage operation, the PMOS transistors are faster than NMOS (the same size) by an order of magnitude, and the write cycle speed decreases due to faster PMOS devices than access NMOS transistors. The best way to increase the write speed is upsizing the NMOS access transistors, but this in turn has an area overhead giving a deteriorative effect on READ and HOLD cycle. However if we use an adaptive supply voltage during the WRITE cycle that decreases the supply voltage to weaken the PMOS transistors, write evaluation is improved though it has no effect on READ and HOLD, because during the READ cycle and HOLD time the supply voltage is connected to VDD. As it can be seen in Fig.7, the supply voltage is changed due to DATA, WRITE, and WL signals. When WL="1" and WRITE is high, then supply voltage decreases to VDD/2 that enable us to decrease the supply voltage for SRAM design even more. This is because the most important constraint that limits designers to work in ultra low supply voltages is write failure due to contention between PMOS transistor and NMOS access transistors. To clarify this technique during the write cycle, dashed square in Fig.8, describes the comparance between the proposed technique and a 6T-SRAM cell with constant supply voltage.

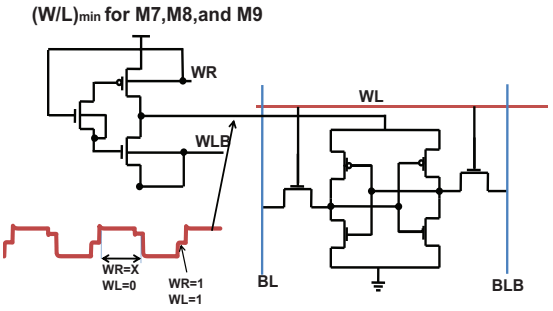

Fig.6. Proposed SRAM design

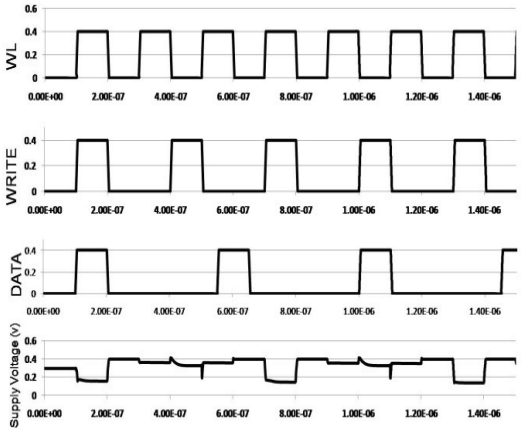

Fig.7. Supply voltage waveform

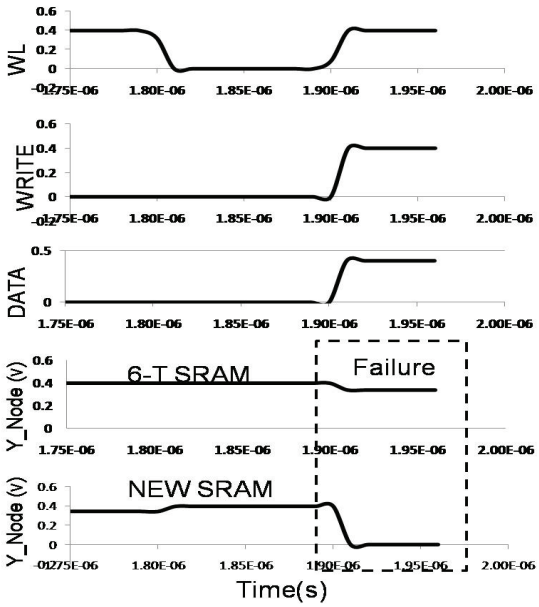

Fig.8. Comparison of the proposed technique with conventional 6T-SRAM cell during write cycle

V. CONCLUSIONS

In this paper a new technique based on the FBB technique is proposed. Using this technique, working at ultra low supply voltages is possible for high speed circuits like domino logic circuits. Also, due to the importance of SRAM in processor design, this technique was employed in SRAM design, significantly increasing the speed of write cycle with lower power dissipation due to lower supply voltages. In domino logic circuits, this technique extremely reduces the contention between PMOS (precharge transistor and keeper transistor) transistors and the evaluation network. It is thus not compulsory to upsize NMOS evaluation network to have a successful evaluation. Furthermore, the optimized bulk voltages were found giving a maximum speed for logic circuit designs.

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