

New Subthreshold Concepts in 65nm CMOS Technology

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Abstract

In this paper challenges observed in 65nm technology for circuits utilizing subthreshold region operation are presented. Different circuits are analyzed and simulated for ultra low supply voltages to find the best topology for subthreshold operation. To support the theoretical discussions different topologies are analyzed and simulated. Various aspects of flip-flop circuits are described in detail to study which topology would be most suitable for ultra low supply voltage and low-power applications. Simulation results show that the power consumption decreases by at least 23% compared with other flip-flops. Also, the setup time and the hold time are improved.

Keywords

Low-voltage, low-power, subthreshold, nanoscale

1. Introduction

In the last few years, large efforts have been made in research and development on low energy circuits for battery operated wireless sensor nodes. Recently a number of papers reporting ADC's utilizing time-domain instead of amplitude domain have been reported [1]-[4]. This class of converters may be built entirely of digital components, but this would put strict requirements on the comparator and sampling circuitry. To meet these requirements low power and high speed flip-flops with a sufficiently low possibility for metastability must be designed. Recently, as we approach atomic scale devices, leakage currents have increased dramatically, leading to higher static power dissipation. Therefore, leakage must be taken into consideration when evaluating these circuits since it has become a significant contributor to the overall power consumption in deep-submicron CMOS processes

Sub-threshold current rises due to lowering of threshold voltage which is scaled down to maintain transistor ON current in the face of falling power supply voltage. Voltage scaling for standby power reduction was suggested since both subthreshold current and gate current decrease dramatically (with V^4 for gate leakage) [5]. Lowering supply voltage thus saves standby power by decreasing both standby current and voltage [6]. The subthreshold region (weak inversion) is often utilized to implement power efficient circuits for ultra low power wireless applications, but due to the much lower current in subthreshold region compared with higher supply voltages, the evaluation speed of such circuits operating in weak inversion is decreased. Therefore, new techniques to improve circuit speed need to be developed.

The rest of the paper is organized as follows. In section 2, some characteristics of 65nm CMOS technology in weak inversion are described. Also the effect of some techniques in

subthreshold region is explained in details. In section 3, new flip-flop design concepts in 65 nm CMOS technology for operation in subthreshold region are proposed by improving upon existing designs. The comparison of results is also included in this section. Conclusions are presented in section 4.

2. Subthreshold 65nm characteristics

Subthreshold design has emerged as a good potential for ultra low power applications such as wireless sensor networks, medical instruments, and portable devices.

We have observed some specific behaviors from devices operating in subthreshold region in the 65nm technology due to lack of well-engineered models for subthreshold region. Short channel devices have been optimized for regular strong inversion circuits to meet various objectives such as high mobility, reduced DIBL, low leakage current, and minimal V_{th} roll-off. However, a transistor that is optimized for operating in superthreshold logics are not necessarily optimal in low voltage, low power dissipation applications designed for operation in the subthreshold region. Optimization problems include the transistor sizing, the drive current for PMOS and NMOS devices, the effects of some techniques such as Forward Body Bias (FBB), Reverse Body Bias (RBB), and stacking effects on threshold voltage and drive current. Although it would be ideal to have a dedicated process technology optimized for subthreshold circuits this is not practically achievable. In order to design optimal subthreshold circuits using CMOS devices that are targeted for superthreshold operation, it is crucial to develop design techniques that can utilize the side effects that appear in this new regime. However, in the absence of such a dedicated process the development of low voltage low power applications using the 65nm CMOS technology requires care and novelty in design.

2.1 DC Analysis

In this section three topologies for basic circuits are presented and simulated using DC analysis. Fig.1 illustrates the topologies that are simulated in 65nm technology with supply voltage equal to $V_{DD}=0.9V$. In all topologies minimum sizes for the transistors are used. Fig.1 (a) shows the three stacked devices (two PMOS and one NMOS referred to as 2PMOS). Fig.1 (b, c) are referred to as 3PMOS and 2NMOS respectively. Simulation results based on DC analysis for these three configurations are illustrated in Fig. 2. As it can be observed, the short circuit current in 2NMOS is higher than for the other circuits, which implies that the delay for 2NMOS is higher than for the other topologies causing increased short circuit current through this circuit.

2.2 Stacking effect in 65nm Technology

Stacking has been proposed as a technique to decrease the leakage current in subthreshold region [7]. This technique is based on increasing the threshold voltage of source to bulk as a result of which the threshold voltage will increase thereby reducing leakage current in idle mode. However, when the circuits are forced to work at ultra low supply voltage (subthreshold region), increased subthreshold current is desired to improve the circuits speed. In order to find better circuit topologies which use the stacking technique, two topologies which utilize the stacking effect are simulated.

As known, in CMOS technologies, the speed of the NMOS is higher than PMOS because of higher mobility of electrons compared with holes, but simulations show that for 65nm technology in ultra low supply voltages (in subthreshold), this behavior is changed. The main reason for this phenomenon is that these models are engineered for superthreshold circuits. For superthreshold applications, the threshold voltage of PMOS devices are lowered to compensate the effect of lower mobility compared to NMOS devices. But in subthreshold region, the exponential dependence of subthreshold current to V_{th} causes some unexpected results [8]-[10]. Fig.3 shows two topologies used to illustrate the stacking effect on speed. These two circuits were simulated for ultra low supply voltages ($V_{DD}=0.2V$) to investigate which is the faster topology. Two similar pulses are applied to the inputs of the circuits, and the charging and discharging speeds of the output nodes are considered and compared for Circuit1 and Circuit2, respectively. Fig.4 shows

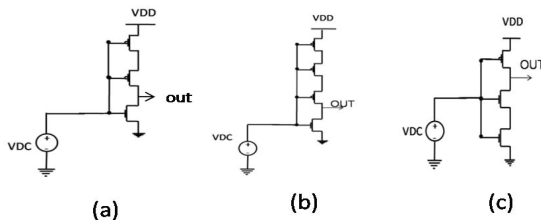


Figure 1: (a) 2PMOS (b) 3PMOS (c) 2NMOS circuits.

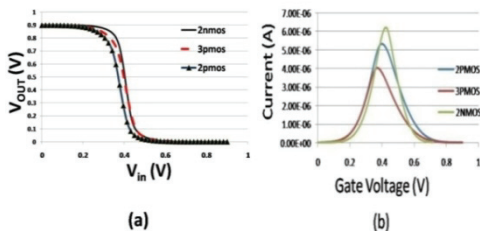


Figure 2: (a) V_{out} vs. V_{in} (b) I_{DS} current vs. gate voltage.

the simulation results for these two configurations, which show that Circuit1 has a higher speed compared with Circuit2 at ultra low supply voltages, so employing Circuit1 configuration in circuits such as D-Flip-flops instead of the Circuit2 topology, gives much better results. To attain the same speed for Circuit2, the NMOS transistors must be upsized 13 times, so the area overhead of Circuit2 is higher than Circuit1 in the same speed. Based on this concept the SAFF (Sense amplifier flip-flop) and the HLFF (Hybrid latch flip flop) are simulated using the complementary circuits of

the NMOS stacked transistors configuration. Results of simulation utilizing Circuit1 topology show that higher operating speeds are achievable at lower supply voltages as a result of which we attain significant reduction in power dissipation. Fig.5 shows the effect of body biasing technique on an inverter with different bulk voltages.

3. Flip-flops in subthreshold

3.1 Hybrid Latch Flip Flop

The Hybrid-latch flip-flop (HLFF) (Fig. 6), presented in [12] is one of the fastest structures presented. It also has a very small PDP [13]. The major advantage of this structure is its soft-edge property, i.e., its robustness to clock skew. One of the major drawbacks of the hybrid design in general is the positive hold time, discussed in Section II-B. Due to the single-output design, the power-consumption range of the HLFF is comparable with that of the static circuits. However, depending on the data pattern, the precharged structures can dissipate more than static structures for data patterns with more “ones”.

Hybrid design appears to be very suitable for high performance systems with little or no penalty in power when compared to classical static structures. As it can be seen in the HLFF circuit, there are stacked NMOS transistors that must evaluate the state of the circuit during the delay for three series inverters. As explained in the previous section, three stacked NMOS configuration has a lower speed than three stacked PMOS transistors in subthreshold region.

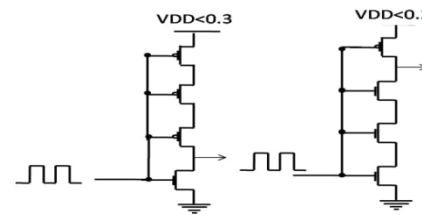


Figure 3: (a) Circuit1 (b) Circuit2 schematics.

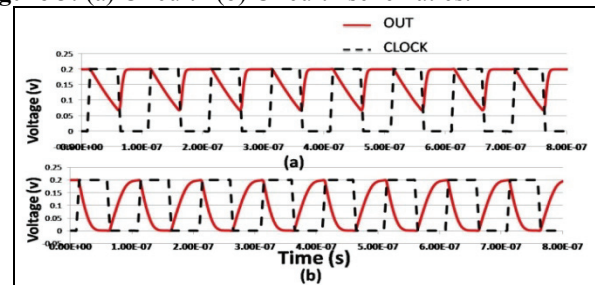


Figure 4: Transient analysis for (a) Circuit2 (b) Circuit1 (with minimum size for all transistors in 27°C, TT model).

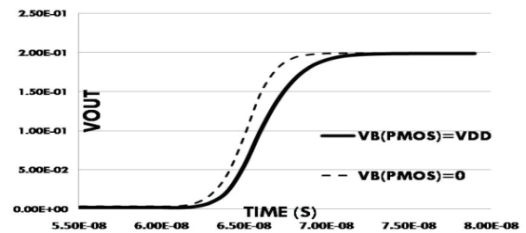


Figure 5: The effect of body biasing technique.

Simulations show that this circuit does not work for supply voltages lower than 0.4V. Fig.7 shows the results of simulations for HLFF at a supply voltage of 0.4V with higher size stacked NMOS transistors. When we reduce the supply voltage to 0.3V it causes some failures in corners. Fig.8 shows failure in output with two different inputs, due to many leakage paths and low active current. Due to the lower current in lower supply voltages, stacked NMOS transistors cannot discharge the related node.

Fig.9 shows the schematic of CHLFF (complementary hybrid latch flip-flop) for ultra low power applications. Because of employing PMOS stacked network, the speed of this circuit is higher. Also the technique of FBB is used to increase the speed of the PMOS network. After applying this technique the supply voltage may be reduced to 0.23V. Simulation results are shown in Fig.10. In this case the proposed circuit is working properly with an area which is two times less than its counterpart for supply voltages close to 0.27V (with two times lower total width compared with HLFF results in Fig.6).

Table 1 and 2 describe the results for HLFF and CHLFF at different supply voltages for five different corners. These results show that the HLFF is fast enough for higher supply voltages, but it fails for lower supply voltages. The HLFF circuit operates properly for VDD=0.4V but with high sized devices that increases the area overhead of this circuit significantly, so it makes it impractical for ultra low supply voltages. However the CHLFF is working as expected for supply voltage even lower than 0.3V and this ability makes this circuit employable in ultra low power applications. Simulations show that the CHLFF circuit has a much higher speed at higher supply voltages like 0.4V. For instance, at the SS corner at Temp=-40, Tc-q is as low as 930ps while HLFF has a Tc-q larger than 4.7ns with higher sized transistors.

FBB is the technique which may be used here to enforce the CHLFF to operate for even lower supply voltages as low as 0.2V. As mentioned in the previous section, for the PMOS transistors (Fig.6), increasing the bulk voltage from zero to VDD decreases the current through the device for supply voltages lower than 0.3V. Therefore, if this technique is applied in the proposed circuit combined with higher size devices, the proposed flip flop may operate at a supply voltage near 0.2V. As it can be seen in Table 4, the speed is increased but for the falling edge a lower speed is observed. It must be taken into account that the simulations are in the worst case. The HLFF cannot operate properly in some corners (like SS, T=-40), the lower supply voltage limit for the HLFF qualifying in all corners is 370mV given that very high sized devices are used.

3.2 Sense Amplifier Based Flip Flop

The sense-amplifier based flip-flop (SAFF), initially proposed in [14]-[15], is one of the most effective flip-flop available. It consists of a fast differential sense-amplifier stage, followed by a slave latch. Fig.11 shows the schematic of the SAFF circuit. The sense-amplifier stage can be seen as a latch whose sampling window closes as soon as the stage switches. This guarantees that the circuit is able to switch independent of circuit sizing. Furthermore SAFF gives near-zero setup time and reduced hold-time. The main drawback

of the SAFF proposed in [13]-[14] is the slave element, composed by a SR NAND latch. While this circuit requires a minimum number of transistors, it results in asymmetrical delays with slow high-to-low clock-to-output propagation. A high speed slave latch for the SAFF has been proposed by Nikolic *et al.* in [15]. In their design, there is a performance gain. However, it is achieved at the cost of having an increased number of transistors, with 16 MOS devices required by the output stage. For these designs, the main problem is operating in very low supply voltage and as a result the very low active current that causes failure in SAFF in some cases (medium size devices for stacked NMOS network).

As said in section 2, at ultra low supply voltages, stacked PMOS devices show a higher speed than stacked NMOS devices. Thus, a new complementary circuit for application in the SAFF circuit which is optimized for ultra low power applications is proposed.

Fig.12 shows the simulation results for the SAFF at low supply voltages. In order to operate well the SAFF must have high size NMOS transistors to evaluate the discharging nodes (S_bar and R_bar) that in turn decreases the Ion/Ioff ratio. Due to this lowered ratio, data retention in SAFF decreases significantly. For instance, when input D (CLK=low) is at low, because of leakage through high sized NMOS devices (dashed line path in Fig.11), it discharges the R_bar signal causing the Q signal switching to in zero.

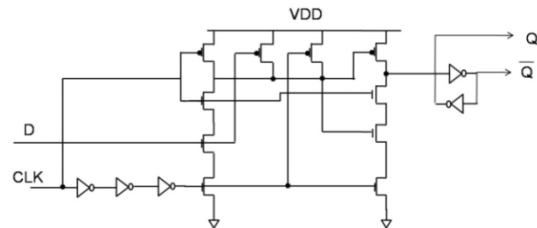


Figure 6: Hybrid Latch Flip-Flop.

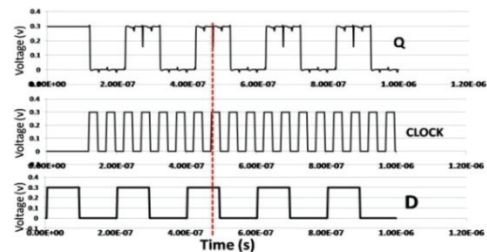


Figure 7: HLFF waveforms in VDD=0.3V, T=27°C (TT).

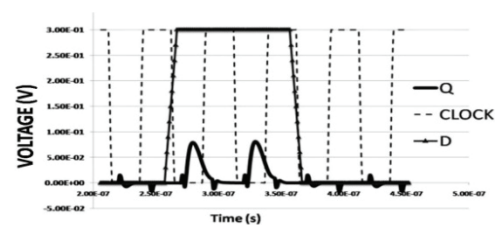


Figure 8: Failure in HLFF circuit.

Fig.13 shows the schematic of CSAFF for ultra low power applications. Simulations using 65nm standard CMOS models show that CSAFF has a much higher speed than SAFF and also it has the capability of working in ultra low supply voltage near 0.15V. Table 3 shows the delays (Tc-q)

for CSAFF. To compare with SAFF circuit, the CSAFF must be simulated for a higher supply voltage such as 0.4V. Simulations show that CSAFF has a lower delay (4-5 times) compared to the SAFF topology even at lower supply voltages.

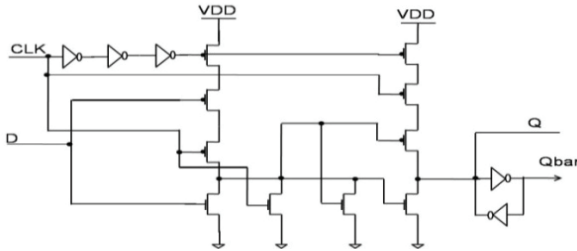


Figure 9: Proposed Complementary Hybrid Latch Flip Flop (CHLFF).

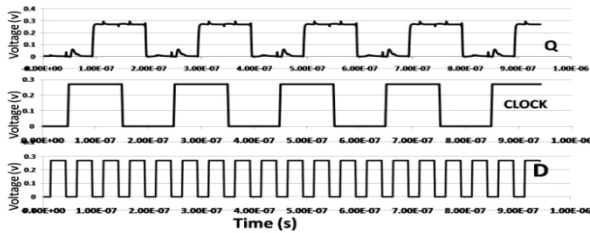


Figure 10: Output of CHLFF (TT model, T=27, VDD=270mV).

Table 1: Simulation results for HLFF (VDD=0.4V).

Temp	FF	SS	TT	SF	FS
110	TCQ=-210ps	610ps	280ps	310ps	160ps
	TDQ=24.19ns	26.88ns	26.55ns	26.58ns	26.43ns
27	300ps	1.39ns	710ps	950ps	640ps
	26.57ns	27.66ns	26.98ns	27.22ns	26.94ns
-40	440ps	4.73ns	1.22ns	1.44ns	1.7ns
	26.71ns	31ns	27.59ns	27.71ns	27.97ns

Table 2: Simulation Results for CHLFF (VDD=270mV).

Temp	FF	SS	TT	SF	FS
110	TCQ=59ps	442ps	320ps	1.1ns	500ps
	TDQ=38.81ns	39.19ns	39.07ns	40.21ns	39.75ns
27	300ps	1.28ns	712ps	400ps	1.124ns
	39.20ns	40.03ns	39.46ns	39.15ns	39.87ns
-40	730ps	7.28ns	1.794ps	1.1ns	6.159ns
	39.48ns	46.03ns	40.54ns	39.85ns	44.909ns

Table 3: Setup and Hold time for HLFF and CHLFF (VDD=0.3V, TT Model).

FLIP FLOP	T _{SETUP}	T _{HOLD}	T _{C=>Q} (Rising)
HLFF	1.3ns	750ps	1.81ns
CHLFF	450ps	950ps	1.3ns

Table 4 shows the simulation results for CSAFF compared with SAFF at VDD=0.3V, for standard 65nm CMOS models at room temperature. Although the CSAFF has a lower effective area than the SAFF circuit, the CSAFF shows better results for setup and hold times. Another drawback for SAFF at VDD=0.3 is its failure in slow corners (SS models, T=-40°C) while the CSAFF is working properly for supply voltages even less than 0.3V with a satisfactory performance. The FBB technique was also applied to the CSAFF by connecting the bulks of the stacked PMOS network (shown with dashed lines in Fig. 13) to ground which helps to increase the speed of the circuit by 1.2 times.

This technique also works for supply voltages near 0.25V by applying the bulk voltage. In this paper we showed that due to the higher drive current for PMOS it is more useful to use a PMOS as evaluation network for some kind of topologies such as FFs, domino logic circuits, and even SRAM design. As an example, due to lower drive current of NMOS than PMOS, using a PMOS network to evaluate write cycle would be more useful. As we showed due to simulations, stacks of NMOS have a lower speed than PMOS stacks.

4. Conclusions

The main reason we find that sub-Vt current is higher for PMOS than NMOS is that often PMOS are designed to have lower |Vt| (which is set by designing the threshold adjust implant of the devices). Above Vt, this helps to compensate their lower mobility, resulting in nearly equal NMOS/PMOS drive; but, in sub-Vt, it results in over compensation due to the stronger dependence of drive current on Vth.

An additional factor might be that, typically, PMOS devices have higher channel doping concentration. As a result, their channel depletion region in sub-Vt is thinner, and therefore results in larger depletion capacitance. As a result, the gate voltage, which affects the channel voltage through a Cox-Cdepletion capacitor divider, has more effect on the channel voltage, possibly resulting in greater transconductance. Based on these results, in this paper, a few design challenges for ultra low supply applications in 65nm CMOS technology were presented. Also we employed body biasing and stack effect techniques for flip flop designs for ultra low power applications. Simulation results showed that the setup time for CHLFF is improved by 65% but the hold time is degraded by 12% compared with HLFF design. However the speed of CHLFF is improved by 3 times compared to the HLFF topology. In CSAFF the speed of circuit is improved by 2 times for high to low of output. Also the effective area of this circuit is 3 times lower than SAFF.

Table 4: Simulation results for CSAFF.

Temp	FF	SS	TT	SF	FS
110	TCQ=- 230ps	1.18ns	340ps	10ps	570ps
27	620ps	4.32ns	1.87ns	1.46ns	2.3ns
-40	1.99ns	17.24ns	6ns	5ns	8.05ns

Table 5: Results for CSAFF and SAFF in VDD=0.3v (T=27°C, TT Models).

FLIP FLOP	T _{SETUP}	T _{HOLD}	T _{C=>Q}
SAFF	250ps	1.25ns	2.13
CSAFF	420ps	-210ps	1.6ns

Table 6: Results for FFs.

D-Flip Flop	Power consumption (x 10 ⁻⁷)	W x L
SAFF	2.22	8.28(um ²)
CSAFF	1.44	3.76(um ²)
HLFF	2.07	8.52 (um ²)
CHLFF	1.59	6.9 (um ²)

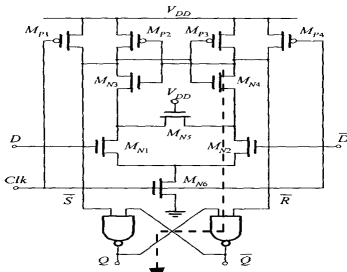


Figure 11: Sense amplifier-based flip flop circuit [16].

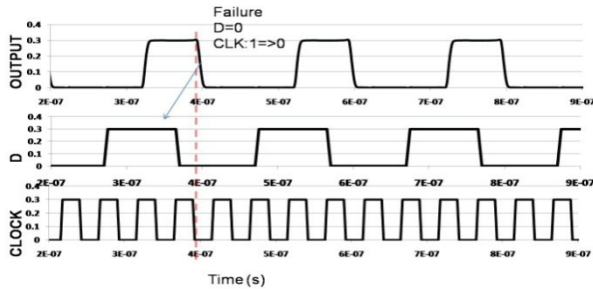


Figure 12: Failure in SAFF.

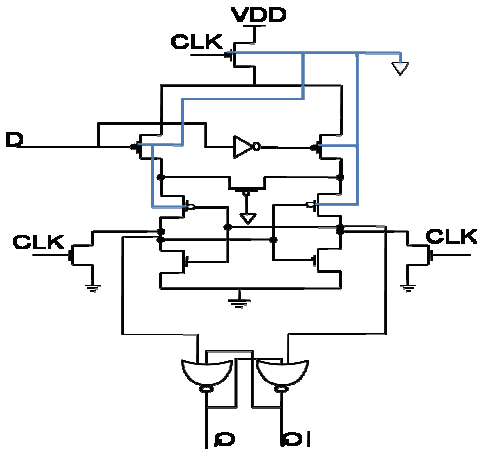


Figure 13: Schematic of CSAFF circuit.

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