Self-Precharging Flip-Flop (SPFF): A New Level Converting Flip-Flop

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Abstract

Clustered voltage scaling scheme is an effective method of power consumption reduction without performance degradation. One of the main issues in this scheme is performance and power penalties due to insertion of level converting flip-flops at the interface from low-supply to high supply clusters to simultaneously perform latching and level converting functions. A new level converting flip-flop, called Self-Precharging Flip-Flop (SPFF), is proposed that outperforms conventional level converting flip-flops in terms of performance and power-delay product. It is a pulsed flip-flop that employs conditional capturing and self-precharging techniques to efficiently perform latching and level converting functions. Based on simulation results in a 0.25μm CMOS technology, the proposed flip-flop exhibits up to 60% delay reduction and 35% improvement in power delay product as compared to conventional level converting flip-flops.

1. Introduction

Supply voltage (V_{DD}) reduction is very effective in reducing power consumption of CMOS circuits, however it is at the expense of the circuit delay. In order to lower the supply voltage without system performance degradation, Clustered Voltage Scaling (CVS) has been developed in which critical and noncritical paths of the design are clustered [1]. Since the speed requirements of the noncritical paths are lower than the critical paths, supply voltage of noncritical path clusters can be lowered without degrading system performance. Whenever an output from a low V_{DD} (V_{DDL}) cluster has to drive an input to a high V_{DD} (V_{DDH}) cluster, level conversion is required at the interface. To reduce the overhead of the level conversion, low V_{DD} clusters are followed by pipeline flip-flops and the level conversion is merged into the flip-flops [1]. These flip-flops, which simultaneously perform latching and level shifting, are called level converting flip-flops. The performance and power consumption of the level converting flip-flops are very critical in the effectiveness of the CVS schemes. The clock and data inputs of a level-converting flip-flop have low voltage swing of V_{DDL} and the output has high voltage swing of V_{DDH}.

The level converter can be merged to the slave part of a master slave flip-flop, which results in the Slave Latch Level Shifting (SLLS) flip-flop proposed in [1] and shown in figure 1-a. The master latch operates with the low supply (V_{DDL}) and the level converter is power by the high supply (V_{DDH}). This scheme suffers from large delay especially when V_{DDL} is much lower than V_{DDH}. The other proposed level converting flip-flop is Clock-level Shifted Sense Amplifier (CSSA) flip-flop, shown in figure 1-b [1]. The problem with low swing data and clock is that they cannot drive PMOS transistors of the flip-flop, which are supplied by V_{DDH}. In order to resolve this problem the clock signal is level-shifted up to V_{DDH} and applied to the PMOS precharge transistors of a sense amplifier flip-flop [2] to enable correct precharging operation. Data is applied to the NMOS transistors of the flip-flop, and therefore does not need to be level-shifted. The main problem of this scheme is that level shifting of the clock signal, which is always switching, can be very energy consuming especially when the clock signal has a very low voltage swing. CSSA uses cross-coupled NAND gates as the set-reset latch that results in unsymmetrical output delays and limits the performance of the flip-flop [2].

Pulsed flip-flops are faster than master slave and static flip-flops [3]. By employing internal clock gating (conditional capturing) [4] it is possible to statistically reduce their power consumption, especially at low data switching activities, by removing redundant internal switching transitions. In this way pulsed flip-flops can show better performance and power-delay products than static flip-flops and this makes them the only choice for critical paths of a design. Unfortunately, the pulsed flip-flops cannot operate with low swing data and clock inputs since in these flip-flops data or clock drives PMOS transistors especially for the precharge operation. Applying level shifting on the clock signal, as used in the CSSA, is not power and performance efficient for very low clock swings.

We propose a new level-converting flip-flop called Self-Precharging Flip-Flop (SPFF), which is a pulsed flip-flop that employs a self-precharching technique to precharge its dynamic node. This removes the need for the clock signal to drive PMOS precharge transistors.

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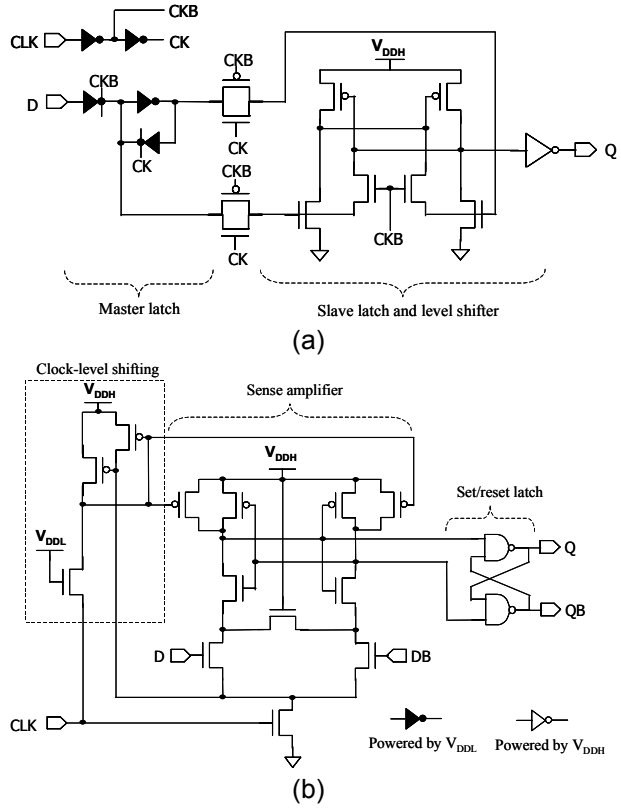

Figure 1. Conventional level converting flip-flops: (a) Slave Latch Level Shifting flip-flop (SLLS) (b) Clock-level Shifted Sense-Amplifier flip-flop (CSSA)

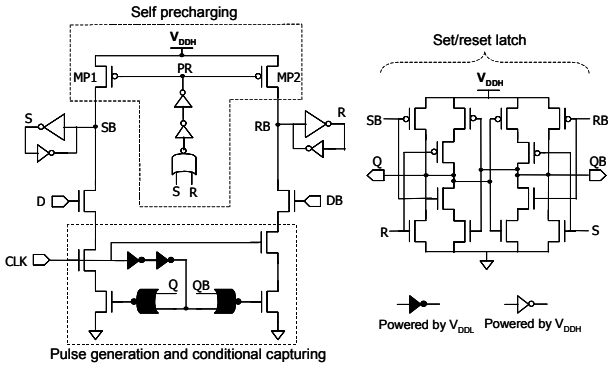

Figure 2. Self-precharging flip-flop (differential)

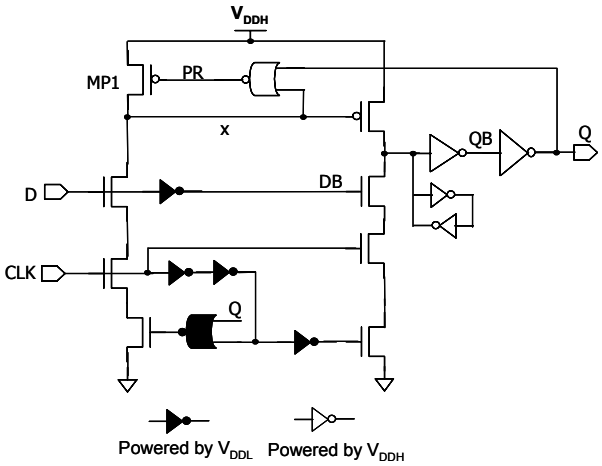

Figure 3. Self-precharging flip-flop (single-ended)

The self-precharging circuit automatically returns the flip-flop to the precharge mode after enough time has been allowed for the input data to propagate and get latched to the output. This flip-flop also incorporates conditional capturing technique [4] to remove redundant internal transitions when the input data is calm.

2. Self-Precharging Flip-Flop

The schematic of the self-precharging flip-flop is shown in Figure 2. It is composed of two stages. The first stage is a sampling circuit detecting the voltage at the input during a pulse window implicitly generated on the rising edge of the clock. During the sampling window, the state of the input is captured to the dynamic nodes (RB and SB) and then stored in the second stage, which is a set-rest latch. Conditional capturing capability has been incorporated by using a feed back from the outputs through the NOR gates that drive the lowest NMOS transistors in the sampling paths. This helps in getting rid of redundant transitions from the dynamic nodes resulting in statistical power saving based on the data switching activity. The amount of power saving achieved by this internal clock gating is larger than the incurred power overhead for relatively low data switching activities. However, for high data switching activities the conditional capturing may not be of benefit since there is less chance to gate the clock and prevent redundant internal switching. The order of the transistor stack in the sampling path is based on the arrival time of the signals. The data input, which is the latest arriving signal, drives the transistor closest to the output node. This ordering increases the performance of the flip-flop and allows more negative setup time. Negative setup time provides soft clock edge property, which is powerful in eliminating clock skew and jitter from timing budget in critical paths [5]. The second stage of the flip-flop is a modified set-reset latch proposed in [2]. The main feature of this set-reset latch is that it balances the delay from D to Q and QB and has a good driving capability.

The precharge transistors (MP1 and MP2) are derived by a self-resetting circuit providing the self-precharging capability to this flip-flop. If any discharge happens on either of the dynamic nodes, it is detected by the NOR gate and a reset pulse (node PR in figure 2) is generated. The reset pulse is applied to the precharge transistors (delayed through the inverters) to precharge SB and RB to V_{DDH}. When the precharge operation is done, the precharge transistors are turned off again and SB and RB are kept charged by the cross-coupled inverters. Then the flip-flop is ready for data sampling at the next rising edge of the clock. The delay of the self-precharging circuit should be long enough to allow the input data to propagate and get latched to the output. This condition can be easily satisfied by using minimum sized transistors for the NOR gate and inverters in the self-

precharging circuit and skewing them in proper directions. Figure 3 shows the single ended version of the self-precharching flip-flop. If the dynamic node (X) is discharged, the output goes high and the precharge transistor (MP1) is turned on and recharges the dynamic node. During the rest of the clock cycle, the NOR gate and MP1 act like an inverter and a keeper and therefore keep the node X charged. If the output goes high due to a discharge on X, the feed back from the output to the sampling path turns off the sampling path so that the self-preharging operation does not cause any short circuit power consumption. In this flip-flop data and clock can have any voltage swing and the level conversion occurs on the dynamic nodes (X, RB, and SB). Another benefit of the self-precharging technique is that it reduces the clock load and reduces clock power. Moreover, the switching activity of the self-precharging circuit is dependent on the data switching activity, which tends to be much less than the clock switching activity. Therefore, for moderate and low data switching activities the power overhead of the self-prechrging circuit is mitigated by the saving from the clock power.

Figure 4 shows the simulated waveforms of the flip-flops. The waveforms are obtained by HSPICE simulations of the flip-flops using typical models of a 0.25µm CMOS technology at 25°C with V_{DDH}=2.5V and V_{DDL}=1.75V and an output load of 30fF. As observed, the delay from the clock to the precharge signal (PR) is long enough so that prechrging happens after the input data is completely latched. There are no internal transitions at the next rising edge of the clock since the input data has not changed.

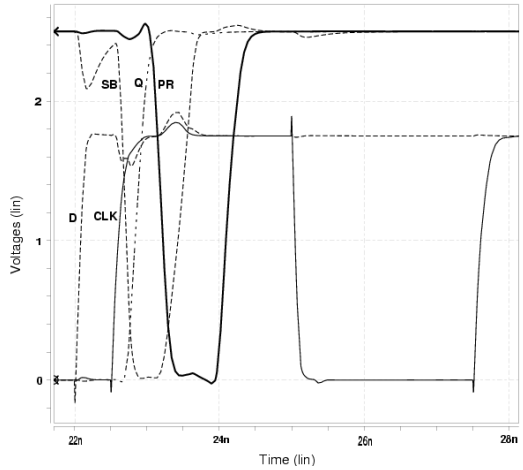

Figure 4. Simulated waveforms (a) differential SPFF (b) single-ended SPFF

3. Simulation results and comparisons

The delay metric for flip-flops is defined as the minimum data to output (D-Q) delay, which includes both setup time and clock to output (CLK-Q) delay [6]. The conventional level converting flip-flops and the proposed flip-flops are designed and optimized in a 0.25µm CMOS technology. For noncritical transistors minimum sizes were used and critical transistors were optimized to minimize the power delay product of the flip-flops. The optimizations were done at V_{DDH}=2.5V, V_{DDL}=0.7×V_{DDH}=1.75V, 25°C, output load of 30fF, data switching activity of 50%, and clock frequency of 200MHz. The load power was excluded to get the net power of the flip-flops. Then V_{DDL} was swept from V_{DDH}=2.5V down to 0.5×V_{DDH}=1.25V and power and delay of the flip-flops were measured. For a fair comparison, single ended and differential flip-flops are compared separately. Figure 5 shows delay comparisons of the flip-flops at different V_{DDL} voltages. Both single-ended and differential SPFF's show superior performance as compared to their conventional counterparts. The performance improvement mainly attributes to the dynamic nature of the flip-flop. Figure 6 shows comparisons of the Power-Delay Products (PDP) of the flip-flops at different V_{DDL} voltages. SPFF's also show better PDP than their conventional counterparts. The PDP increase at very low V_{DDL} is because of large delays at low V_{DDL} voltages.

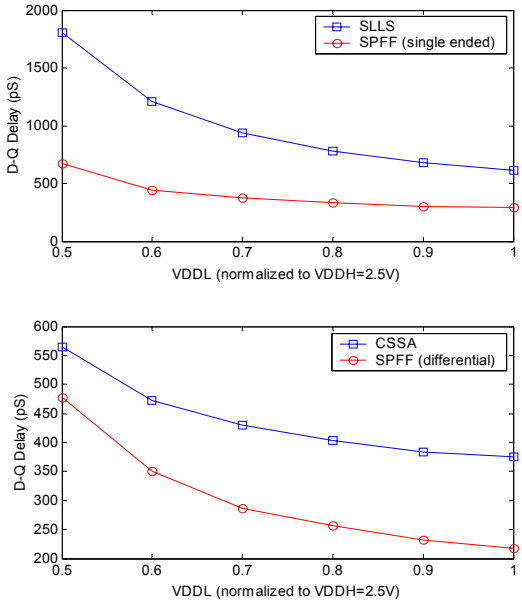

Figure 5. Delay versus VDDL

Table 1. Flip-flop characteristics (VDDH=2.5V ; VDDL=1.75V ; Output load=30fF ; Clock frequency=200MHz; Data switching activity=50%)

Flip-Flop	Transistor count	D-Q delay (pS)	Setup time (pS)	Power (uW)	PDP (fJ)	Ratio
CSSA	21	430	-68	86.4	37.2	1
SPFF (differential)	48	287	-130	108.9	31.3	0.84
SLLS	26	938	298	38.3	35.9	1
SPFF (single-ended)	32	372	-53	63.1	23.5	0.65

Figure 7 shows PDP of different flip-flops versus data switching activity. The single-ended SPFF shows better PDP at all switching activities than the SLLS flip-flop. Compared to the CSSA, the differential SPFF shows better PDP at data switching activities less than 70%; however, it does not show better PDP for higher data switching activities. It is because of the fact that the power overhead of the internal clock gating (conditional capturing) employed in the SPFF can only be mitigated at low and moderate data switching activities. Conditional capturing saves some energy by removing redundant transitions of the internal nodes when the input data is calm. However, at high switching activities there are not enough redundant transitions to be removed; and therefore, the power overhead of the internal clock gating cannot be mitigated. Table 1 shows some numerical results for different flip-flops. Differential SPFF shows 33% delay reduction and 16% PDP improvement compared to CSSA. Single ended SPFF shows 60% delay reduction and 35% PDP improvement compared to SLLS. The simulation results verify that SPFF is a better level-converting flip-flop for critical paths in clustered voltage scaling designs. This flip-flop can also operate very well for low swing clocking schemes.

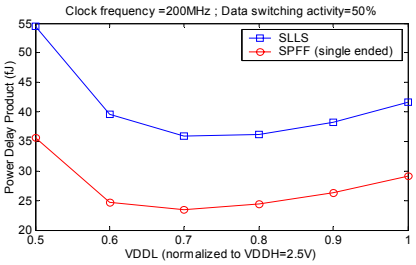

Figure 6. PDP versus VDDL

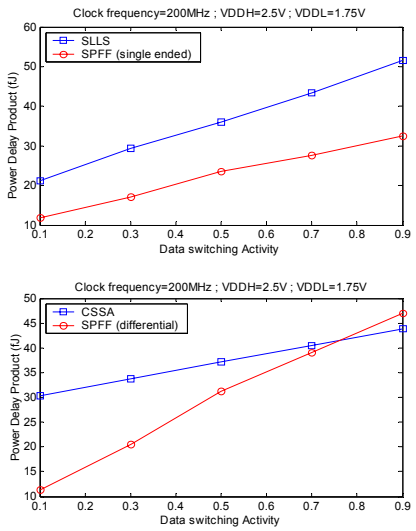

Figure 7. PDP versus data switching activity

4. Conclusion

We proposed the self-precahrging flip-flop, which is a pulsed flip-flop that incorporates self-precharging and conditional capturing to efficiently perform latching and level converting functions. It outperforms conventional level converting flip-flops in terms of performance and power delay product and is well suited for level conversion for critical paths in clustered voltage scaling designs.

5. References

[1] M. Hamada, *et al.*, "A top-down low power design technique using clustered voltage scaling with variable supply-voltage scheme," *Custom Integrated Circuits Conf.*, pp. 495–498, 1998.

[2] B. Nikolic, *et al.*, "Improved sense-amplifier-based flip-flop: design and measurements," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 876–884, June 2000.

[3] J. Tschanz, *et al.*, "Comparative delay and energy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microprocessors," *International Symp. on Low Power Electronics and Design*, pp. 147–152, 2001

[4] B. S. Kong, *et al.*, "Conditional-capture flip-flop for statistical power reduction," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1263 –1271, Aug. 2001.

[5] H. Partovi, "Clocked storage elements," in Chandrakasan, *et al.*, Design of High-Performance Microprocessor Circuits. IEEE press, Piscataway NJ, 2000, 207-234.

[6] V. Stojanovic, *et al.*, "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 536–548, April 1999.