65NM SUB-THRESHOLD 11T-SRAM FOR ULTRA LOW VOLTAGE APPLICATIONS

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ABSTRACT

In this paper a new ultra low power SRAM cell is proposed. In the proposed SRAM topology, additional circuitry has been added to a standard 6T-SRAM cell to improve the static noise margin (SNM) and the performance. Foundry models for a 65 nm standard CMOS process were used for obtaining reliable simulated results. The circuit was simulated for supply voltages from 0.2V to 0.35V verifying the robustness of the proposed circuit for different supply voltages. The simulations show a significant improvement in SNM and a 4X improvement in read speed still maintaining a satisfactory write noise margin compared with the 6T-SRAM cell. The proposed circuit has an area overhead between 22%-28% compared with the 6T-SRAM.

KEYWORDS: SRAM, ULTRA LOW POWER DESIGN, Static Noise Margin

I. INTRODUCTION

PROBLEMS arising from technology scaling have recently made power reduction an important design issue for circuits and applications that traditionally are driven almost solely by performance constraints. The increased importance of power is even more notable for a new class of energy-constrained systems [1, 2]. Supply voltage scaling has been proposed for low-voltage/low-power digital designs. Supply voltage scaling is a well known method to reduce the power consumption of a circuit. The leakage is reduced due to smaller voltage differences between the drain, source and body of a transistor [3, 4]. Scaling the supply voltage decreases the power consumption, but increases the delay of circuit. Therefore the threshold voltage are reduces to reduce the circuit delay. In order to satisfy the performance requirements demanded by applications, like wireless sensor networks (WSN), the threshold voltage (*V*th) should also be lowered, to have both low power operation and satisfactory performance. However, there is a cost of higher static power dissipation due to large leakage currents [1].

Subthreshold circuit design involves scaling the supply voltage below the threshold voltage, where load capacitances are charged / discharged by subthreshold currents. In subthreshold region, the active current is defined by:

$$I_{sub} = I_0 e^{\frac{V_{GS}-V_T+\eta V_{DS}}{nV_{th}}}\left(1 - e^{\frac{-V_{DS}}{V_{th}}}\right) \quad (1)$$

$$I_0 = \mu_0 C_{ox}\frac{W}{L}(n-1)V_{th}^2 \quad (2)$$

where n is the subthreshold slope factor ($1+C_d/C_{ox}$), and V_{th} equals kT/q. The subthreshold propagation delay with a load capacitance C_g is thus defined as [5]:

$$t_d = \frac{KC_gV_{DD}}{I_0 e^{(V_{GS}-V_T)/nV_{th}}} \quad (3)$$

where K is the delay fitting parameter. As shown by Eq. 3, the speed of circuits operated in subthreshold region is proportional to the supply voltage. When VGS=VT, the propagation delay has an inverse dependence to I_0, so by changing temperature, device sizing, VGS, and the physical parameters, the propagation delay is changed. Equation (1) shows that lowering VDD will produce a proportional reduction in subthreshold current degrading the performance. At very low VDS values, the parenthetical term produces a more pronounced roll-off in subthreshold current [5].

The most important concern in subthreshold region is the low ON current (referred as Ion). To increase the subthreshold current, upsizing is one option. Upsizing the transistors will however increase the parasitic capacitances and in some cases (like for SRAM) cause failures [4]. Fig. 1 shows Ion (VGS=VDD) and Ioff (when VGS=0) for different processes corners. As illustrated in Fig. 2, the ratio between Ion and Ioff is small for such a low supply voltage. In the 65nm

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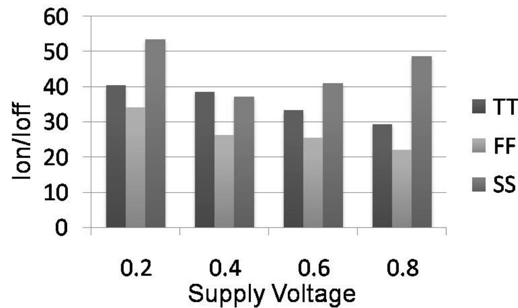

Fig. 1. Ion/Ioff ratio for different supply voltages

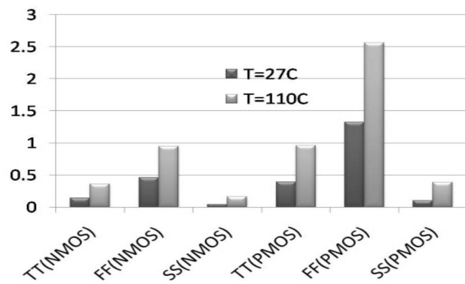

Fig.2. Comparison Ion current for PMOS and NMOS

technology an unusual behavior is observed for specific supply voltage ranges. For minimum length devices, at low supply voltages, the PMOS current level is higher than an order of magnitude more than that for the NMOS. This is illustrated in Fig. 2. Due to the significant reduction in evaluation current in both NMOS and PMOS, subthreshold circuits are usually impractical in high speed applications, but for some applications like wireless sensor networks design, it is not necessary to have a high sampling frequency. In another words, the most important concern in WSN applications is to minimize the power consumption. As a result the frequency must be reduced to get correct evaluation. The low Ion causes some problems in SRAM design. SRAMs comprise a significant percentage of the total area for many digital systems as well as the total power consumption, so SRAM leakage can dominate the total leakage of a chip. If the SRAM leakage power is reduced, the total leakage power of the system will then decrease. Pushing SRAM in subthreshold region reduces the leakage power significantly but it degrades the SNM of SRAM in read and write cycles due to lower read current and also the effect of BDGO (breakdown gate oxide) of NMOS transistors in SRAM circuit.

II. 6T-SRAM CIRCUIT

Fig. 3 shows the standard 6T-SRAM cell. In this circuit, storage nodes are specified by X, Y. Suppose that node X stores “0” and node Y stores “1”. Due to low supply voltage, leakage sources are important. The leakage sources are shown in Fig. 3. In this case, M1, M4 are turned on. Also, M2 and M3 are turned off. During the hold time, when WL is not selected (idle mode), M5 and M6 are turned off. In idle mode, M5 and M2 give a small rise on node X because of leakage currents, so node X has a low voltage in range of few millivolt (instead of zero) that causes an increase in leakage through M3 potentionally introducing failures [6].

When WL is selected (Read cycle) M6 is turned off and M5 is turned on. In this case, the read cycle is done through M5 and M1, but a rise in node X due to stacking effect [7] causes more leakage through M3. This causes a drop in the voltage of node Y, so the read cycle speed is degraded and in some cases it flips the data on storage nodes. To improve the speed of the read cycle, the best way is upsizing M1 and M5, but there are some limitations on increasing sizes of transistors. Fig. 4 shows the effects of upsizing on read noise margin in 6T-SRAM cell. As it can be seen from Fig. 4, by increasing the ratio of WM1/WM5, discharging BL is faster, but due to the upsizing of these devices the voltage of node X is increased which increases the leakage current through M3 and then discharges node Y more causing an increase in the leakage through PMOS that is higher than NMOS in 65nm CMOS technology for ultra low supply voltages.

As Fig. 4 shows, smaller sizes for NMOS transistors cause lower speed but in this case the reliability of the cell is higher. For larger device sizes in the read path, the reliability is lower but the speed is improved.

Another concept that is important in SRAM design is static noise margin (SNM) [8, 9]. SNM quantifies the amount of voltage noise required at the internal nodes of a bitcell to flip the cell's contents [5, 10]. In 65nm, due to the different behavior in sub-Vt (PMOS is stronger than NMOS by an order of magnitude with minimum length) SNM is more affected. Fig. 5 shows the output of an inverter versus the input voltage. To balance the devices the NMOS must be upsized by an order of magnitude larger than PMOS. This problem is more challenging during the write cycle where stronger access NMOS transistors are needed.

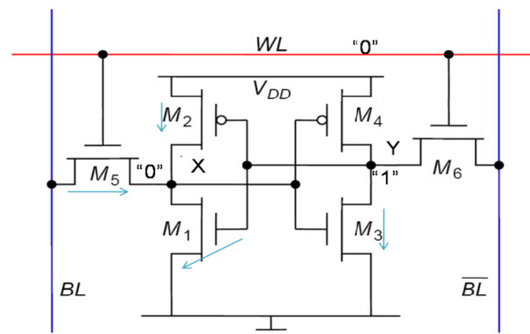

Fig.3. 6T-SRAM cell

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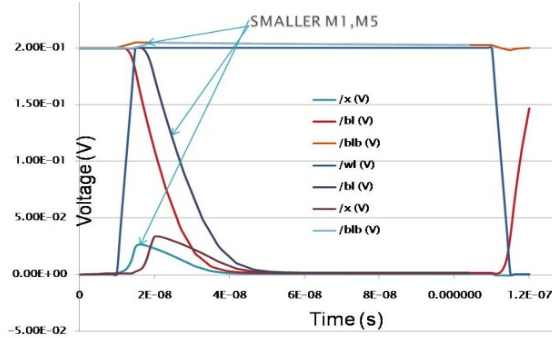

Fig. 4. Output waveforms for 6T-SRAM cell

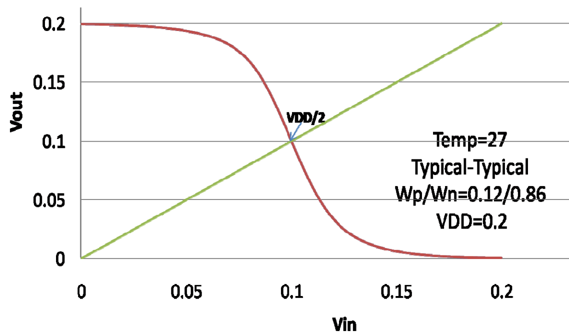

Fig.5. an inverter output in 65nm

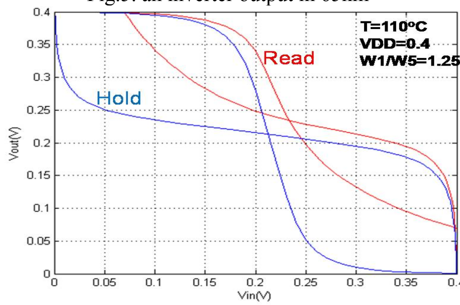

Fig. 6. SNM for HOLD and READ in 6T-SRAM (VDD=0.4)

At the onset of a read access, the wordline is “1” and the bitlines are precharged to “1”. The internal node of the bitcell that represents a zero gets pulled upwards through the access transistor due to the voltage dividing effect across the access transistor and drive transistor, which degrades the read SNM. Fig. 6 shows the butterfly curves during the hold and read cycles for VDD=0.4V illustrating the degradation in SNM during read.

As illustrated, the read noise margin is degraded at low supply voltages. Due to increased leakage through the transistors, especially PMOS, at higher temperatures, read noise margin is more decreased. Fig. 7 shows SNM versus WM1/WM5 for different temperatures (27°C and 110°C) for TT CMOS models. To improve the SNM in subthreshold region, an 11T-SRAM design is proposed. In this circuit, the read line is distinct from the write wordline as proposed in [11].

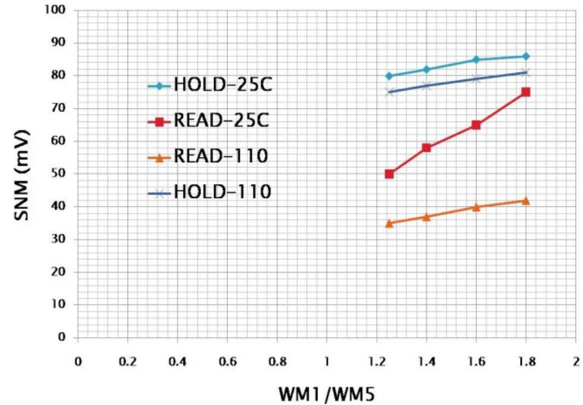

Fig. 7. SNM versus WM1/WM5 for different temperatures.

III. SUBTHRESHOLD 11T-SRAM

Fig 8 shows the schematic of the proposed 11T-SRAM bitcell. Transistors M2, M4, M5, and M6 are identical to 6T-SRAM, but two transistors M1 and M3 are downsized to the same size as the PMOS transistors. The bitline and wordline are distinct from the write wordline. In this case, memory can have distinct read and write ports. During the hold time, RDWL and WL are not selected. In the 6T-SRAM part, suppose that node Y stores “0” and node X stores “1” as was described for the 6T-SRAM part in the previous section. For the added circuitry the following behavior is observed when transistor M12 is turned off. Also the M11 state is dependant of the voltage in node Y. If node Y stores “1”, then M8 connects the gate of M11 to ground so M11 is turned off. However if node Y stores “0”, M9 is turned off and it starts to charge the gate of transistor M11. Therefore there is a leakage path through M11 that connects the node YN to zero. Minimum size transistors were used for the added 5T-circuitry, except the access transistor that has a larger size. The most important part of the 11T-SRAM is a boost capacitor (CB) that connects source of M9 to RDWL.

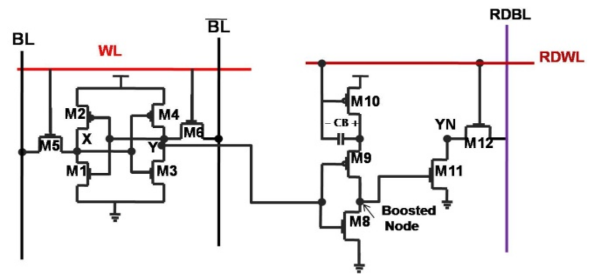

Fig. 8.proposed 11T-SRAM cell

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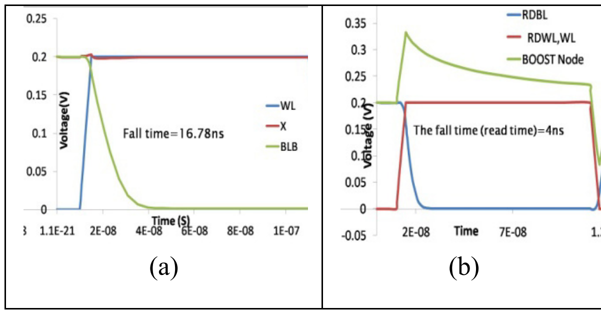

Fig.9. Output waveforms during read a. 6T-SRAM b. 11T-SRAM

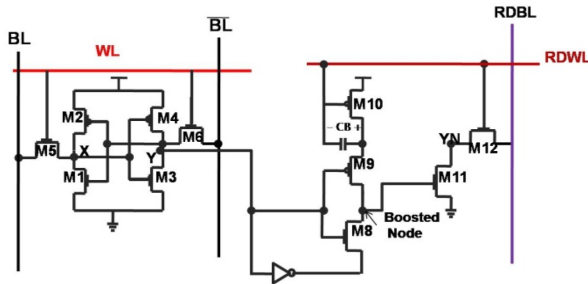

Fig. 10. Modified 11T-SRAM (13T-SRAM)

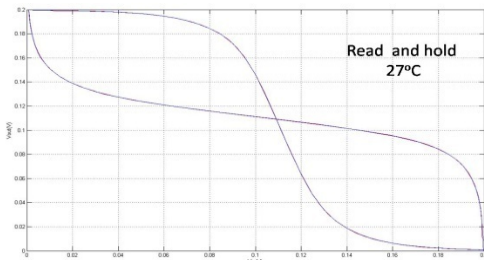

Fig.11. Butterfly plot for 11T-SRAM

Assume that the node Y has stored "0". During the hold and write times, RDWL is connected to zero, so CB starts to be charged to VDD but transistor M9 does not let CB charge to VDD. Simulations show that it is charged to VDD/2, but due to the minimum size of M9 it is floating. Thus the gate of M11 is connected to a voltage almost less than VDD/2 that discharges the YN node to ground slowly. When RDWL is selected, the source of M9 rises to 1.5VDD connecting the gate of M11 to a voltage higher than VDD. This increases the read current by an order of magnitude compared with the 6T-SRAM cell. Fig. 9 shows the output waveforms of the 11T-SRAM and the 6T-SRAM. As illustrated, the read time is decreased by more than 4X compared with the 6T-SRAM cell.

In the other case, when node Y stores "1", M8 is turned on and connects the boosted node to ground. This turns off M11 that causes the read path to be disconnected

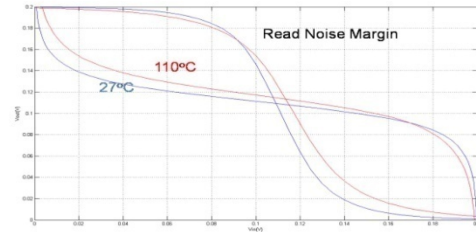

Fig. 12. Butterfly plot for 11T-SRAM at different temperatures

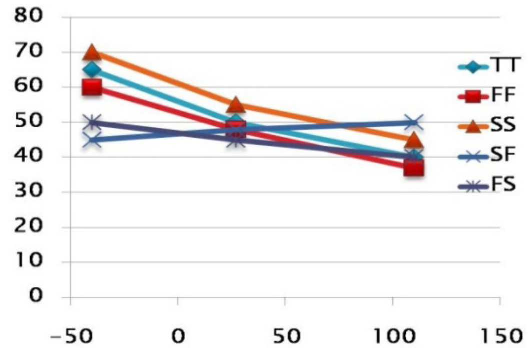

Fig. 13. Read noise margin in mV versus temperature for 11T-SRAM

from ground. However leakage through M11 causes some reduction in RDBL voltage. Also during this time, M9 is turned off, and because its source is connected to a high voltage it will be leaky. Still this leakage has no effect on YN or RDBL, because the drain of M9 is connected to ground via M8.

However there is a leaky path during the read cycle, when Y has stored "0". In this case the drain of M8 is at a high voltage more than 1.4VDD that causes more channel leakage through M8 and also gate leakage in M11. To suppress the channel leakage path through M8, a modified topology as shown in Fig. 10 is proposed. When Y is high the source of M8 is connected to ground through the added inverter, but when Y stores "0", the source of M8 is connected to VDD, which suppresses the leakage path in M8 during the read cycle.

Fig. 11 shows the simulation results for the proposed circuit for SNM in read and hold cycles. As it can be seen, SNM of the 11T circuit in hold and read mode is the same, which is due to higher read current of the proposed circuit. The circuit was also simulated for a temperature of 110°C with a supply voltage VDD=0.2. These results were compared to the results with a temperature of 27°C in Fig. 12 which shows that the SNM at higher temperature is lower. This is because of the many leakage sources and also dependence of current to temperature. Fig. 13 shows read noise margin for 11T-SRAM in different process corners.

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As mentioned before, the PMOS devices have a higher current than NMOS devices. This causes some problems in write mode. Therefore the circuit was redesigned for write mode using larger devices. The access NMOS transistors must be larger to dominate the current via PMOS transistors (M2, M4) to write a "0" in storage nodes. However there are some limitations on upsizing transistors. In this case (write mode) the sizes of M2 and M4 must be decreased while M5 and M6 must be increased to have a correct write with at high speed. Still the speed in write mode is the same as for 6T SRAM cell, so by working at a 0.25V supply voltage results in a very low speed during write mode.
However, this problem is eliminated by increasing the supply voltage to a voltage more than 0.3V. In this case, both circuits are running at a satisfactory speed with a proper write noise margin.
The effective area overhead for the proposed circuit is typically between 22%-28%, but due to employing minimum size devices and lowering the sizes of PMOS devices in 6T-SRAM and also downsizing the NMSO transistors in 6T-SRAM cell, the area overhead may be reduced. The SNM is significantly increased (more than 6X in some cases compared with 6T-SRAM) and also simulations show that the speed of the proposed circuit is 4 times higher than the 6T-SRAM cell. Table 1 shows a comparison of the read noise margin between this work and the 10T-SRAM in [11]. As it can be seen the read noise margin of the 11T-SRAM is higher than that of the SRAM in [11]. Since both topologies relies on the same 6T-circuit for the write cycle, the write noise margins are comparable.

Table1. Read noise margin comparison.

Process corner	Temperature (°C)	Read Noise Margin (mV) [11]	Read Noise Margin (mV) 11T-SRAM
TT	-40	62	85
	27	57	76
	110	52	62
FF	-40	61	70
	27	54	61
	110	51	48
FS	-40	50	70
	27	45	63
	110	38	60
SF	-40	64	62
	27	59	67
	110	52	71
SS	-40	57	81
	27	55	72
	110	47	54

IV.CONCLUSIONS

An 11T-SRAM cell with higher SNM and higher speed operated at a supply voltage 0.2V was presented. In this circuit distinct lines for read and write were used. Compared to the 6T-SRAM cell higher speed, higher SNM and lower power consumption were demonstrated through simulations at a cost of a moderately increased area. Also, to further decrease the off current compared to the 6T-SRAM, an additional inverter was added to 11T-SRAM. The modofoed circuit shows a better SNM in read mode compared to the 6T-SRAM and the work reported in [11], maintaining the same SNM in write mode.

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