A Leakage-Tolerant CMOS Comparator in Ultra Deep Submicron CMOS Technology

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ABSTRACT: In this paper a new design for CMOS comparator is presented. This circuit is simulated using predictive 70nm CMOS technology models. The results show significant improvement in noise immunity and also fairly considerable total power reduction. Proposed circuit simulated for high fan-ins (8, 16, 32, and 64 bits). The results show a very small area overhead and 10% - 30% reduction in total power dissipation. Also, for some of circuits, our proposed circuit had a higher speed.

INTRODUCTION

High fan-in comparators are widely used in circuits, such as high-performance microprocessors, communication systems, and many other systems [7]. A faster and power efficient comparator is desirable. Superscalar microprocessors make extensive use of associative matching logic and comparators to support out-of-order execution and virtual memory mechanisms. The traditional equality comparators used for implementing associative logic in modern datapaths. in this paper, we present two comparator circuits that employed for low leakage and high speed applications. First circuit is a low power and high speed with very small area overhead. But about second circuit, is a low leakage, high speed and with no area overhead.

The rest of the paper is aligned as follows: section II discusses briefly about previous work. Section III describes the proposed circuits. Section IV contains the obtained results.

PREVIOUS WORKS

The schematic of a high fan-in (16-input) dynamic comparator based on standard footless domino logic comparator (FLDLC) has been shown in Fig. 1. In precharge mode, all inputs go low, and the precharge node is precharged high and the output goes low. During the precharge mode, CLK is low. So, MP1 is on and MP2 is off. The precharge node started to charge to high. Then OUT node goes low and MP2 is turned on. Just when A and B are different, the pull down transistors start to discharging the precharge node. In the evaluation phase, when the clock is high, inputs are applied to the gate. If all the corresponding bits of A and B inputs are equivalent, there is no is charging path for the precharge node. However, if A and B inputs differ in any bit position, a conduction path from the precharge node to the ground is established, discharging the dynamic and causing the output to go high. In literature, some other circuits have been proposed [1], [2]. The standard Footed domino logic comparator (FDLC) has been shown in fig. 2. The N-foot transistor improves the noise immunity and reduces the total power consumption. But this circuit has an area overhead and also lower speed rather than FLDLC circuit.

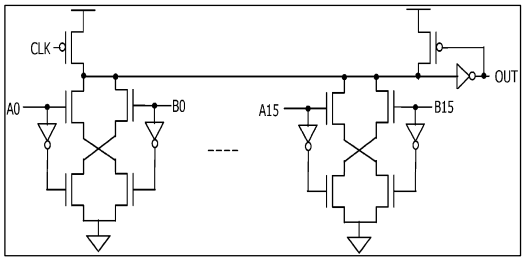

Fig.1 Footless Domino Logic Comparator (FLDLC)

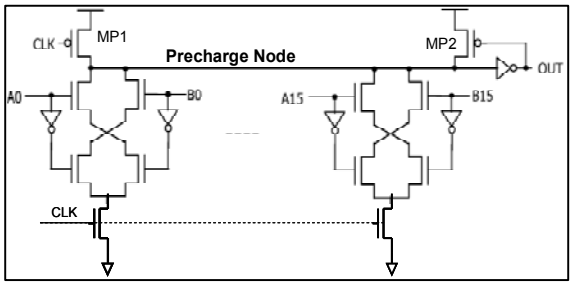

Fig.2. Footed Domino Logic Comparator (FDLC)

In many situation where the circuit of Fig. 2 is used in modern datapaths (in applications alluded to earlier) mismatches occur with a much higher frequency compared to full matches. Consequently, significant energy saving can be realized if comparators and associative logic can be designed to dissipate energy only

on a full match and little or no energy on mismatches. In recognition of this inefficiency, first noticed in [3], a

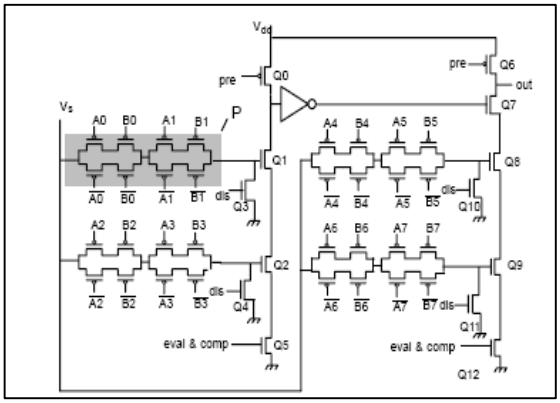

Fig. 3 .Domino-Style Comparator (DSC)

series of such dissipate on match comparator (DMC) introduced in [2], [6]. A new comparator introduced in [2] that is a domino-style comparator design. This circuit is working as follows:

two 8-bit comparands are compared using a combination of pass-transistors and domino-style logic. Pass transistor block (such as P in fig. 2) compare two bits of the comparands at a time. A high voltage level Vs is passed on the right by each of these p-transistor blocks.

When the full match is happened, the gates of the transistors Q1, Q2, Q8, and Q9 are changed to Vs voltage. The problem of this circuit is higher area overhead compared with FDLC circuit, because of using 35 p-transistors and 12 n-MOS transistors. The power dissipation depends on Vs values. Another circuit proposed in [4] was pass-logic, single stage comparator (PLSSC) design. In this circuit, the lower speed compared to FDLC circuit is its main problem. The lower speed is from 4-stacked transistors. Other problem is area overhead of this circuit, because of using P-MOS transistors. The power dissipation in Fig. 3 is more than Fig. 4, because dissipation happened during 4-bit match and full match. In [4], the PLSSC used transistors in 180nm CMOS technology that has a low leakage compared with 70nm CMOS technology. The PLSSC circuit doesn't work properly in sub 100nm CMOS technology. Because, the lower supply voltage is suitable for sub 100nm technology. The PLSSC circuit examined using 0.9 V supply voltage, but it makes some problems because of charge sharing.

In our proposed circuit, we have used 70nm CMOS predictive models. Because of applying low supply voltage (0.9v) and also very low leakage, the total power is less than other works.

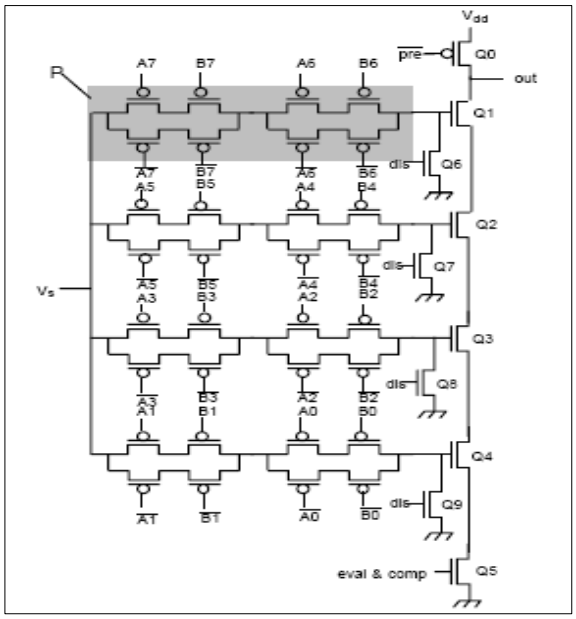

Fig. 4 .the PLSSC Circuit

PROPOSED COMPARATOR

Fig. 5 shows the schematic of our proposed comparator [8]. The worst case scenario for delay is when inputs A

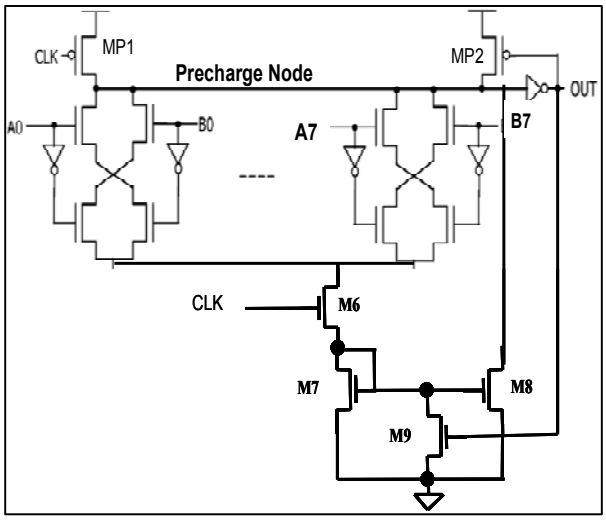

Fig 5. Proposed Comparator

and B are different in only a single-bit position. In this

case, only one of the evaluation branches conducts and discharges the precharge node. The worst case scenario for noise at the inputs is the case where all the inputs are low and receive the same noise in the evaluation phase [5]. In the FLDLC, the keeper transistor is upsized from a keeper ratio of 1 to 2 in order to achieve different data points for delay and noise immunity. This circuit doesn't work fairly in high fan-in application. N-MOS Transistors M8 and M7 in our proposed circuit help evaluation phase to be faster. Because of using n-MOS transistors of minimum size, the evaluation phase will be slow without current mirror (M7, M8).

The FLDLC comparator fails to operate for smaller keeper sizes because of high leakage in scaled technologies (70 nm). The main problem of our circuit is dynamic power dissipation compared to PLSSC and domino style circuit. We compensate this power overhead using small size evaluation transistors and also low power supply voltage. The PLSSC circuit doesn't work properly in low supply voltage. Because charge sharing problem, doesn't let the output node to be in VDD voltage. Also, the leakage power dissipation in 70nm CMOS technology for n-MOS transistor with drain connected to VDD and gate connected to a noise source is comparable with dynamic power dissipation even more than 40% of total power. So the results for total power dissipation for our work and previous circuits are shown in Fig. 6. As shown, total power dissipation for 32 and 64-bits proposed comparator is less than other circuits. These results are from low leakage in high fan-in for the proposed comparator. The total power measured for 8, 16, 32, and 64 bits inputs with half bits matches. This metric is not exactly correct, but it can be an average of the total power dissipation for different inputs.

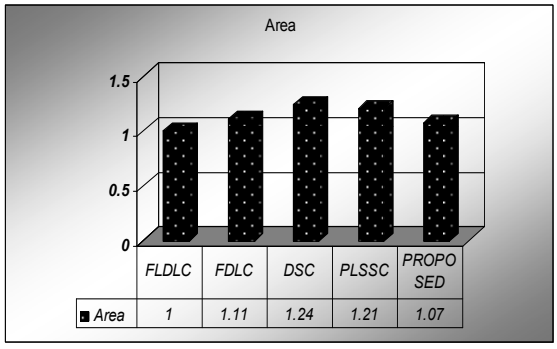

Fig. 6 .Total power dissipation for 8, 16, 32, and 64-bits comparators (left to right: FLDLC, FDLC, DSC, PLSSC, and Proposed Circuit-Normalized to FLDLC total power)

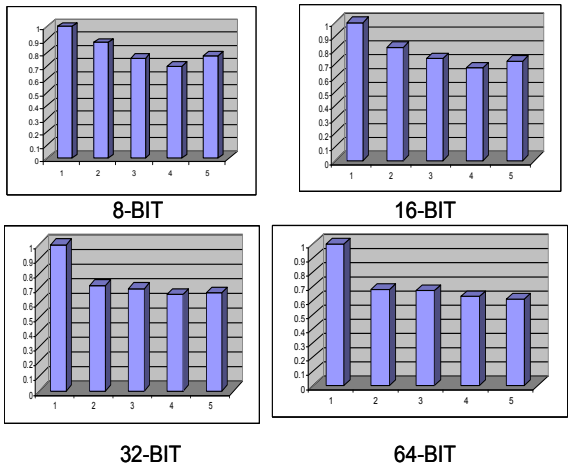

Fig. 7 .Area comparison for logic comparators (normalized to FLDLC area)

We also count area for all circuits. The results show that area for proposed circuit is smaller than PLSSC and DSC circuits. The area counted by Multiply all W and L of transistors. Fig. 7 shows that our proposed circuit has smaller area compared with other circuits, because of employing minimum size evaluation transistors. In PLSSC circuit, the p-MOS transistor Q0 must be large enough to have a fast response time. Also, in precharge phase four transistors Q6, Q7, Q8, and Q9 consumes dynamic power that increases total power dissipation. The proposed circuit has a faster response time compared with PLSSC and DSC and also FDLC circuits. The results for speed comparison have been shown in Fig .8.

These results have been obtained for 8-bit comparators. The results show speed improvement in our proposed circuit compared with other circuits.

CONCLUSIONS

We proposed a new comparator used for UDSM technologies. We found it suitable for high fan-in applications. The proposed circuit is more efficient for wide applications. Also, the proposed circuit is power efficient for wide gates. The proposed circuit is an optimal design for high speed, low power and also leakage –tolerant applications.

REFERENCES

[1] Berkeley Predictive Technology Model. Univ. Berkeley, Berkeley, CA. [Online]. Available: http://www-device.eecs.berkeley.edu/~ptm

[2] Ergin, O., Ghose, K., Kucuk, G., Ponomarev, D., "A Circuit–Level Implementation of Fast, Energy–Efficient CMOS Comparators for High–Performance Microprocessors", in Proc. Of ICCD, 2002, pp.118–121.

[3] Brooks, D.M., Bose, P., Schuster, S.E. et al, "Power–Aware Microarchitecture: Design and Modeling Challenges for Next–Generation Microprocessors", IEEE Micro Magazine, 20(6), Nov./Dec. 2000, pp. 26–43.

[4] ., Ponomarev, D., Kucuk, G., Ghose, K., Ergin, O., "Power Efficient Comparators for Long Arguments in Superscalar Processors" , IN Proc. of ISLPED 2003.

[5] Mahmoodi H., Roy K., "Diode-Footed Domino: A Leakage-Tolerant High Fan-in Dynamic Circuit Design Style", *IEEE Transactions on Circuits and systems*, vol. 51, no. 3, pp. 495-503, March 2004.

[6] Kucuk, G., Ghose, K., Ponomarev, D. and Kogge, P., "Energy–Efficient Instruction Dispatch Buffer Design for Superscalar Processors," in *Proc. ISLPED*, 2001, pp. 237–242.

[7] Menendez E. R., Dumezie M., "CMOS Comparators for High-Speed and Low-Power Applications", in Proc. IEEE 2006.

[8] Moradi F., Peiravi A., Mahmoodi H., "A New Leakage-Tolerant Design for High Fan-in Domino Circuits" in *proceeding of International Conference on Microelectronics, Tunisia. 14-16 MAY 2004.*