A Low-Power SRAM Using Bit-Line Charge-Recycling Technique

Keejong Kim
School of ECE,
Purdue University
West Lafayette, IN 47906, USA
1-765-494-3372
keejong@ecn.purdue.edu

Hamid Mahmoodi
School of Engineering,
San Francisco State University
San Francisco, CA 94132, USA
1-415-338-6579
mahmoodi@sfsu.edu

Kaushik Roy
School of ECE,
Purdue University
West Lafayette, IN 47906, USA
1-765-494-2361
kaushik@ecn.purdue.edu

ABSTRACT
We propose a new low-power SRAM using bit-line Charge Recycling (CR-SRAM) for the write operation. In the proposed write scheme, differential voltage swing of a bit-line is obtained by recycled charge from its adjacent bit-line capacitance. In order to improve the data retention capability of un-selected cells during write, the power supply lines of memory cells in one column are connected to each other and separated from the power lines of other columns. A test-chip is fabricated in 0.13μm CMOS and measurement results show 88% reduction in total power compared to the conventional SRAM (CON-SRAM) at V_{DD}=1.5V and f=100MHz.

Categories and Subject Descriptors
B.3.1 [**Memory Structures**]: Semiconductor Memories – *Static memory (SRAM);* B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Memory Technologies*

General Terms
Measurement, Design

Keywords
Charge-recycling, SRAM, Low power, Write power, Process variation, Write margin

1. INTRODUCTION
Considerable attention has been paid to the design of low power and high performance SRAM's as they are critical components in both hand-held devices and high performance processors. Read-cycle power consumption is kept low by limiting the swing of the bit-lines, but write-cycle power consumption remains quite large due to the full swing nature of the bit-lines during the write operation. Reducing voltage swing of the bit-line is an effective way to save the power dissipation in write cycles. Voltage swing reduction of bit-lines is, however, limited due to possible write-failures under process variations.

In this paper, a new write scheme is proposed for low-power SRAM which uses charge-recycling (CR) [1,2] on bit-line. In the proposed write scheme, the low voltage swing of each bit-line is obtained by the recycled charge from the adjacent bit-line capacitance, instead of the power line. In order to improve the data retention capability of un-selected SRAM cells during write cycle, the power supply lines of memory cells in a column are connected to each other and separated from the other column's power lines. We have also investigated CR-SRAM write stability under process variations. A proto-type 4KB CR-SRAM is implemented in IBM 130nm CMOS technology and it exhibits write power dissipation of 192μW with 1.5V supply voltage at 100MHz. A 4KB CON-SRAM array without charge-recycling was also implemented to compare the SRAM write power. Measurement results show that the proposed write scheme can reduce total power by 88% compared to that in the conventional SRAM.

The rest of the paper is organized as follows. In Section 2, the write scheme using CR is proposed. In Section 3, we present the power comparison of CON-SRAM and CR-SRAM, and present write immunity under process variation. In Section 4, we present the measurement results. Finally, conclusions are drawn in Section 5.

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2. CHARGE-RECYCLING ARCHITECTURE
In this section, first, we will explain a new concept of SRAM write scheme using CR method to reduce active power of bit-lines in write cycle. Second, we will explain the power control circuitry which is introduced to improve the data retention capability during write operation. Third, we will discuss the SRAM mode change between read and write cycles in the proposed scheme. Finally, we will describe the implementation of CR-SRAM based on the proposed write scheme.

2.1 Concept of SRAM Writing Using Bit-Line Charge-Recycling
Figure 1(a) shows a simplified circuit diagram for SRAM write using CR method. A bit-line pair is composed of a bit-line (BL) and a complementary bit line (BLB). In Figure 1(a), we assumed that the number of CR bit-line pairs, N, is 2. The simplified write circuit using CR is composed of 2 bit-line pairs, 2 exchangers and 5 switches connected in series which are controlled by EV and EQ signals. From input data, the exchanger determines whether the bit-line and complementary bit-line will be directly- or cross-connected to the neighboring bit-line pair. When the input data of SRAM is high, the bit-line is connected to the upper bit-line pair with the higher voltage and the complementary bit line is connected to the lower bit-line pair with the lower voltage. The bit-line, which is in the top bit-line pair and must be connected to the upper bit-line pair with the higher voltage, is connected to

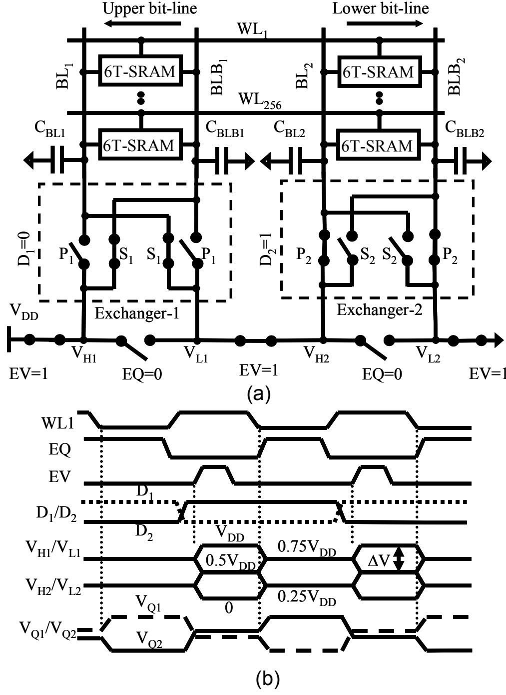


Figure 1. (a) Schematic circuit for charge-recycling on bit-lines with N=2 in SRAM; (b) voltage waveforms when EV=1, EQ=0, D1=0, D2=1

V_{DD}. On the contrary, the bit line, which is in the bottom bit-line pair and must be connected to the next bit-line pair with lower voltage, is connected to ground. Figure 1(b) shows voltage waveforms when two-bit input data D_1=0, D_2=1. It can be observed from the figure, BLB_1 and BL_2 are charged with higher voltage than BL_1 and BLB_2 since D_1=0 and D_2=1. When SRAM is in equalization mode, all connections between bit-line pairs, which are predetermined by input data, are disconnected and two bit lines in each bit-line pairs are connected by an EQ signal. Two bit lines in the bit-line pair with different voltages share their charges and their voltage is average of the two values. If we assume that the number of CR bit-line pair is N and all bit lines have the same capacitances, the voltage in the ith bit-line pair becomes $[(2i-1)/2N]\times V_{DD}$ [1]. When the SRAM is in evaluation mode, two bit lines in each bit-line pair are disconnected and all bit-lines are connected to bit-lines in the neighboring bit-line pair by an EV. A bit line and its neighboring bit line are connected by a predetermined input data. They share their charges and their voltage is the average of the two values. At this time, two bit-lines in a bit-line pair have different voltages by connecting the neighboring bit lines. As a result, the ith bit-line pair has a voltage difference (ΔV) of $(1/N)\times V_{DD}$. If input data to be written is high, the voltage of the bit-line becomes $(1/N)\times V_{DD}$ higher than that of the complementary bit line. On the contrary, if input data is low, the voltage of bit line becomes $(1/N)\times V_{DD}$ lower than that of the complementary bit line. Using the $(1/N)\times V_{DD}$ voltage difference between bit-line pair, we can write data into SRAM cell. Through the charge sharing between bit lines in the same bit-line pairs and in the different bit-line pairs during equalization and evaluation, respectively, the charge used in the upper bit-line is recycled in the lower bit-line pair in the next clock cycle, as shown in Figure 1(b). In Figure 1(b), Q1, Q2 represent the internal node voltage of

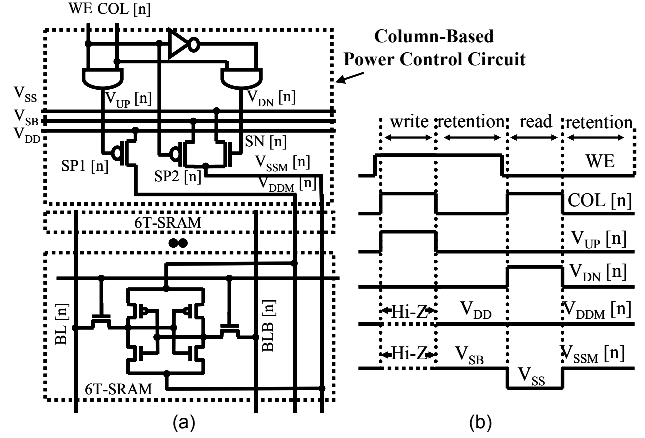


Figure 2. (a) power control circuit for proposed write scheme (b) timing diagrams of power control circuit.

SRAM cells. In this scheme, the charge of bit-line can be recycled again and again by rolling down to the lower adjacent bit-line pair in every cycle, until this charge reaches ground. If the number of CR bit-line pair is N, the bit-line charge in the top bit-line pair is recycled N times through N bit-line pairs from V_{DD} to ground. When a group has N bit-line pairs and bit-line capacitance is C_{BL}, the N bit-line pairs consume the power of $(1/N)\times C_{BL}\times V_{DD}^2$ per clock cycle instead of $N\times C_{BL}\times V_{DD}^2$. The power saving ratio of the bit lines in the CR-SRAM becomes $1/N^2$ [1]. As N increases, the power saving in the CR-SRAM drastically increases.

2.2 Column-Based Power Control Circuit for Charge-Recycling

In order to increase power saving and ensure a write using CR, the charge loss due to bit line leakage current should be minimized. Because the bit line leakage current reduces the voltage swing between bit-line pair during write operation and hence, causes the degradation of write stability. The bit-line leakage current including SRAM cell leakage current can be simply reduced by increasing the source-line voltage from V_{SS} to V_{SB}, due to the increased reverse body bias of access transistors [3,4]. To be able to write a data into SRAM cell using low-voltage swing on bit-lines, the SRAM cell should be isolated from power sources (V_{DD} and V_{SS}) during CR while the word-line is activated [5]. The isolation of the word-line activated SRAM cells from power sources (floating) during a write cycle, however, decreases the data retention stability particularly for the SRAM cells of unselected columns [5]. The word-line activated SRAM cells become largely unstable when the supply voltages of SRAM cells are in floating states, and the data in these SRAM cells are easily destroyed. In order to improve the data retention stability of the un-accessed SRAM cells during a write operation, we make the SRAM cells to be floating only in the selected columns. By introducing the column-based power-line control [5], we can improve the data retention capability for the memory cells which are not selected to be written. Figure 2 (a) illustrates the key structure of the technique. The power lines (V_{DDM} and V_{SSM}) of memory cells in a column are connected to each other and separated from the other column's. The V_{DDM} [n]/V_{SSM} [n] are connected to V_{DD}/V_{SS} by power switches of SN [n], SP1 [n], and SP2 [n]. These power switches are controlled by the write enable signal WE and column selection signal COL[n], and it is turned off when the memory cell in the column is accessed for writing,

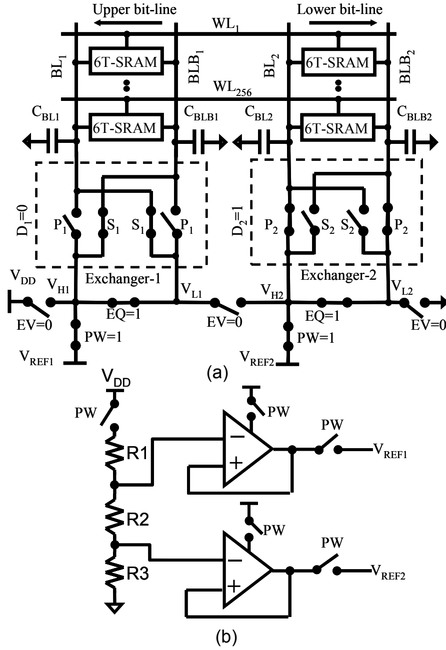


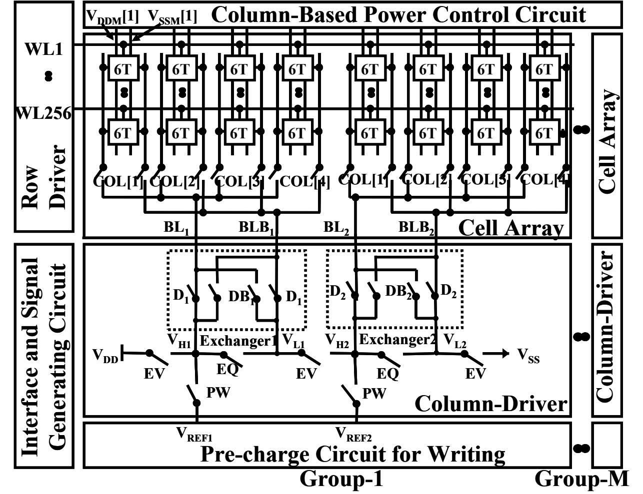
Figure 3. SRAM mode change from read to write (a) configuration when EV=0, EQ=1, PW=1, D1=0, D2=1 (b) Reference generation circuit for write start-up (N=2).

and V_{DDM} [n]/V_{SSM} [n] change to a floating state. The isolation of SRAM cell from power lines also results in significant leakage reduction on idle cells.

Figure 2(b) shows the timing diagram of the control circuit in write/read cycles based on proposed write scheme. The control signals V_{UP} [n] and V_{DN} [n] are synchronized with the nth column selection signal COL[n], and the power switches (SN [n], SP1 [n], and SP2 [n]) are turned off when COL[n] becomes high in write-cycle (WE='1'). After COL[n] become low, both V_{UP} [n] and V_{DN} [n] go back to low, V_{DDM} [n] and V_{SSM} [n] become V_{DD} and V_{SB}, and small swing data is amplified to (V_{DD}-V_{SB}) swing inside a cell. The cycle time can be divided into three parts depending on whether write enable signal WE and column selection signal COL[n] are high or low. When COL[n] is low, the SRAM maintains the data retention mode irrespective to the status of WE since the virtual V_{SS} and V_{DD} line voltages (V_{SSM}, V_{DDM}) become V_{SB} and V_{DD}, respectively, and the cell stores the data at a reduced voltage swing of (V_{DD}-V_{SB}). When COL[n] and WE are high, both V_{SSM} [n] and V_{DDM} [n] are in floating states (Hi-Z) and SRAM is in write mode. When COL[n] and WE is high and low, respectively, V_{SSM} [n] is zero and V_{DDM} [n] is high and SRAM is in the read mode. Note that the column selection signal COL[n] should switch to '0' after the word-line is turned-off to ensure successful write to a cell.

2.3 Mode Change between Read and Write Cycles

There are several differences between conventional and CR-SRAM. In the write cycle, bit-lines have different voltage levels determined by the charge-recycling operation. This fact requires a special design consideration to transition between read and write cycles. In the read cycle, all bit-lines are pre-charged to V_{DD}. When the cycle changes from read to write, bit-line voltages need to be preset to their write voltage levels that they would normally be obtained after several consecutive charge recycling write



6T: 6T-SRAM, D_1,DB_1(D_2, DB_2): Input data to write, BL_1-BLB_1(BL_2-BLB_2): bit-line pairs, EV, EQ: evaluation and equalization, PW: initial pre-charge signal, V_{REF1}, V_{REF2}: reference voltages to pre-charge, V_{DDM}[1], V_{SSM}[1]: power-lines at the first column, WL1, WL256: word-lines

Figure 4. CR-SRAM architecture (N=2, 256-row word-lines, 4-column MUX switches).

operations. We address this issue by generating the set of voltage levels needed to initialize bit-lines upon transition from read to write. Figure 3(a) shows the pre-charge configuration to write when EV=0, EQ=1, PW=1, D_1=0, D_2=1, and N=2. When the operation mode changes from read to write, the initial node voltage of V_{H1}/V_{L1} and V_{H2}/V_{L2} are preset to V_{REF1} and V_{REF2} respectively by switching PW='1'. Figure 3(b) shows the reference generation circuit for write pre-charge when mode changes from read to write. The PW signal is activated only once when mode is changed from read to write. If the PW is switching to an off-state, all the power-lines of reference generation circuit are cut-off state. Since these initial start-up reference voltages are required only upon transition from read to write cycle, the power overhead of the start-up circuit including reference voltage sources is negligible. Figure 4 shows the implemented CR-SRAM structure. The CR-SRAM is composed of a column/row driver, interface signal generator, power control circuit, and M-grouped blocks. Each block has a column driver and N bit-line pairs. Each bit-line pair has one transistor to equalize two voltages of the bit-line pair.

3. SIMULATION RESULTS AND COMPARISONS

In order to verify the effectiveness of proposed SRAM in scaled technologies [6], we will evaluate the power consumptions and SRAM stability using predictive technology models [7]. In Section 3.1, we will evaluate the SRAM power dissipations with read/write operations, technology nodes, and frequencies. In Section 3.2, we will evaluate the write stability for process variations. The data retention capability during write operation will be investigated in Section 3.3. Finally, in Section 3.4, we will investigate the read/hold SNM and write margins.

3.1 Writing Power Comparison of CR-SRAM

The power dissipation of the proposed SRAM is simulated using 0.18μm predictive technology model [7]. Figure 5 shows a simulated waveforms when read cycle=50% and write cycle=50% in 4-stacked bit-line pairs (N=4) at 100MHz. When WE switches

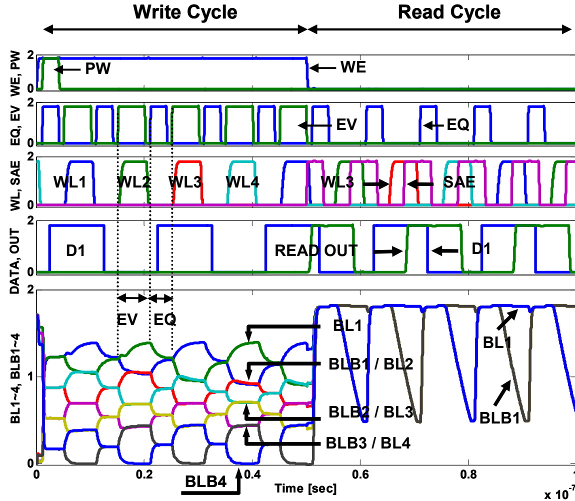


Figure 5. Simulated waveforms of CR-SRAM (180nm, W/R(%)=50/50, V_{DD}=1.8V, V_{SB}=0.2V, f_{CLK}=100MHz, N=4, T=25℃)

to high, SRAM switches to the write cycle and the initial start-up signal PW is activated to preset the voltages of the bit-lines. Then, the voltages of the bit-lines are maintained by charge-recycling operation. Figure 5 also shows the waveforms when SRAM mode changes from write to read cycle. When the mode changes from write to read, the bit-lines are pre-charged to V_{DD} and SRAM begins to read the stored data.

Figure 6(a) shows the power comparison of CR-SRAM and CON-SRAM for several write/read (W/R) cycle patterns. The total power includes leakage power of SRAM array, row driver power, power of the charge-recycling control circuit, and column driver power. The column driver power includes power dissipation in charging/discharging of bit-line (write power). In this comparison, we assumed that the bit-line of a CON-SRAM has full voltage swing of V_{DD}. The leakage power is negligibly small and the most power in CON-SRAM is dissipated in column driver by dynamic power due to full-swing. By using the CR method, the power dissipation in a CR-SRAM is reduced to 7.7% of the CON-SRAM power (92.3% power reduction). Figure 6(b) shows the comparison of power consumption under write cycle with number of bit-line pair N in a group of SRAM. As N increases, the total power decreases to 18.5% (N=2), 7.7% (N=4), 6% (N=6) and 4.8% (N=12) of that of CON-SRAM.

We investigated the total power savings of the proposed scheme with the transistor scaling. Figure 7 shows the comparisons of total power consumption for different technology nodes (100nm, 70nm). As the transistor size is more scaling down, the leakage power becomes more important. At 70nm technology node, the proposed scheme saves the total power 94% compared to conventional scheme.

3.2 Write Immunity under Process Variations

Die-to-die and within-die variations in process parameters result in mismatch in the strength of different transistors in an SRAM cell, resulting in write failures [8,9]. In the proposed write scheme, the power supply lines are floating during the time the word-line is high. Floating power supply lines (V_{DD} and V_{SS}) in the memory cell assist the write operation because the floating

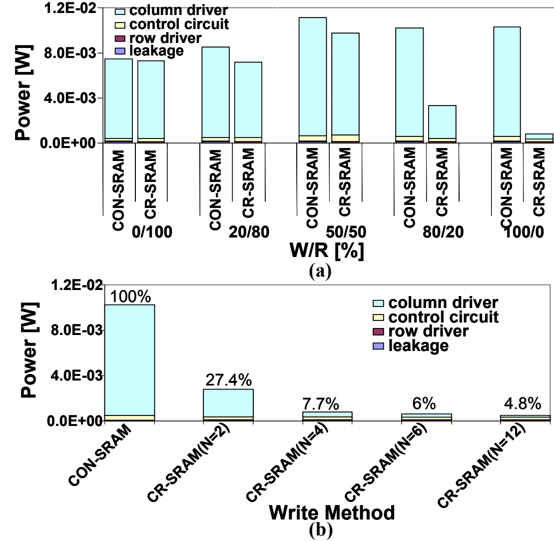


Figure 6. Power estimation (a) with read/write cycle when N=4 (b) with recycling bit-line pairs of N (180nm, CBL=300fF, RBL=60Ω, f_{CLK}=100MHz, 25°C).

power supply lines disable the driver NMOS and load PMOS of the cell [5]. In order to estimate the write immunity under process variations, we evaluate the maximum allowed mismatch in threshold voltages of SRAM cell transistors in the worst case direction (ΔV_{TH}) for the write operation. Table 1 tabulates the threshold voltage assignments in an SRAM cell when threshold voltage mismatch is worst case direction. Figure 8 shows the maximum allowed worst case mismatch in threshold voltages for different number of bit-line pairs N (70nm, 180nm). In the simulation, we assumed V_{DD}=1.5V (180nm), 1.2V (70nm), f=100MHz, and T=25°C. As N increases, the acceptable range of ΔV_{TH} decreases because the voltage differential between bit-lines in a bit-line pair decreases at the rate of $(1/N)\times V_{DD}$. Smaller voltage differential between bit-lines in a bit-line pair reduces the tolerance to threshold voltage variation in the write operation. If we assume that ΔV_{TH} (3σ) is 90mV in the 70nm technology, N should be less than 6.

3.3 Data Retention Capability of Un-selected Cells

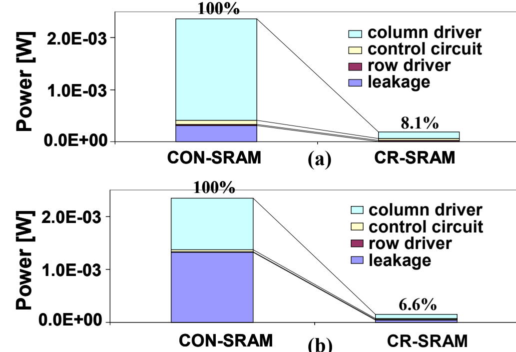


Figure 7. Power estimation with technology nodes when SRAM is writing operation (a) 100nm (b) 70nm (CBL=167fF@100nm, CBL=117fF@70nm, f=100MHz, N=4).

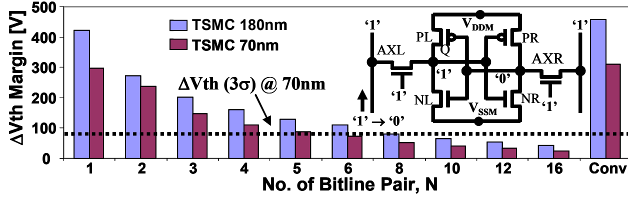


Figure 8. Worst case simulation over process variations with for stable write operation with number of bit-line pair N

Table 1. Worst case mismatch of 6T-SRAM under write operations ($|\Delta V_{TH}|$: V_{TH} Variation, V_{TN0}/V_{TP0}: nominal V_{TH} of NMOS/PMOS)

V_{TH}		V_{TH} Definition	6T SRAM
High V_{TH}	NMOS	$V_{TN0} + \lvert\Delta V_{TH}\rvert$	NL, AXL, AXR
	PMOS	$V_{TP0} - \lvert\Delta V_{TH}\rvert$	PR
Low V_{TH}	NMOS	$V_{TN0} - \lvert\Delta V_{TH}\rvert$	NR
	PMOS	$V_{TN0} + \lvert\Delta V_{TH}\rvert$	PL

during Write Operation

We investigated the data retention capability for the unselected SRAM cells during write operation. In order to improve the data retention stability of the un-accessed SRAM cells during the write operation, we make the SRAM cells to be floating only in the selected columns using column-based power selection scheme [10]. Figure 9 (a) shows SRAM cells when WL1 and COL[1] are selected. When WL1 and COL[1] are selected, the C1 and C9 cells are accessed to write. Since COL[1] is selected, the power lines of cell C5 and C13 are in floating state while the word-line is in off-state. In order to investigate the data retention capability of SRAM cells, we evaluated the maximum threshold voltage mismatch in the worst direction for the retention condition. Figure 9(b) shows allowed threshold voltage mismatch for data retention of C5. As the transistor feature size is scaled down, the allowed threshold voltage mismatches in the worst direction decreases due to the higher leakage current of transistor during write operation. It is confirmed from Figure 9(b) that data retention capability for an un-accessed cell (C5) is guaranteed since allowed threshold voltage mismatch for data retention is higher than 165mV at

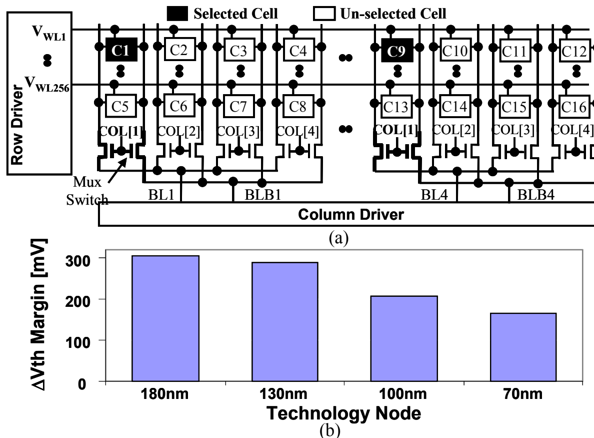


Figure 9. Data-retention capability of un-accessed cell (C5) under process variation (a) SRAM cells when WL1 and COL[1] are selected. (b) ΔV_{TH} margin for data retention (N=4, f_{CLK}=100MHz, 25℃, V_{SB}=0.2V, V_{DD}= 1.8V@180nm, 1.6V@130nm, 1.4V@100nm, 1.2V@70nm)

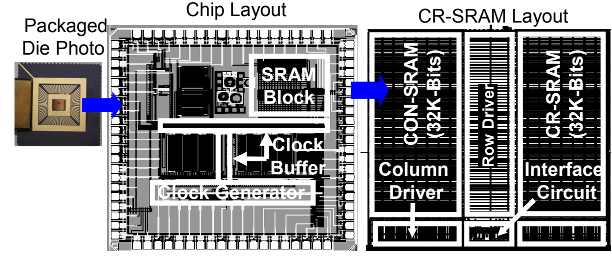


Figure 10. Chip micrograph of 64K-Bite prototype module

Table 2. Features of the test chip.

Technology	0.13um CMOS
Supply Voltage	1.5 V
Number of CR Bit-Line Pair	4
Organization	32K-Bits CR-SRAM, 32K-Bits CON-SRAM
Chip Core Area	0.765mm² (CR-SRAM + CON-SRAM)

70nm technology, which is 1.8 times of 3σ, if 3σ is assumed to be 90mV.

4. MEASUREMENT RESULTS

A 4-kbyte SRAM test chip with the proposed writing scheme (CR-SRAM) was fabricated in a 0.13-μm IBM CMOS technology. The microphotograph of the test chip and layout showing the organization are shown in Figure 10. The layout is consisted of row driver, column driver, SRAM array, and interface circuits. A conventional 4-kbyte SRAM (CON-SRAM) array without charge-recycling, i.e., full-swing writing was also implemented to compare the SRAM write power. The fabricated memory was measured at room temperature at different power supply voltages. Table 2 tabulates the measured test chip. The measured power consumptions are 162 μW (CR-SRAM) and 990 μW (CON-SRAM) at 100-MHz clock, respectively. The core area of the test chip is 0.765mm². In HSPICE simulation, the maximum clock speed is 1.20 GHz.

The leakage power of SRAM array is measured at V_{DD}=1.5V and 25°C while sweeping the source-bias voltage (V_{SB}) from 0 to 1.5 V (Figure 11). Leakage power savings becomes moderate for V_{SB} above 0.4 V since the reduction in cell leakage levels off and junction leakage becomes a significant portion [11]. The measured leakage power of the 4-kbyte SRAM at V_{SB} of 0.4V was 23.4 μW. This is only 5% compared to the array leakage without source biasing SRAM.

We also measured the SRAM writing power separately from column driver. Figure 12 shows the measured writing power of a CR-SRAM for various clock frequencies, and for comparison, we also measured writing power of a conventional SRAM. The write

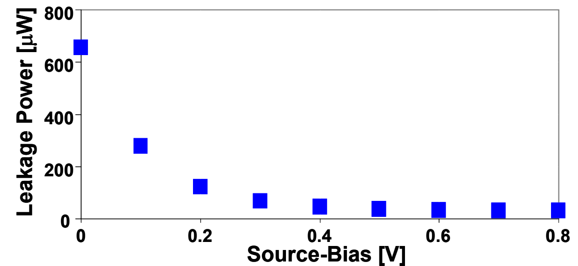


Figure 11. Measured leakage power of SRAM array with source bias voltage at V_{DD}=1.5V (256b×256b).

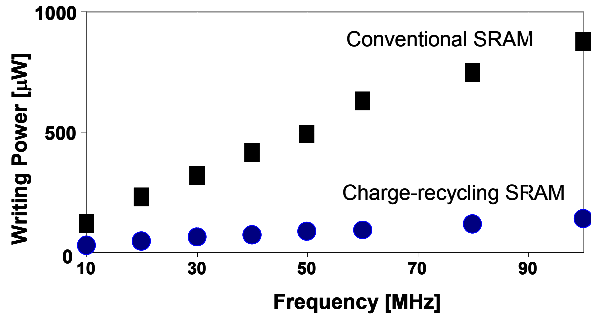


Figure 12. Measured writing power of CR-SRAM and CON-SRAM (V_{DD}=1.5 V, V_{SB}=0.4 V, N=4, 128b×256b).

power is more saved as the clock frequency increases since the power dissipation by charging and discharging of bit-lines becomes more dominant compared to the power of the other circuits. When the clock frequency approaches 100 MHz, the total writing power saving is increased up to 88% for the conventional full-swing scheme.

Figure 13 compares the total power dissipation in CR-SRAM with those in CON-, SB-SRAM. The power consumptions in each part of the SRAM are measured at 100MHz under the write mode with a 1.5V supply voltage (V_{DD}) and a 0.4V source line voltage (V_{SB}). By raising V_{SB} from 0V to 0.4V, the SB-SRAM was able to reduce the total power by 61% from CON-SRAM, however, the power dissipation in column driver still accounts for as high as 92% among total power. By applying the proposed CR technique, the power dissipation in a CR-SRAM is reduced to 20% and 12% compared to SB-SRAM and CON-SRAM, respectively. Figure 14 shows the measured readout waveforms from data output buffer at 1.5V V_{DD} and 50MHz clock frequency.

5. CONCLUSION

This paper presents a low power charge-recycling SRAM for battery-operated portable applications. By applying the charge recycling technique to the bit-lines, it is possible to effectively reduce the SRAM write power associated with charging and discharging of the highly capacitive bit-lines. The CR-SRAM is implemented in IBM 130nm CMOS technology and measurement results show 88% reduction in total power dissipation compared to the conventional SRAM at V_{DD}=1.5 V and f=100MHz. The proposed CR-SRAM architecture is a promising candidate for embedded memory of battery operated portable applications.

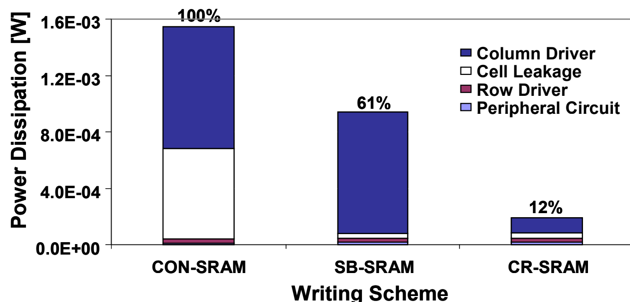


Figure 13. Measured total-powers of proposed and conventional SRAM (128b×256b, N=4, V_{DD}=1.5V, V_{SB}=0.4V, f_{CLK}=100MHz, 25℃).

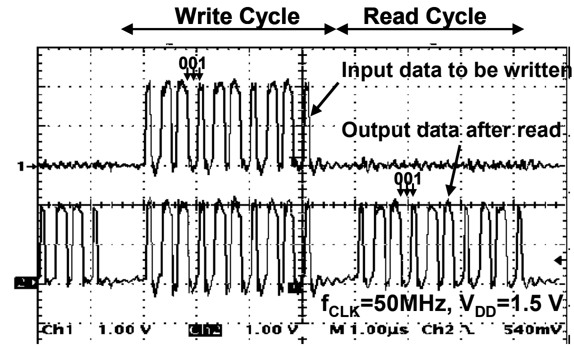


Figure 14. Measured readout waveforms from data output buffer (f_{CLK}=50MHz, V_{DD}=1.5V, V_{SB}=0.4V, $V_{I/O}$=2.3V)

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