Clock Gating and Negative Edge Triggering for Energy Recovery Clock

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Abstract

Energy recovery clocking has been demonstrated as an effective method for reducing the clock power. In this method the conventional square wave clock signal is replaced by a sinusoidal clock generated by a resonant circuit. Such a modification in clock signal prevents application of existing clock gating solutions. In this paper, we propose a clock gating solution for energy recovery clocking by gating the flip-flops. Applying our clock gating to the energy recovery clocked flip-flops reduces their power by 1000X in the idle mode with negligible power and delay overhead in the active mode. Applying the proposed clock gating technique to a system of 1000 flip-flops with idle mode probability and data switching activity of 50%, reduces the total power by 47%. We also propose a negative edge triggering solution for the energy recovery clocked flip-flops.

1. Introduction

Energy recovery is a technique originally developed for low power digital circuits [1]. Energy recovery circuits achieve low energy dissipation by restricting the current across devices with low voltage drop and by recycling the energy stored on capacitors by using an AC type (oscillating) supply voltage [1, 2]. The major portion of total power in highly synchronous systems is dissipated on the clock network. Hence, energy recovery clocking is an effective low power solution [3]. In this method the clock is a resonant sinusoidal signal that recycles the energy from the clock network capacitances to the supply voltage. Replacing the conventional square wave clock signal with a sinusoidal one requires modifications in the design of the flip-flops. Recently new flip-flops have been developed to operate with energy recovery clock signals [2, 3].

Clock gating is another popular technique for reducing clock power [4]. Even though energy recovery clocking results in substantial reduction in clock power, there still remains some energy loss on the flip-flops themselves due to non-adiabatic switching. Hence, it is still desirable to apply clock gating to the energy recovery clock for further reducing the flip-flop power during idle periods. The existing clock gating solutions are based on masking the local clock signal using masking logic gates (NAND/NOR) [4]. These methods of clock gating do not work for energy recovery clocking. This is because insertion of masking logic gates eliminates energy recovery from the remaining capacitances in downstream fan-out. To the best of our knowledge there have not been any clock gating solutions proposed for the energy recovery clocking.

In this paper, we propose clock gating by modifying the design of the existing energy recovery clocked flip-flops to incorporate a power saving feature that eliminates any energy loss on the internal clock and other nodes of the flip-flops. Applying the proposed clock gating technique to the flip-flops reduces their power by a substantial amount (1000X) during the sleep mode. Moreover, the added feature has negligible power and delay overhead when flip-flops are in the active mode. We also designed an energy recovery clock generator that maintains its oscillation amplitude under process and temperature variations.

In most synchronous systems, it is required to use both positive and negative edge triggered flip-flops. Obtaining negative edge triggering in conventional square wave clocked flip-flops is easily done by inverting the input clock signal using an inverter logic gate. This approach however is not applicable to the energy recovery clocked flip-flops since insertion of an inverter logic gate in the path of an energy recovery clock changes the shape of the clock and eliminates the energy recovery property. To the best of our knowledge there have not been any negative edge triggered energy recovery clocked flip-flops proposed in the literature. In this paper we propose a class of negative edge triggered energy recovery clocked flip-flops.

The remainder of this paper is organized as follows. In Section 2, the design of the energy recovery clock generator is explained and a review of existing energy recovery clocked flip-flops is provided. In Section 3, the clock gating approach is proposed for energy recovery clocked flip-flops. In Section 4, negative edge triggered energy recovery clocked flip-flops are presented. Finally, Section 5 draws the conclusion of the paper.

2. Energy Recovery Clock and Flip-Flops

The designed energy recovery clock generator is shown in Fig. 1. The energy recovery clock generator is a single phase resonant clock generator. The clock generator is composed of a NMOS transistor M1, its drive circuitry and a lumped inductor connected to the DC supply which is half of the Vdd supply. Transistor M1 receives a pulse to pull down the clock signal to ground when the clock reaches its minimum, thereby maintaining the oscillation of the resonant circuit. This transistor is a fairly large sized transistor and is

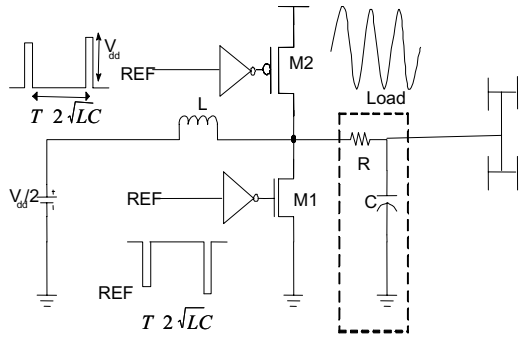

Fig. 1: Energy recovery clock generator

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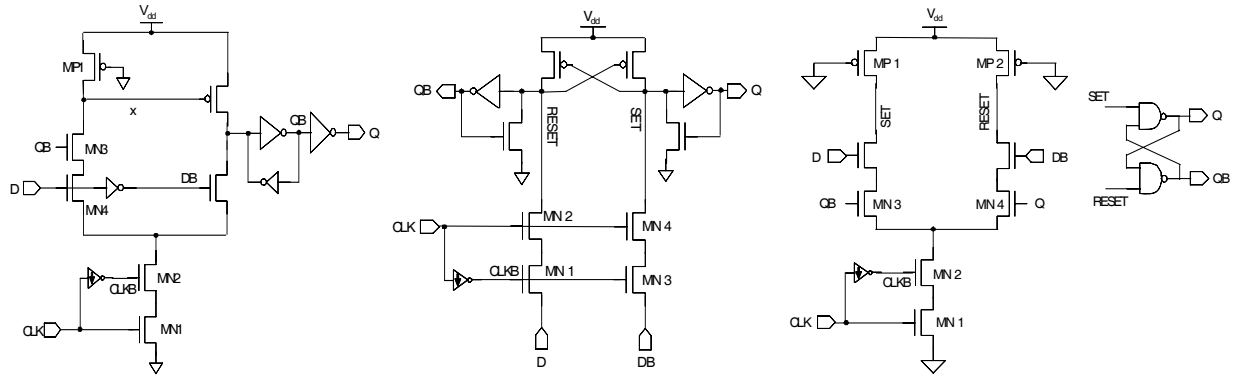


(a) SCCER **(b) SDER** **(c) DCCER**

Fig. 2: Energy Recovery Clocked Flip-Flops [3]

driven by an inverter.

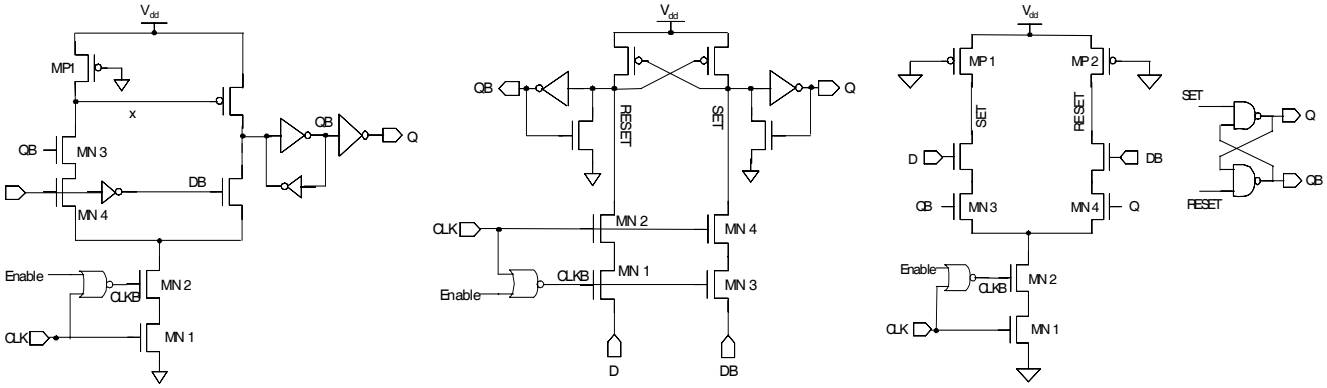
Without transistor M2, the clock generator would be vulnerable to process and temperature variations. The amplitude of the waveform would change with changes in temperature and process parameters because of the resulting change in resistances in the oscillation path. Such amplitude variation is not acceptable as it could result in flip-flop malfunction or timing uncertainties. The designed clock generator is made immune to process variations by adding a pull up transistor (M2) to the network as shown in Fig. 1. The pull up transistor M2 prevents variations in the oscillation amplitude. Transistor M2 receives a pulse which has the same frequency but is out of phase with the pulse of the pull down transistor by 180 degrees. The pull up transistor is activated when the waveform reaches its peak, and hence pulling up or clipping the waveform to the full supply amplitude. Therefore, the clock generator is not affected by changes in temperature or threshold voltage. The pull up transistor is a fairly large transistor and is responsible for making the clock generator robust. We simulated the clock generator at different temperatures and threshold voltages and measured the power consumed by the clock generator for the worst case scenario for the amplitude degradation (temperature of 100 C and high threshold voltage corner). The power dissipated by the clock generator under the worst case scenario is 4.26 mW at 160 Mhz.

The energy recovery clocked flip-flops capable of operating with an energy recovery clock have been proposed in [3] (Fig. 2(a), (b) and (c)). These flip-flops operate with sinusoidal clock signals and are more energy efficient than square wave flip-flops.

Fig. 2(a) shows the Single-Ended Conditional Capturing Energy Recovery (SCCER) flip-flop. Transistor MN3 which is controlled by the output QB provides conditional capturing. Fig. 2(b) shows the Static Differential Energy Recovery (SDER) flip-flop. The energy recovery clock is applied to a minimum sized inverter skewed for fast high to low transitions. Fig. 2(c) shows a Differential Conditional Capturing Energy Recovery clocked flip-flop (DCCER). The conditional capturing is implemented by using the feedback from the output to control the transistors MN3 and MN4.

3. Energy Recovery Clock Gating

As opposed to square wave clocking, the clock gating cannot be implemented by insertion of masking logic gates at any arbitrary node on the clock network. That is because insertion of such logic gates on a sinusoidal clock network destroys the shape of the clock and eliminated the energy recovery property in the downstream fanout capacitances of the clock network. Here, we propose a different approach to clock gating of energy recovery clock by inserting the gating feature inside flip-flops themselves. The energy recovery clocked flip flops (Fig. 3(a), (b), and (c)) cannot save power during sleep mode if the clock is still running. There are two components of power dissipation in flop-flops: clock circuit power (power of logic gates connected to the clock) and data circuit power (power of the rest of the flip-flop circuit). We



(a) Clock gating SCCER **(b) Clock gating SDER** **(c) Clock gating DCCER**

Fig. 3: Energy recovery clocked flip-flops with clock gating

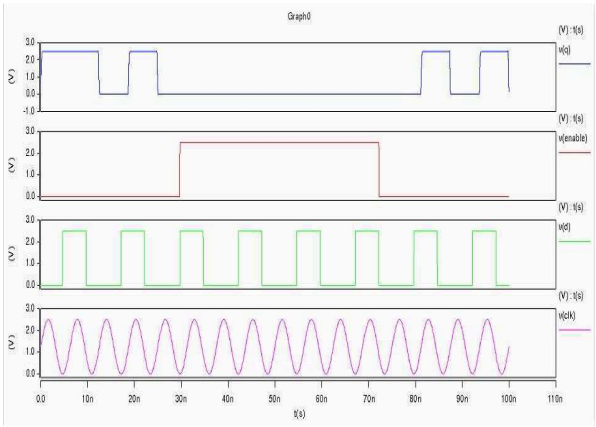


Fig. 4: Typical waveforms for SCCER flip-flop with clock gating

separated the clock circuit power from the data circuit power in our power measurements. Disabling the clock circuit (inverter gates connected to the clock input in Fig. 2) in the idle state can eliminate both the clock circuit and data circuit power. Hence, disabling of the inverter gates is the proposed approach to implementing clock gating inside energy recovery clocked flip-flops.

Fig. 3(a) shows SCCER with clock gating. Clock gating was implemented by replacing the inverter with the NOR gate. The NOR gate has two inputs: the clock signal and the enable signal. In the active mode, the enable signal is low so the NOR gate behaves just like an inverter and the flip-flop operates just like the original flip-flop. In the idle state, the enable signal is set to high which disables the internal clock by setting the output of the NOR gate to be zero. This turns off the pull down path (MN2) and prevents any evaluation of the data. Hence, not only the internal clock is stopped (clock power saving) but also all the internal switching is prevented (power saving on data circuits). Typical waveforms for SCCER flip-flop with clock gating are shown in the Fig. 4. A similar clock gating approach is applicable to other energy recovery clocked flip-flops. Fig. 3(b) and (c) show the SDER and DCCER with clock gating, respectively. The skewed inverter was replaced by a NOR gate. It should be mentioned that the skew direction for the NOR gate should remain same as that in the original inverter gate (skewed for high to low transition; pull-down network stronger than pull-up).

Table 1 shows results for the power consumed during the active mode for 50% data switching activity in both the original and clock gated flip-flops. It is observed that the clock gating does not introduce any power overhead. This is because of the use of small transistors in the NOR gates and also reduction in the short circuit power dissipated on the logic gates connected to the sinusoidal clock (the NOR gate shows less short circuit power than the inverter gate due to larger stack of transistors).

Table 2 shows results for the power consumed during the sleep mode for 50% data switching activity. Power results show significant savings when the clock gating is applied to the flip-flop during the idle state. Power savings of more than 1000 times are obtained during the idle state when compared to the power consumed without clock gating. The power savings increase with increase in the data switching activity.

Table 3 shows the delay comparisons between the original flip-flops and the flip-flops with clock gating. The results show that the clock gating addition has no impact on setup and hold time of the flop-flops. The delay overhead is caused by an increase in the clock to output (clk-Q) delay due to addition of NOR gates. The overhead in the data to output (D-Q) delay is less than 6.3%.

To show power savings due to clock gating, we integrated 1000 SCCER flip-flops through an H-tree clock network driven by the clock generator. The power saving by clock gating is dependent on sleep mode probability as shown in Fig. 5. The higher the sleep mode probability, the higher the power saving. For a sleep mode probability of

Table 1: Comparison of power consumption during active mode for 50% data switching activity (Numbers inside parentheses represent % overhead).

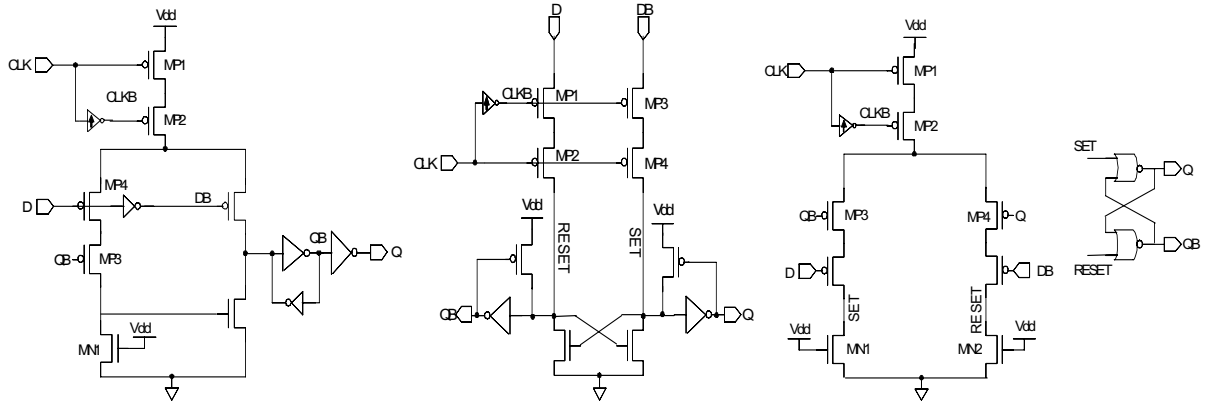
	Original flip-flops in Active Mode			Flip Flops with clock gating in Active Mode		
	Data power (µW)	Clock power (µW)	Total Power (µW)	Data power (µW)	Clock power (µW)	Total Power (µW)
SCCER	45.5	11.1	56.6	45.1 (-0.8%)	11.1 (0%)	56.2 (-0.7%)
DCCER	51.0	11.0	62.0	51.4 (0.7%)	10.8 (-1.8%)	62.2 (0.3%)
SDER	62.7	19.8	82.5	63.5 (1.2%)	18.9 (-4.5%)	82.4 (-0.1%)

Table 2: Comparison of power consumption during sleep mode for 50% data switching activity (Numbers inside parentheses represent % saving).

	Original flip-flops in Sleep Mode			Flip Flops with clock gating in Sleep Mode		
	Data power (µW)	Clock power (µW)	Total Power (µW)	Data power (µW)	Clock power (µW)	Total Power (µW)
SCCER	45.5	11.1	56.6	5.7 (99.9)	3.0 (99.9)	8.7 (99.9)
DCCER	51.0	11.0	62.0	1.1 (99.9)	3.2 (99.9)	4.3 (99.9)
SDER	62.7	19.8	82.5	11.6 (99.9)	2.8 (99.9)	14.4 (99.9)

Table 3: Comparison of delay for 50% data switching activity (Numbers inside parentheses represent % overhead).

	Original flip-flops				Flip Flops with clock gating			
	Set up Time (PS)	Hold Time (PS)	Clk – Q Delay (PS)	D-Q Delay (PS)	Set up Time (PS)	Hold Time (PS)	Clk – Q Delay (PS)	D-Q Delay (PS)
SCCER	40	60	232	277	40	60	237	282 (1.8%)
DCCER	140	130	184	329	140	130	205	350 (6.3%)
SDER	150	140	185	330	150	140	202	347 (5.1%)



(a) SCCER **(b) SDER** **(c) DCCER**

Fig.6: Negative edge triggered energy recovery clocked flip-flops

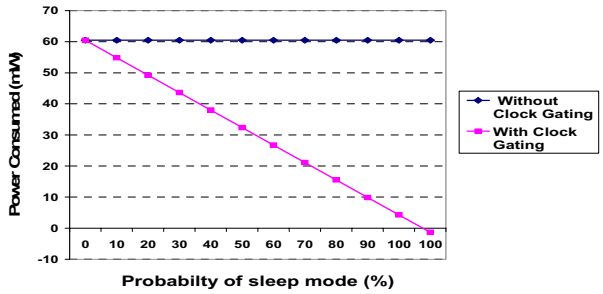


Fig. 5: Power savings due to clock gating

50% and data switching activity of 50%, the flip-flop clock gating technique reduces the system power by 47%.

4. Negative Edge Triggering

The existing energy recovery clocked flip-flops are positive edge triggered. In a synchronous system there is a need for both positive and negative edge triggered flip-flops. Unlike square wave flip-flops it is not possible to have negative edge triggering by simply inverting the clock signal. This is because inversion of a sinusoidal clock signals using an inverter gate destroys the signal and eliminates energy recovery property. Hence, negative edge triggering requires a separate design. The existing flip-flop designs can be modified to obtain negative edge triggering as shown in Fig. 6. Fig. 6(a) shows the negative edge triggered version of SCCER. The negative edge triggered SCCER is a complement of the positive edge triggered SCCER. Similarly the negative edge version of SDER and DCCER are devised by complementing their positive edge triggered design as shown in Fig. 6 (b) and (c). Table 4 shows the power and delay results obtained for the negative edge triggered flip-flops and their comparison with the positive edge triggered flip-flops. There is a considerable power overhead due to increase in number of PMOS transistors in the negative edge triggered flip-flops and also due to the larger sized PMOS transistors needed to obtain functional negative edge triggered flip-flops. There is no delay penalty for the negative edge triggered SCCER which ensures the same performance as the positive edge triggered SCCER. Negative edge triggered SDER has power savings compared to the positive edge triggered SDER. Negative edge DCCER performance is very similar to that of the positive edge triggered DCCER.

Table 4: Comparison of negative and positive edge flip-flops at 50% switching activity (Numbers inside parentheses represent % overhead)

	SCCER		DCCER		SDER	
	Positive Edge	Negative Edge	Positive Edge	Negative Edge	Positive Edge	Negative Edge
Power	56.6 µW	109 µW (92%)	62.1 µW	133 µW (114%)	82.5 µW	81.8 µW (-0.8%)
Delay (clk-q)	232p	194 ps (-16%)	184 ps	208 ps (13%)	185 ps	593 ps (220%)
Set up time	40p	70 ps	140 ps	170 ps	150 ps	120 ps
Hold time	60p	130 ps	130 ps	430 ps	140 ps	280 ps

5. Conclusion

We proposed a clock gating approach for energy recovery clocks. Clock gating in energy recovery clocked flip-flops result in significant power savings during the idle state of the flip-flops without any considerable overhead compared to the original flip-flops. Applying the proposed clock gating technique to the system of 1000 flip-flops with idle mode probability and data switching activity of 50%, reduces the total power by 47%. We also designed negative edge triggered energy recovery clocked flip-flops. Negative edge triggered flip-flops provide flexibility in designing an energy recovery system by having both positive and negative edge triggering options. Due to their considerable overheads compared to positive edge triggered flip-flops, negative edge triggered flip-flops should be used only when they are absolutely required.

6. References

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