# Robust Sense Amplifier Design under Random Dopant Fluctuations in Nano-Scale CMOS Technologies

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**Abstract**
*Variation in transistor characteristics and particularly threshold voltage (Vt) has emerged as a major challenge for circuit design in scaled technologies. Process variations result in increased mismatch among neighboring transistors which can affect the correct functionality of circuits such as sense amplifiers. In this paper, we will analyze the impact of process variations on sense amplifier circuits in detail. We will explore statistical design and optimization techniques based on transistor sizing to improve the reliability of sense amplifiers under process variations. Furthermore, we will exploit dual Vt option to enhance the sense amplifier robustness. According to simulation results in a 70nm process, by optimal transistor sizing and dual Vt assignment, failure probability of sense amplifiers can be greatly reduced (by more than 80%).*

## 1. Introduction

By scaling down of CMOS technology, transistor parameters such as channel length ($L$), width ($W$), oxide thickness ($T_{ox}$) and threshold voltage ($V_t$) scale down. However, variability in process parameters increases with technology scaling [1], resulting in unpredictability of circuit responses such as delay and power dissipation. Random dopant fluctuation is emerging as a major cause of intra-die random variations in threshold voltage of transistors in scaled technologies [1, 2]. Under random dopant fluctuations, even two adjacent transistors can have different threshold voltages which lead to functional failures in circuits that rely on matched transistors such as SRAM cells and sense amplifiers.

In this paper we analyze the failure mechanisms of different types of sense amplifiers under random dopant fluctuations. Then we analyze the impact of design parameters on failure probability of a sense amplifier. The design parameters that are considered include transistor sizing ($W$ and $L$), dual Vt assignment, and the number of fingers in transistor layout. Our analysis provides a statistical design approach for sense amplifiers in scaled technologies.

The organization of the paper is as follows. Section 2 presents the modeling of impact on Vt variation due to random dopant fluctuation. Section 3 discusses the failure mechanisms of sense amplifiers under random Vt variations. Then, design options for reducing failure probability of sense amplifiers are discussed in section 4. Based on the observations made in section 4, the overall results of the optimization of sense amplifiers are presented in section 5. Finally, Section 6 concludes the paper.

## 2. Vt Variation Due to Random Dopant Fluctuation (RDF)

Under random dopant fluctuation, threshold voltages of transistors (Vt) have independent random variations (δVt) following a Gaussian distribution with mean=0 and a variance given by [1]:

$$\sigma_{Vt} = \left[ \frac{qT_{ox}}{\varepsilon_{ox}} \sqrt{\frac{(N_a W_d)}{3L_{min}W_{min}}} \right] \times \sqrt{\frac{L_{min}W_{min}}{LW}} = \sigma_{Vt0} \times \sqrt{\frac{L_{min}W_{min}}{LW}} \quad (1)$$

where, $N_a$ is the effective channel doping, $W_d$ is the depletion region width, $T_{ox}$ is the oxide thickness, and $L_{min}$ and $W_{min}$ are the minimum channel length and width, respectively.

## 3. Failure Mechanisms in Sense Amplifiers

There are two commonly used latch-type sense amplifiers: (1) Current-Latched Sense Amplifier (CLSA) and (2) Voltage-Latched Sense Amplifier (VLSA) (Fig.1) [2].

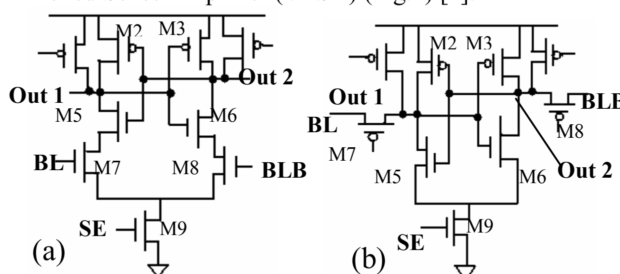


Fig.1 Two commonly used sense amplifiers: (a) Current-latched sense amplifier (CLSA) and (b) Voltage-latched sense amplifier (VLSA)

Due to process variations like random dopant fluctuations, Vt of transistors have random variations which cause mismatch among neighboring transistors. This mismatch can induce trip point mismatch among the cross-coupled inverters of sense amplifiers and/or current mismatch in the evaluation branches of the sense amplifier circuit, resulting in operational failures.

Referring to the circuit of CLSA, ideally, without parametric variations, the circuit is symmetrical. During precharge phase, output nodes are precharged to Vdd by the two precharging transistors. BL and BLB are applied to the circuit (e.g. $BL = V_{DD}$ and $BLB = V_{DD} - \Delta V$ ). Upon arrival of the sensing enable signal (SE), the circuit conducts and outputs start discharging. A stronger current is developed in M7 than M8 due to the higher gate input voltage (BL>BLB), thus making output 1 discharge faster than output 2. The rapid drop of output 1 turns on the strong positive feedback of the cross-coupled inverters and turns on the PMOS of output 2, thus charges output 2 back to $V_{DD}$. With output 1 continuing to discharge, a full swing signal is obtained between the output nodes resulting in a correct operation. However, under random threshold variations, transistor M7 might have developed a higher Vt than M8. In this case, even the gate input of M7 is higher than that of M8, the current induced in M8 could still be larger than that in M7. In this case, output 2 discharges faster than output 1 and the circuit flips in the wrong direction and hence resulting in an operational failure. This type of failure mechanism is activated by current mismatch and thus is not observed in VLSA since it does not operate base on current differential.

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The other failure mechanism induced by Vt variation is activated by trip-point mismatch among the cross-coupled inverters of the sense amplifier circuit which can happen in both types of sense amplifiers. Under threshold variation, different trip point voltages are developed for the two inverters in the circuit. The initial voltage difference at the output nodes created by either current difference (in the case of CLSA) or directly by bitline voltage difference (in the case of VLSA) may not result in the flipping of the cross-coupled inverters in the right direction if there is sufficient trip point voltage mismatch to offset the difference.

To estimate failure probability of a sense amplifier, Monte-Carlo simulations are performed in HSpice, where threshold variation of every transistor is represented as a Gaussian function given by Eq. 1. Therefore, random threshold variation can be generated for each transistor independently in each simulation. Simulations are repeated for 1000 times and failure probability of the sense amplifier is estimated as:

$$P(F) = \frac{\#\text{ of faulty cases}}{\text{total }\#\text{ of simulations}} \quad (2)$$

Failure probability strongly depends on Vt variation. With larger Vt variation ($\sigma_{Vt}$), failure probabilities of both sense amplifiers increase drastically (Fig.2). CLSA shows more failure probability than VLSA because it is susceptible to both current mismatch and trip-point mismatch.

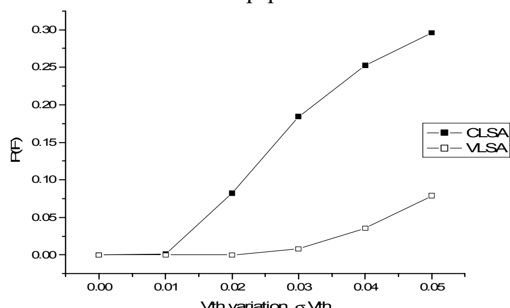


Fig.2 Effect of Vt variation on failure probability.

**4. Design Options for Reducing Failure Probability of Sense Amplifiers**

In this section, we consider three design options and investigate their effectiveness in improving the robustness of sense amplifiers. They are: (A) Transistor sizing, (B) Dual Vt assignment, and (C) Multiple finger layout structure.

**(A) Impact of Transistor Sizing**

Transistor sizing can affect failure probability in different ways. It can directly determine the threshold voltage variation due to random dopant effect (Eq. 1). It also affects the trip point mismatch and current mismatch because both of them are functions of Vt variation. In CLSA, the current difference induced in the two discharging paths determines the initial ΔV developed between the two outputs. The larger this value is, the greater the chances of correct evaluation. Sizing also determines the trip point voltages which determine when the cross-coupled inverters flip. This is crucial in the evaluation process for both types of sense amplifiers. Upsizing the NMOS of the inverter lowers its trip point voltage, which makes the cross-coupled inverters flip at a lower output voltage when there is more output voltage differential developed. This improves the probability of correct operation.

Critical transistors that determine failure probability are those in the discharging paths or cross coupled inverters, i.e. M2, M3, M5, M6, M7, M8 and M9. We chose a design with transistor sizing showing reasonable power, delay and failure probability, and then we observed the impact of length and width variations of each transistor independently.

It is observed that for both types of sense amplifiers, increasing the widths of M5 and M6 result in considerable reduction in failure probability (Fig.3). That is because increasing the widths of M5 and M6 decreases their Vt variation and lowers the trip point voltage. Increasing the width of M9 does not lower failure probability because it is a common transistor for the two paths and its variation affects both paths equally. Power dissipation increases by increasing widths of transistors (Fig.4). Transistor width increase typically reduces delay unless self-loading dominates. The impact of width of different transistors on sensing delay is shown in Fig.4. Notice that increasing the width of the bitline transistors (M7 and M8) results in delay increase due to the self-loading effect.

The impact of length of transistors is shown in Fig.5 and 6. Increasing length of M7 and M8 effectively reduces failure probability of CLSA because it reduces current mismatch. This can be theoretically explained as follows:

Using square-law current models the current of transistors M7 and M8 can be expressed as $I_{on} = \frac{1}{2}k'\frac{W}{L}(V_{dd} - V_t)^2$ Hence the variance of the current has the following relation with the variance of the threshold voltage: $\sigma_{Ion}^{\ 2} \propto \left(\frac{W}{L}\right)^2 \sigma_{Vt}^{\ 2}$ Since the variance of the threshold voltage is inversely proportional to sizing ($\sigma_{Vt}^{\ 2} \propto \frac{1}{WL}\sigma_{Vt0}^{\ 2}$) (Eq. 1), therefore:

$$\sigma_{I_{on}}^{\ 2} \propto \left(\frac{W}{L}\right)^2 \cdot \frac{1}{WL} \cdot \sigma_{Vth0}^{\ 2} \Rightarrow \sigma_{I_{on}}^{\ 2} \propto \frac{W}{L^3} \quad (3)$$

From Eq. 3, we could expect that increasing the length would significantly reduce current variation and hence lower failure probability. This justifies the trend observed in Fig.5. Eq. 3 also shows that increasing width of M7 and M8 increases current variation. That explains why increasing width of these transistors increases failure probability as shown in Fig. 3. For VLSA, upsizing lengths of M5 and M6 is effective because it reduces Vt variation and hence trip point mismatch. Increasing the length of transistors typically increases delay and power (Fig. 6).

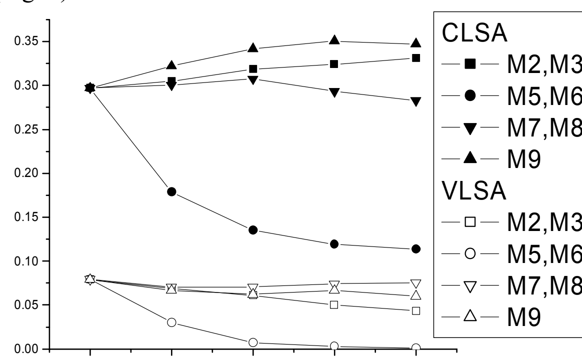


Fig.3 Impact of width of different transistors on failure probability.



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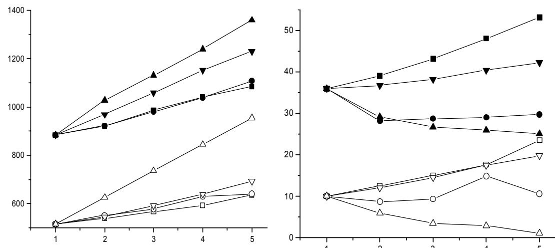

Fig.4 Impact of width of different transistors on power (left) and delay (right). (Same legend as Fig.3)

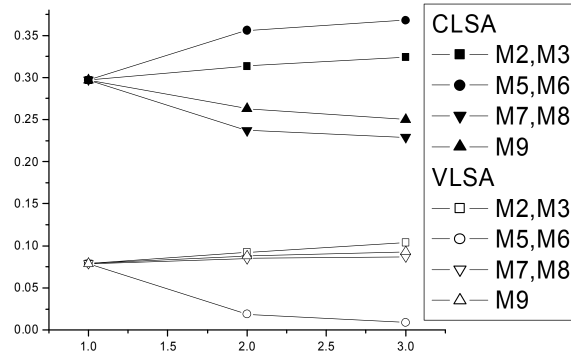


Fig.5 Impact of length of different transistors on failure probability.

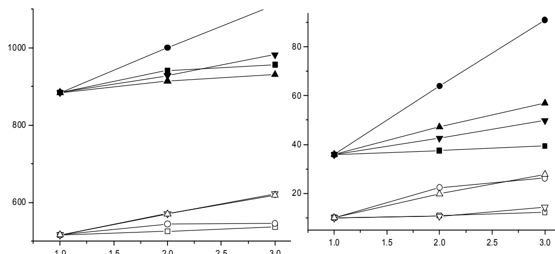

Fig. 6 Impact of length of different transistors on Power (left) and Delay (right). (Same legend as Fig.5)

**B. Dual Vt Assignment**

Dual Vt is a technology that provides optionally low or high threshold voltage for each transistor [5]. It was originally developed for leakage power reduction [5]. The impact of high or low Vt on Vt variation is negligible; however, similar to sizing, Vt affects the amount of current that flows through a transistor. The advantage of dual Vt over sizing is that Vt does not affect area and gate capacitance of the transistor and hence does not affect the area and switching power. Moreover, dual Vt can reduce leakage power. Here we consider the impact of dual Vt assignment on failure probability. With the options of low or high Vt for each critical path transistor in the circuit, there are altogether 16 combinations of dual Vt assignment for each sense amplifier scheme. Best Vt assignments for both sense amplifiers are shown in Table 1.

For CLSA, the best assignment is M2, M3, M5, M6 and M9 having low Vt and M7, M8 having high Vt. With this assignment, failure probability reduces by 29% without any power or delay penalty compared to all low Vt cases. In fact, there is some reduction in delay and power. Reduction in power is attributed to leakage reduction and delay reduction is due to reduction in the initial voltage of the common source node (common source of M7 and M8 is initially charged to $V_{DD}$-$V_t$ and has to be discharged to ground). As for VLSA, the best assignment is the original scheme where all transistors have low Vt. This shows that dual Vt assignment is not as helpful to VLSA as in the case of CLSA. This is because dual Vt assignment can control current flow through transistors which is helpful in CLSA but not in VLSA.

Table 1. Comparison of using dual Vt to improve sense amplifier robustness.

| | CLSA **without** dual Vt | CLSA- best case **with** dual Vt | VLSA best case - **without** dual Vt |
|---|---|---|---|
| M2,M3 | Low | Low | Low |
| M5,M6 | Low | Low | Low |
| M7,M8 | Low | High | Low |
| M9 | Low | Low | Low |
| **P(F)** | 0.297 | 0.210 (**↓26%**) | 0.079 |
| **Power(nW)** | 884 | 849 **(↓4%)** | 516 |
| **Delay(ps)** | 35.9 | 31.5 (**↓12%**) | 10.0 |

**C. Impact of Multiple Finger Layout Structure**

Multiple finger structure is a commonly used technique in layout design to implement large transistors because it provides better aspect ratio and less area for layout of large transistors. Implementing a large transistor in multiple finger structure is similar to having more number of smaller sized transistors in parallel that collectively show the same size (Fig. 7 shows the layout of single and multiple finger structure and equivalent schematics).

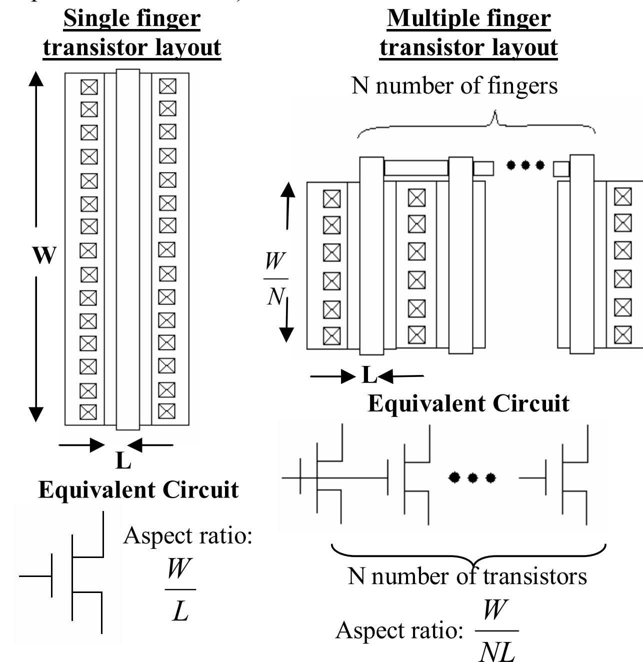


Fig.7 Layout and schematic comparison between single finger and multiple finger transistors.

Since Vt variation is inversely proportional to the size of a transistor (Eq. 1), multiple finger structure increases the variability of threshold voltage of each smaller transistor in the finger structure. This can be mathematically formulated as follows. A single finger transistor with size W/L has the following Vt variation:



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$$\sigma_{Vth} = K / \sqrt{WL}$$

where $K$ is a constant determined by process parameters (Eq.1) and W, L are the channel width and length, respectively. If this transistor is implemented in multi-finger structure with N number of fingers, each finger would have a width of (W/N), and hence Vt variation of each individual transistor is:

$$\sigma_{Vth}' = K / \sqrt{WL / N} = \sigma_{Vth} \sqrt{N}$$

Therefore, Vt variation of each finger increases with more number of fingers. However, the overall effect of variability of multiple-fingered transistor was found to be cancelled out due to the parallel structure in multiple finger layouts (the finger that shifts to high Vt cancels the effect of the finger that shifts to low Vt and vice versa) due to the property of randomness in dopant fluctuation. Hence, it is expected that multiple finger structure does not impact the robustness of sense amplifiers. This is observed from simulation results of using different number of fingers for transistors. Failure probability was found to be very much insensitive to number of fingers for any of the transistor (Fig. 8). Therefore it is concluded that multiple finger structure does not impact failure probability of sense amplifiers under random dopant fluctuation.

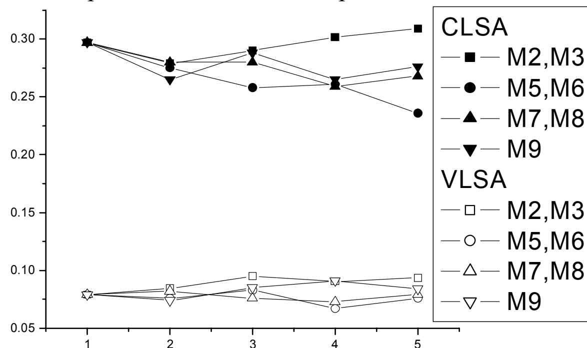


Fig.8 Impact on failure probability of increasing number of fingers for individual transistors.

## 5. Results of Optimization

Utilizing the design options studied earlier, we optimized the basic design of both the current-latched and voltage-latched sense amplifiers (basic designs are designs that are optimized for reducing power and delay only without considering failure probability).

Table 2 and 3 summarize the changes made after a statistical optimization considering failure probability. Results are obtained through Monte Carlo simulations using HSpice in a predictive 70nm technology. We observed an 81% reduction in failure probability in CLSA. 72% of the total improvement comes from transistor sizing and 26% comes from dual Vt assignment. As for VLSA, sizing is the only effective modification for improving robustness, but with the optimal sizing, failure probability can be reduced by up to 99%. It should be noticed that the decrease in failure probability comes with power and delay penalties compared to the basic design that is solely optimized for power and delay.

## 6. Conclusion

Robustness of sense amplifiers is degrading with increasing random dopant fluctuations in scaled technologies. In this paper, we explored statistical design and optimization techniques using transistor sizing, dual Vt assignment, and multiple finger layout structure. It is observed that optimal transistor sizing is very effective in improving robustness of sense amplifiers in scaled CMOS technology. Dual Vt assignment is also effective in improving robustness of CLSA without delay or power penalty. Multiple finger structure, however, does not affect failure probability in sense amplifiers.

Table 2 Overall optimization of CLSA.

| | **Basic CLSA** | **Optimized CLSA** |
|---|---|---|
| M2,M3 W/L (nm) | 100 / 70 | 100 / 70 |
| M5,M6 W/L (nm) | 100 / 70 | 400 / 70 |
| M7,M8 W/L (nm) | 200 / 70 | 200 / 140 |
| M9 W/L (nm) | 300 / 70 | 300 / 70 |
| M2,M3 Vt | Low Vt | Low Vt |
| M5,M6 Vt | Low Vt | Low Vt |
| M7,M8 Vt | Low Vt | High Vt |
| M9 Vt | Low Vt | Low Vt |
| M5,M6 fingering | 1 | 1 |
| M7,M8 fingering | 1 | 1 |
| M9 fingering | 1 | 1 |
| **P(F)** | **0.297** | **0.056 (↓81%)** |
| **Power (nW)** | **884** | **1059 (↑20%)** |
| **Delay (ps)** | **35.9** | **39.1 (↑9%)** |

Table 3 Overall optimization of VLSA.

| | **Basic VLSA** | **Optimized VLSA** |
|---|---|---|
| M2,M3 W/L (nm) | 100 / 70 | 100 / 70 |
| M5,M6 W/L (nm) | 100 / 70 | 500 / 70 |
| M7,M8 W/L (nm) | 100 / 70 | 200 /140 |
| M9 W/L (nm) | 300 / 70 | 300 / 70 |
| M2,M3 Vt | Low Vt | Low Vt |
| M5,M6 Vt | Low Vt | Low Vt |
| M7,M8 Vt | Low Vt | Low Vt |
| M9 Vt | Low Vt | Low Vt |
| M5,M6 fingering | 1 | 1 |
| M7,M8 fingering | 1 | 1 |
| M9 fingering | 1 | 1 |
| **P(F)** | **0.079** | **0.001 (↓99%)** |
| **Power (nW)** | **10** | **13.9 (↑39%)** |
| **Delay (ps)** | **516** | **765 (↑48%)** |

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