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A NOVEL LEAKAGE-TOLERANT DOMINO LOGIC CIRCUIT WITH FEEDBACK FROM FOOTER TRANSISTOR IN ULTRA DEEP SUBMICRON CMOS

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ABSTRACT: As the CMOS manufacturing process scales down into the ultra deep sub-micron regime, the leakage current becomes an increasingly more important consideration in VLSI circuit design. In this paper, a high speed and noise immune domino logic circuit is presented which uses the property of the footer transistor to alleviate the sensitivity of the dynamic node to noise and results in improved performance. The new circuit has been added to conventional footed standard domino logic for highly improving leakage tolerance, especially at the beginning of the evaluation phase. According to simulation results obtained using the 70nm Berkeley Predictive Models [1], our proposed circuit increases the noise immunity by least 2X compared to previous circuits.

INTRODUCTION

Domino logic circuits with high fan-in are widely used due to their high performance. Scaling down the supply voltage is known to be the most effective way to reduce power consumption. For lower power supply voltage, the threshold voltage of transistors also needs to be scaled down to meet performance requirements. However, the lowering of the threshold voltage leads to an exponential growth of subthreshold leakage current. Dual-threshold voltage techniques have been proposed by some researchers in order to solve this problem [2].
As the CMOS process scales down in the sub-100nm regime, the gate oxide thickness is scaled down to sub-20 Å. Such thin gate oxide leads to significant gate leakage currents by various direct tunneling mechanisms [3]. Moreover, increased gate leakage current has the potential to become the dominant factor for sub-100nm generations. Gate leakage models for MOSFET have been proposed [4, 5], and device and circuit level schemes to reduce gate leakage have been proposed [6, 7].
Several new domino circuits have been proposed such as HS domino [8, 9], STHS domino [10], and other circuits in the literature. These circuits improve noise immunity and performance, especially in high fan-in circuits. However, they have several shortcomings such as area overhead and increased dynamic power consumption due to the switching power of the devices added [11-12].
We have proposed two leakage-tolerant, high speed domino circuits in our previous papers [13, 14]. In our proposed circuits there are some shortcomings like area overhead, dynamic power consumption as well as the existence of a short circuit path between supply and ground.
We propose a new domino circuit that uses a feedback from the source of the footer transistor to improve noise immunity and performance simultaneously. This feedback reduces current through the keeper transistor due to the DC voltage of the drain of the footer transistor. The rest of this paper has been arranged as follows: in section two, some of the previous works will be described; in section three, the proposed circuit will be explained. Section four describes the results and comparison. Conclusions will be included in section five.

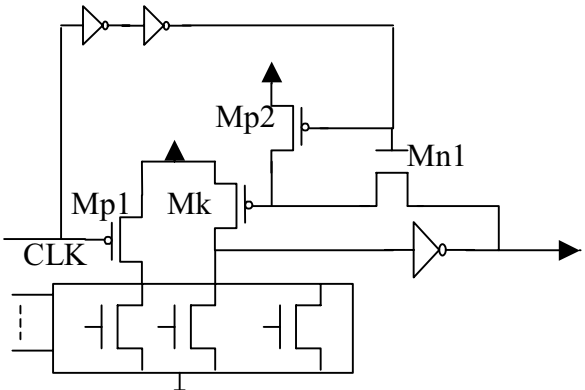

Fig.1. HS domino logic circuit

PREVIOUS WORKS

HS Domino

The schematic of the HS domino logic is shown in Fig.1. At the beginning of the evaluation phase, when clock is switched to high, PMOS MP2 is ON, so it turns off the keeper transistor MK. After the delays for the inverters, the PMOS transistor MP2 is turned off. If the dynamic node is discharged to ground and the output is high, the NMOS transistor MN1 remains off. But if the dynamic node remains high during the evaluation phase, then MN1 is turned on and pulls down the gate of the keeper transistor to low and turns on the keeper transistor.
However, since the keeper transistor is disabled, the dynamic node is floating at the beginning of the evaluation phase. If there is noise at the inputs, the

evaluation node may be discharged without the keeper. Node A can be Vdd – $Vt_{\_Mn1}$, where $Vt_{\_Mn1}$ is the threshold voltage of the NMOS transistor MN1. So, it results in a DC current through the PMOS keeper transistor and the NMOS logic tree.

Conditional Keeper Logic

Another existing leakage-tolerant domino circuit is the conditional keeper domino logic (CKL) [8]. The circuit schematic of the conditional keeper is shown in Fig.2. The circuit works as follows: at the beginning of the evaluation phase, the smaller keeper (P1) is ON for keeping the state of the dynamic node. After delay of the inverters, if the dynamic node is still high, the output of the NAND gate goes low to turn on P2. This keeper transistor is sized larger than P1 to maintain the state of the dynamic node for the rest of the evaluation period. However, the conditional keeper remains off if the dynamic node is discharged to the ground. CKL logic has some problems like limitations on decreasing delays of the inverters and the NAND gate to improve noise immunity. Noise immunity can be improved by upsizing delay inverters, but this significantly increases power dissipation [11-12].

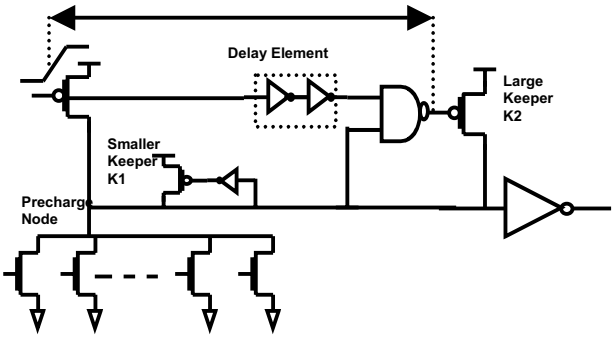

Fig.2. Conditional keeper domino

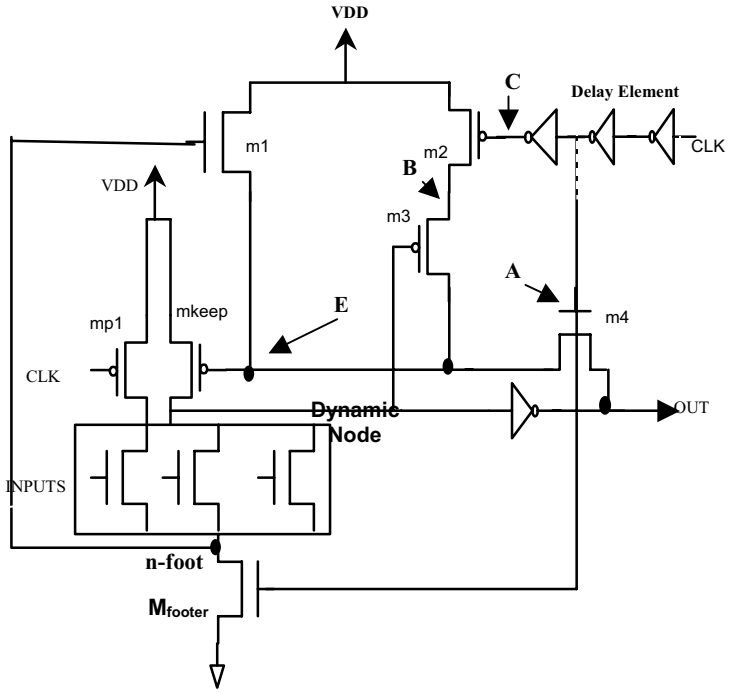

Fig.3. Proposed high-speed and leakage tolerant domino circuit

PROPOSED DOMINO CIRCUIT

We propose the use of feedback from the footer transistor as shown in Fig.3. When clock is low, assuming that circuit has been in standby mode (all inputs '0') during the evaluation phase, node A is high but nodes C, E, and OUT are low. Therefore, the keeper transistor remains ON. During the early stages of the precharge mode, the NMOS device M_{footer} remains turned ON, thus the M_{footer} node is connected to the ground. After a delay of the two inverters, the footer transistor and M_{footer} are turned off. Still, node C is low and node E starts to be charged a little. So, during the precharge mode, the PMOS devices remain off. Just the gate of the keeper transistor is charged a little. This causes a decrease in current through keeper transistor.
When clock is switched high, the precharge transistor MP1 is turned off. The states of the other nodes during the evaluation phase are as follows:

When All Inputs Are At Zero

1- Devices m4, m2, m3, and M_{footer} remain in off state. Considering the sizing of the evaluation transistors, the NMOS transistor m1 may be turned on by applying a small voltage to the gate. But we have upsized the evaluation transistor so that the N-foot node could not exceed the threshold voltage of m1. If this occurs, the power consumption is increased, but this would decrease the current of the keeper transistor.
2- At this time, the path of VDD to node E is disconnected. Transistor m4 is turned on, so it causes pulling node E to low. Thereby, m1 is off.
3- During the rest of the evaluation phase in this state, the keeper transistor remains on.

At Least One Input Is Switched To High

1- The dynamic node starts to discharge through the gate of transistor m1. The n-foot node starts to be charged through the evaluation transistors and causes transistor m1 to be turned on. Node E starts to be charged. Increasing the DC voltage of node E will result in more decrease in the voltage of source to gate of keeper transistor m1. So this causes a decrease in current through the keeper transistor. Therefore, it serves to mitigate the contention between keeper transistor and evaluation transistors. This has two effects on the circuit. First, this decreases the power consumption due to a decrease in current through keeper transistor and also the leakage current through evaluation transistor. Second, this decreases the subthreshold leakage current due to the stacking effect. The dc voltage present on node M_{footer} has three effects at the beginning of the evaluation phase:

1- If some transistors are in off state, this dc voltage causes the gate to source voltage of evaluation transistors to decrease. Therefore, this exponentially decreases the leakage current.
2- This voltage turns on the m1 transistor, which causes more decrease in the current of keeper transistor. This would alleviate the contention between keeper transistor and evaluation transistors.
3- Decreases the drain to source voltage of evaluation transistors, which causes the current flowing through to decrease.

After delays for two inverters, the voltage of M_{footer} node is grounded by transistor NMOS M_{footer} has been turned on. Node C is in high state, so the path of PMOS transistors, m2 and m3, is off. After the delay of an inverter, node C is switched to low, so the PMOS devices are turned on and charge the gate of keeper transistor and cause it to turn off. The waveforms of selected nodes are shown in Fig. 4.

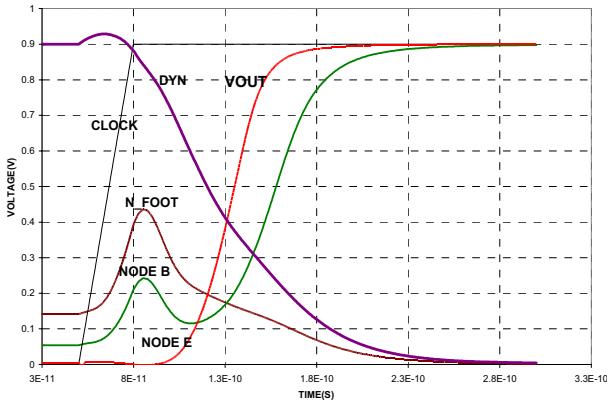

Fig.4. Waveforms of selected nodes in our proposed circuit

As shown in Fig.4, the voltage of node E exceeds even more than 0.2V, so it leads to a decrease in current through the keeper transistor at the beginning of the evaluation phase.

Noise Metrics

The noise metrics is the metric that has been employed in [4]. We apply a pulse noise to all inputs with an amplitude which is a fraction of supply voltage and a pulse width equal to 30ps. Then, the amplitude of the input noise pulse is increased until the amplitude of the resulting output noise voltage is equal to that of the input noise signal. This noise amplitude is defined as Unity Noise gain (UNG):

$$UNG= \{V_{in,}\ V_{noise}=V_{output}\} \quad (1)$$

SIMULATION RESULTS

We simulated our proposed circuit using predictive models for 70nm CMOS technology and at the high temperature of 110C. The supply voltage for circuit is 0.9V. Fig.5 shows the UNG versus delay to compare the proposed circuit with other circuits. As can be seen from Fig.5, for instance, for 16-in OR gate, the UNG of our proposed circuit for delay equal to 1.15, is 0.554, but UNG of CKL and HS domino logics at the same delay, is 0.21 and 0.124 respectively. So, our proposed circuit is suitable for high speed and noise immune applications.
In our proposed circuit, the minimum size for the keeper transistor has been used. So, for improving the performance of our proposed circuit, we used the feed back transistor, as shown in Fig.3 by m1. Meanwhile, we can use the keeper upsizing for improving the noise immunity of our proposed circuit. Upsizing the evaluation transistors and footer transistor can aid to increase the speed of our proposed circuit.
To compare the results and show the improvements achieved in noise immunity, the iso-delay test is used. The simulated results show an improvement in noise immunity even more than 2 times. So, the proposed circuit can be employed in high fan-in domino circuits for high noise immunity and high speed applications. Fig. 5 shows the results for UNG versus delay for some circuits.

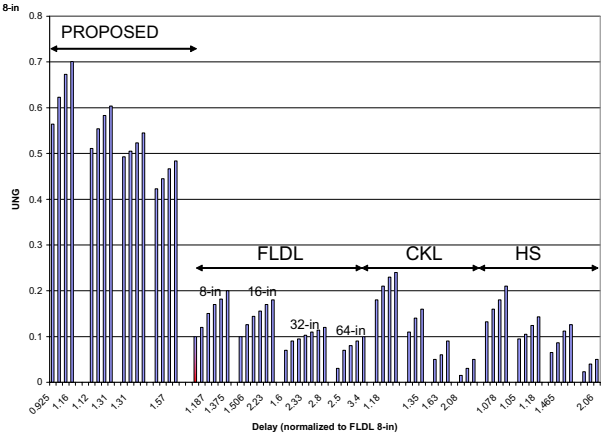

Fig.5. UNG vs. Delay for the proposed domino logic circuit

CONCLUSIONS

A new leakage tolerant, high speed domino logic circuit is presented in this paper. Simulated results show significant improvement in leakage tolerance and acceptable speed for high speed applications. Meanwhile we used minimum size for keeper transistor and also smaller size for the evaluation network. Therefore, the power consumption and area were decreased simultaneously in our proposed circuit.

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