Double-Gate SOI Devices for Low-Power and High-Performance Applications

Kaushik Roy*, Hamid Mahmoodi, Saibal Mukhopadhyay*, Hari Ananthan*,**
Aditya Bansal*, and Tamer Cakici*
***Dept. of Electrical and Computer Engineering, Purdue University, West Lafayette, IN**
****School of Engineering, San Francisco State University, San Francisco, CA**
*<Kaushik, sm, hanantha, bansal, cakici>@ecn.purdue.edu
** mahmoodi@sfsu.edu**

Abstract:

Double-Gate (DG) transistors have emerged as promising devices for nano-scale circuits due to their better scalability compared to bulk CMOS. Among the various types of DG devices, quasi-planar SOI FinFETs are easier to manufacture compared to planar double-gate devices. DG devices with independent gates (separate contacts to back and front gates) have recently been developed. DG devices with symmetric and asymmetric gates have also been demonstrated. Such device options have direct implications at the circuit level.

Independent control of front and back gate in DG devices can be effectively used to improve performance and reduce power in sub-50nm circuits. Independent gate control can be used to merge parallel transistors in non-critical paths. This results in reduction in the effective switching capacitance and hence power dissipation. We show a variety of circuits in logic and memory that can benefit from independent gate operation of DG devices. As examples, we show the benefit of independent gate operation in circuits such as dynamic logic circuits, Schmitt triggers, sense amplifiers, and SRAM cells. In addition to independent gate option, we also investigate the usefulness of asymmetric devices and the impact of width quantization and process variations on circuit design.

1. Introduction

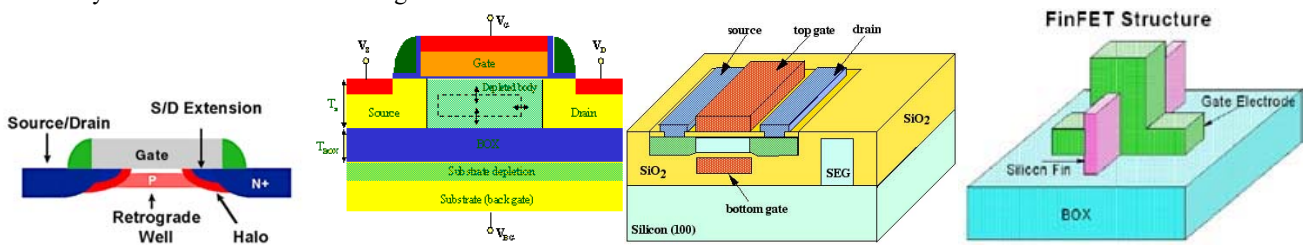
The scaling of conventional bulk CMOS technology is facing great challenges due to increased leakage and process variations with scaling down of device dimensions. Channel engineering techniques such as retrograde well and halo implantation are introduced to improve scalability and performance of such devices (Fig. 1(a)) [1,2]. However, the scalability of such a device structure is limited due to increased short channel effects [3]. This has motivated the need for non-classical silicon devices to extend CMOS scaling beyond 45nm node (Fig. 1(b-d)). Ultra thin body SOI FETs employ very thin silicon body to achieve better control of the channel by the gate, and hence, reduced leakage and short channel effects. Use of intrinsic or lightly doped body reduces threshold voltage (Vt) variations due to random dopant fluctuations [4] and enhances the mobility of careers in the channel region and therefore ON current. In these devices, there can be a weak common back gate that is shared as a common substrate among all the transistors. Such a process is referred to as Ground Plane SOI (GP-SOI) [31]. Better scalability can be achieved by introduction of a second gate at the other side of the body of each transistor resulting in a Double Gate (DG) SOI structure (Fig. 1(c)). Due to excellent control of short channel effects, double-gate SOI devices have emerged as the device of choice for circuit design in sub-50nm regime [5]. Low subthreshold leakage and higher ON current in DG devices make them suitable for circuit design in sub-50nm regime [6-7]. There are a variety of device structures suitable for double gate technologies. One of the promising structures is FinFET (Fig. 1(d)) [8]. Double gate devices with isolated gates (independent gates) are also being developed [9-10]. Independent gate option can be useful for low power and mixed signal applications [10-14].

Such developments at the device level provide opportunities for new ways of circuit design for low power and high performance. In this paper, we first review the device design options for the double gate device structures (Section 2). Then, we discuss the circuit design options using such devices for logic and memory applications (Section 3 and 4).

2. Double Gate SOI Devices

A classification of DG devices and their implications on circuit design is illustrated in Fig. 2. There are two main device processes possible for DG devices (Fig. 2 and 3), namely (a) symmetric device with same gate material (e.g. near-midgap metals) and oxide thickness for the front and the back gate [15-16] and (b) asymmetric device with different strengths for front and back gates. Different strengths can be obtained by using either different oxide thickness (asymmetric oxide) [17] or materials of different work-function (e.g. n+ poly and p+ poly) for the front and the back gate (asymmetric work-function) [15].

Regardless of the underlying device process, DG devices can also be classified in terms of their structure (Fig. 2). Typically the front and back gates of DG devices are connected together resulting in a 3-Terminal (3-T) device. 3-T devices can be used



(a) (b) (c) (d)

Fig.1: Scaled silicon devices: (a) advanced bulk MOS, (b) Ultra thin body SOI, (c) Planar double gate SOI, and (d) FinFET

Proceedings of the 19th International Conference on VLSI Design (VLSID'06)
1063-9667/06 $20.00 © 2006 IEEE

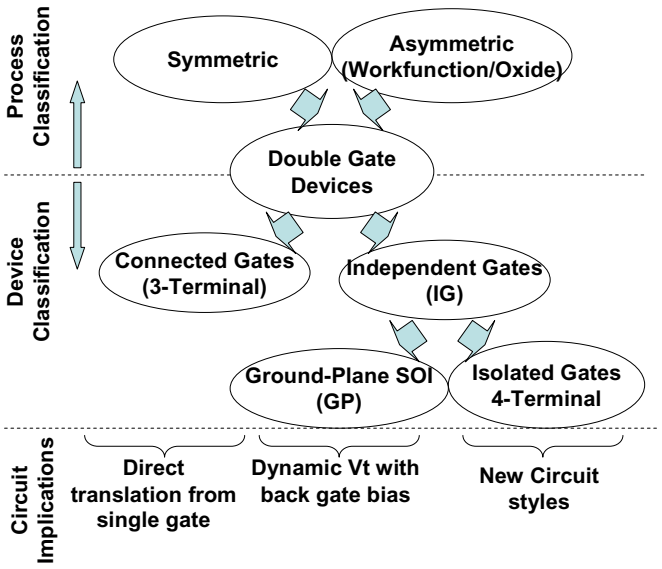


Fig. 2: Classification of double gate devices and their circuit design implications

for direct replacement of conventional single gate bulk CMOS devices. Recently, double gate devices with independent gate control option (separate contacts for back and front gates) have been developed [9-10]. Such DG devices are referred to as Independent or Isolated Gate (IG) devices (Fig. 2). The GP SOI process (Fig. 1-b) can also be considered as a class of IG devices with the exception that the second gate is shared among all the devices. GP SOI is attractive for dynamic Vt design with dynamic control of the common back gate bias (this will be further discussed in Section 2). IG devices with a second gate for each device are referred to as 4-Terminal (4-T) devices. In such technologies, one can choose to connect the back and front gates together or to control them separately while designing a circuit resulting in new circuit styles (some examples will be shown in Section 2). Connected back and front gates (3-T configuration) provides a simple way of mapping circuits designed in single gate technologies to double gates technologies. 3-T configuration provides more ON current for transistors as well [10]. On the other hand, independent gate control (4-T configuration) can be used for designing new circuit styles. For example, back gate bias can be used to dynamically adjust the threshold voltage of the front gate to tune the power and performance requirement of a circuit. It can also be used for merging parallel transistors or driving non-critical transistors in single gate driven mode to reduce power dissipation. These circuit design alternative in independent gate devices will be further discussed in Sections 3 and 4.

One of the major advantages of using double gate transistors is the lower leakage current. The major leakage components in double gate devices are: (a) subthreshold leakage and (b) gate leakage (Fig. 4) [18]. In double gate structures presence of two gates and ultra-thin body helps to reduce the Short-Channel Effect (SCE), which significantly reduces the subthreshold leakage current [32]. Lower SCE in DG devices and the higher driver current (due to two gates) allows the use of thicker oxide in DG devices compared to bulk-CMOS structures. This helps to reduce the gate leakage current. Moreover, lower SCE allows the use of lower body doping (body can even be intrinsic) in DG devices compared to bulk-CMOS structure. Hence, to induce equal inversion charge, DG devices require lower electric field compared to bulk-CMOS structure, which also helps to reduce the gate leakage current in DG devices [19]. Although leakage current is significantly reduced in DG devices, it is important to analyze different leakage current mechanisms in such devices. In particular, different double gate device options, principally, symmetric doped body poly gate devices (SymDG), symmetric intrinsic body mid-gap devices (MGDG) and asymmetric (n+ poly/p+ poly) intrinsic body (AsymDG) devices [7], have a strong impact on the different leakage components. Hence, it is necessary to analyze which DG device structure is most suitable for low-leakage circuit design. Let us now discuss the impact of different devices on the leakage currents:

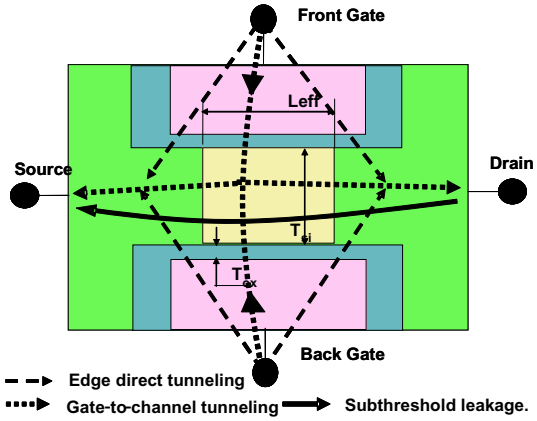


Fig. 4: DG device structure and different leakage mechanisms.

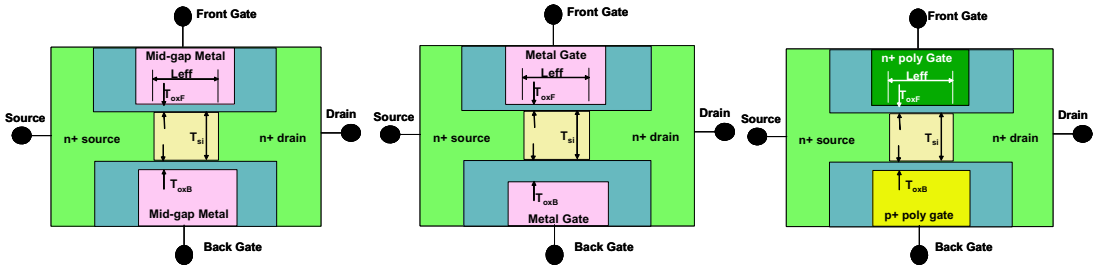


Fig.3: Processes of double-gate devices. (a) Symmetric device with near mid-gap metal gates, (b) Asymmetric device with different front and back oxide thickness and (c) Asymmetric device with front and back gate materials of different work-functions (eg. n+ poly/p+ poly) (L_{eff}=physical gate length, L_{gate}=drawn gate length, T_{si}=silicon thickness, T_{oxF}=front oxide thickness, T_{oxB}= back oxide thickness).

Proceedings of the 19th International Conference on VLSI Design (VLSID'06)
1063-9667/06 $20.00 © 2006 IEEE

(a) **Subthreshold Leakage:** Electrically coupled front and back gates and ultra-thin body reduce the short channel effect in double gate devices, resulting in a reduction of subthreshold leakage [19]. Moreover, for an equal "on" current MGDG device shows lower subthreshold leakage compared to the SymDG and AsymDG devices. This is due to the fact that, surface electric field is higher in poly gate devices (due to higher doping) and asymmetric devices (at the front gate due to large work-function difference between front and back gates) which reduces the mobility (due to higher surface scattering). Hence, for an equal "on" current MGDG device can be designed with a higher Vt compared to the SymDG and AsymDG devices. This is further enhanced by the elimination of poly depletion in MGDG devices (which is present in SymDG and AsymDG devices thereby lowering effective gate capacitance). Due to the higher Vt, for an equal "on" current MGDG device shows lower subthreshold leakage [18].

(b) **Gate Leakage:** Gate leakage in DG devices is due to gate to channel tunneling and overlap tunneling current. Due to the presence of lower body doping (as SCE is controlled by two gates and ultra-thin body) oxide field is lower in DG devices compared to bulk devices (for equal "inversion" charge") [19]. Hence, DG devices show lower gate-to-channel tunneling compared to bulk devices. This effect is more pronounced in MGDG devices as the body is intrinsic. Hence, midgap intrinsic body devices have lower gate-to-channel leakage compared to SymDG devices [18]. In AsymDG devices due to the work-function difference of front and back gates, front surface field is very high whereas back surface field is negligible. Hence, tunneling occurs only through front gate (which is larger than MGDG device but smaller than SymDG device) [18]. In the "off" state (Vgs=0, Vds=Vdd) overlap tunneling occurs due to tunneling of electron from gate to n+ drain. In MGDG devices (or in p+ poly back gate of AsymDG devices) overlap tunneling occurs due to tunneling of electron below the metal Fermi level (or due to electron tunneling from valance band of p+ poly). On the other hand, in SymDG devices tunneling occurs from conduction band of n+ poly. Since, the barrier height for tunneling of electron is higher in case of tunneling from metal gate (barrier height = Si-SiO_2 barrier height + Eg/2), MGDG devices show lower overlap tunneling leakage compared to SymDG devices. AsymDG devices have overlap leakage more than MGDG devices but lower than SymDG devices (as tunneling through back gate overlap is negligible) [18].

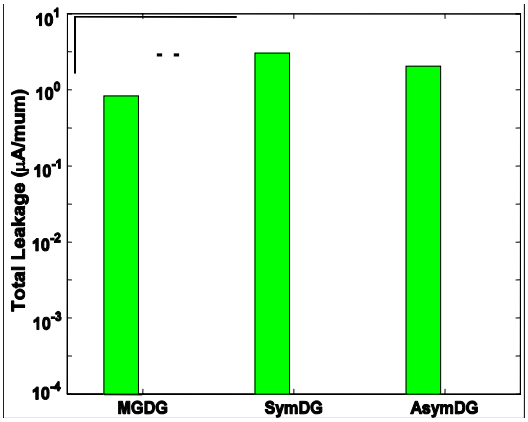


Fig. 5: Comparison of total leakage in DG devices

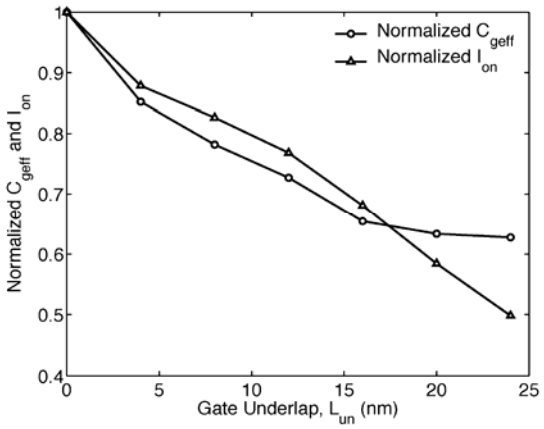


Fig. 6: Normalized on-current and effective gate capacitance vs. gate underlap.

From the above discussion, it can be observed that midgap and intrinsic body devices have lower subthreshold and gate leakage compared to other double gate structures. Fig. 5 shows the total leakage of MGDG, SymDG and AsymDG devices (L_{gate}=30nm, L_{eff} = 20nm, T_{si}= 5nm, T_{ox} =1nm, Vdd=1V) designed for equal "on" current [18]. It can be observed that, MGDG devices have lower total leakage current compared to SymDG and AsymDG devices. Hence, the use of mid-gap intrinsic body devices can be effective for designing low-power circuits [18].

(c) **Band-to-band tunneling (BTBT) of electrons:** BTBT across a reverse-biased p-n junction from the p-side valence band to the n-side conduction band is becoming an important component of leakage in nanoscale bulk and SOI CMOS technologies. It is manifested both as gate-induced drain leakage (GIDL) in the drain-gate overlap region and reverse-biased junction leakage in the halo-implant region. With double-gate CMOS likely to become the mainstream technology around the 45nm or the 32nm node, it is important to study the BTBT phenomenon in these devices. A detailed study and modeling of BTBT leakage for DG devices can be found in [20].

The device level parameters that impact power and performance include the geometrical parameters and the electrical properties of the materials used for gate (work-function). In particular, it is important to analyze the impact of gate electrode thickness and gate underlap on the fringe capacitance of nanoscale double-gate MOS transistors. Underlap can affect power and performance of DG devices as described in the remainder of this section.

An analytical fringe capacitance model considering gate underlap and finite source/drain length has been proposed (details can be found in [21]). A comparison with the simulation results shows that the model can accurately estimate the fringe capacitance of the device. An optimum gate underlap can significantly reduce the fringe capacitance resulting in higher performance and lower power consumption. With an increase in the gate underlap, the ON current also reduces. However, it can be shown that in extremely scaled gate length (<20nm) devices, fringe capacitance initially reduces faster than the ON current (Fig. 6), resulting in reduced intrinsic delay at an optimal underlap.

3. Logic Design using Double Gate Devices

A circuit designed in single gate technology (e.g. bulk-CMOS) can be directly translated to DG technology by replacing each transistor with a connected gate (3-T) DGMOS, where the front and the back gates are tied together. However, the directly translated circuit style does not utilize possibility of independent control of front and back gates (4-T configuration) [9-10]. The fabrication of both 3-T and 4-T DG on the same process has been recently reported [10]. We will observe that independent control of the front and the back gate can be very attractive for circuit design.

DG devices with connected back and front gates or 3-T DG devices show more ON current which is desired for high performance; however, they introduce larger gate capacitance loading, resulting in higher power dissipation. IG 4-T devices however can operate in single gate driven mode (zero back gate bias). They not only can be used for merging two parallel transistors with common source and drain terminal, but also as independent gates. Such a mode of operation reduces capacitive loading on inputs of the transistor and can be advantageous for power reduction. This mode of operation, however, results in ON current reduction and hence, the delay increases. Therefore, independent Gate (IG) devices can be exploited in non-critical paths to reduce the strength of the non-critical transistors. Such a mode of operation reduces capacitive loading on critical transistors, allowing them to be smaller in size for any target delay. We can also exploit lower capacitive loading and the possibility of having dynamic Vt control with back gate bias to design novel circuit styles. In this section several classes of circuits that can benefit from independent gate control are discussed.

3.1 Independent Gate Skewed Logic

In a pre-charge-evaluate logic such as skewed logic [22], the relative strengths of pull-up and pull-down transistors are modified in favor of a particular transition direction to achieve better delay. This modification, known as "skewing", increases I_{ON} of critical transistors and changes trip points in favor of the critical transition (low to high or high to low) [22]. A new way of skewing through use of IG 4-T devices (IG skewing in Fig. 7) has been proposed in [13]. In Fig. 7, significant skewing is achieved by connecting the back gate of the PMOS transistor to Vdd. Further skewing can be achieved by upsizing critical transistors. Skewing changes the trip point of a gate in favor of the critical transition. Based on the idea of IG skewing, a new skewed CMOS logic style is presented to improve performance and to reduce power dissipation. A chain of four inverters are

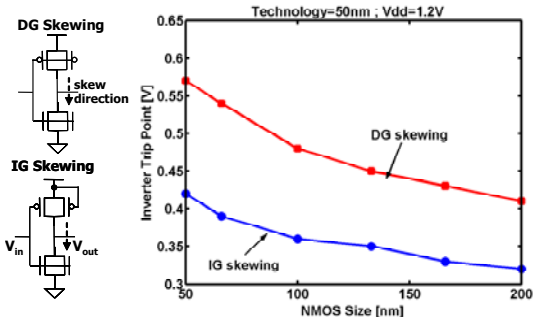


Fig. 7: Trip point of an inverter with Double Gate (DG) skewing and Independent Gate (IG) skewing (PMOS width is kept minimum)

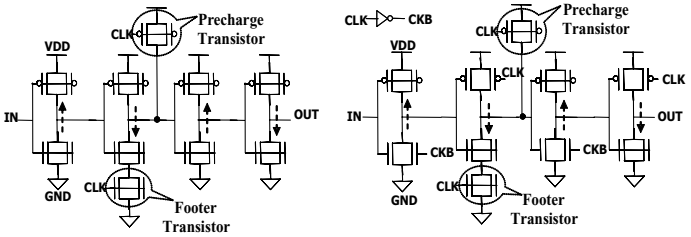


Fig. 8: Schematics of (a) DG and (b) IG skewed logic styles

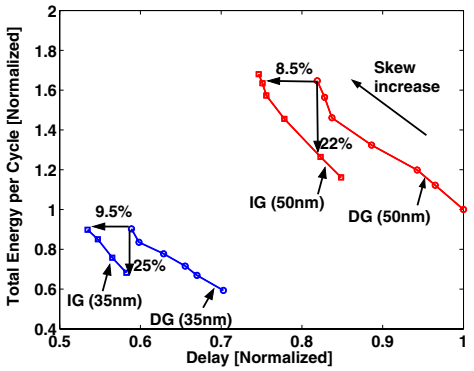


Fig. 9: Comparisons of DG and IG skewed logic styles (clock energy is included in total energy per cycle)

used to demonstrate the independent gate skewed logic style (Fig. 8).

As the gates are more skewed, the evaluation delay reduces; however, the pre-charge delay increases. The pre-charge delay should be as small as the evaluation delay in order to maximize speed. This can be achieved by selectively inserting PMOS pre-charge transistors on logic stages along with NMOS footers to avoid short circuit current (Fig. 8). As the evaluation delay decreases by skewing, the pre-charge delay has to catch up, which in turn requires upsizing the pre-charge transistors and/or inserting pre-charge transistors on more number of stages. To minimize power dissipation for any target delay, the number, location, and size of pre-charge transistors should be optimally chosen. The overall delay can be reduced by more skewing (less evaluation delay) and insertion of larger and/or more pre-charge transistors (less pre-charge delay). This results in an increase in the overall capacitance of the circuit and hence, larger energy dissipation.

In the IG skewed logic (Fig. 8(b)), back gates of non-critical transistors are connected to clock signals (CLK or CKB) to dynamically change the skew of the gates for the preferred transition in both evaluation and pre-charge phases. In the evaluation phase when CLK is high, back gates of PMOS and NMOS non-critical transistors are connected to Vdd and GND, respectively, providing significant skewing. Moreover, in the pre-charge phase when CLK is low, the back gates of these transistors are connected to GND and Vdd, respectively, resulting in faster precharging. Faster precharging helps in reducing the size of the inserted pre-charge transistors. The IG skewed logic achieves the same skewing as 3-T DG skewed logic with smaller sizes (less gate capacitance) for critical transistors, and therefore less power dissipation for a given target delay (Fig. 9). In the 50nm node, the IG skewed circuit shows savings of 22% in total energy per switching compared to its 3-T DG counterpart. Moreover, the delay is reduced by 8.5%. Since the double gate to single gate I_{ON} ratio increases with technology scaling, the energy savings of this logic style

1063-9667/06 $20.00 © 2006 IEEE

also increases with scaling (Fig. 9). In the 35nm technology node, the IG skewing technique shows a reduction of 25% in total energy per switching and 9.5% in delay compared to its 3-T DG counterpart.

3.2 Independent Gate Domino Logic

IG skewing is also applicable to domino circuits (Fig. 10) [12]. The static inverter of the domino circuit can be dynamically skewed for the preferred transition. The inverter is desired to be skewed for fast low-to-high transition during the evaluation phase and fast high-to-low transition during the pre-charge phase. These requirements can be simultaneously achieved by connecting the back gate of the NMOS transistor of the inverter to the inverted clock signal (CKB). The keeper transistor is also a 4-T IG device. The keeper is also assumed to be a minimum sized transistor (which is acceptable for typical low fan-in gates). In the IG domino logic, approximately half of the strength of the keeper is given to the pre-charge transistor by connecting the back gate of the keeper to the clock. Hence, the evaluation delay is further improved because the keeper strength is reduced by half and the loading of the keeper on the output node is reduced.

In IG domino, since the back gates of the keeper and NMOS of the inverter are connected to the clock, there is considerable pre-charge delay reduction at same sizing compared to DG domino. Hence, IG domino can use a smaller pre-charge transistor for the same pre-charge delay. Smaller pre-charge transistor is desirable for reducing energy. Moreover, due to dynamic skewing in the static inverter, the evaluation delay of IG domino is less than that of 4-T DG domino. Hence, at any target evaluation delay, IG domino can use smaller critical transistors (NMOS in the evaluation network and PMOS in the inverter), resulting in less energy (Fig. 11). As observed from Fig. 11, under same evaluation delay, energy reduction of 20%, and under same energy, delay reduction of 15% is observed.

It should be noted that, in IG skewed and IG domino logic

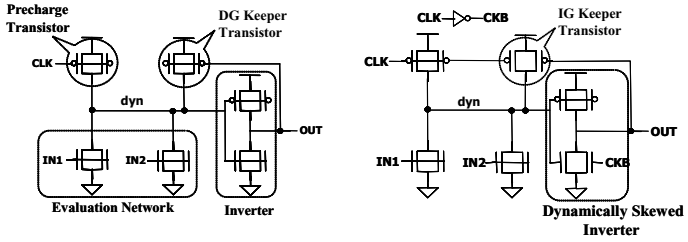


Fig. 10: Schematic of (a) DG and (b) IG domino logic styles

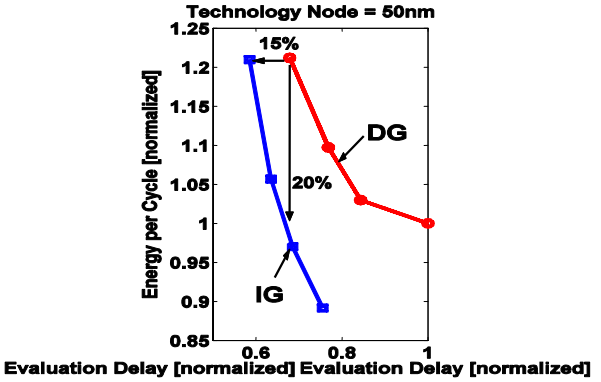


Fig. 11: Comparisons of DG and IG domino logic styles (clock energy is included in total energy per cycle)

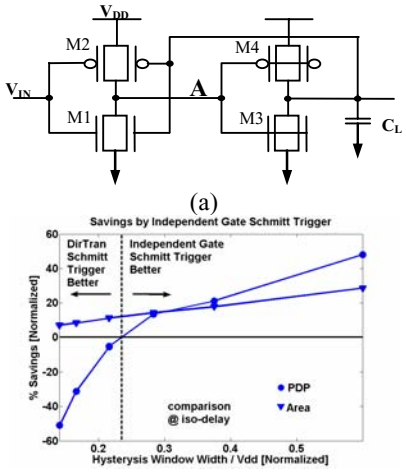


Fig. 12: (a) Low power four transistor Schmitt trigger (b) energy and area savings.

styles, when a 4-T transistor is OFF, both of its gates are at zero bias. Hence, the IG skewing technique does not cause any increase in leakage due to independent gate operation. In fact, there is leakage reduction due to the use of smaller transistors for any given target delay. Moreover, for 4-T transistors that are ON, the back gate bias is set at zero, only when they are not in a critical path.

3.3 Schmitt Trigger

The device/circuit co-design and trade-offs in area/speed/power can be well explained using Schmitt Trigger as an example. Schmitt Triggers are traditionally used as pulse shapers to reduce noise in digital circuits [23]. However, sizing up the Schmitt Triggers (to reduce the rise and fall times of signals) increases layout area and power dissipation of chips. A novel low power four transistor Schmitt Trigger for asymmetric double gate fully depleted SOI devices (Fig. 12) is presented in [14]. The first inverter stage of the new Schmitt Trigger exploits the independent gate technology. With the help of asymmetric devices the new scheme leads to reduced layout area and decreased short circuit power during switching compared to conventional six transistor Schmitt Trigger. At high noise immunity corner of the technology (L_{CH}=50nm, Vdd=1.2V), the new scheme shows 58% (30%) reduction in power dissipation (gate area) with 12% delay penalty (C_L=10fF) against that of conventional six transistor Schmitt Trigger.

3.4 Dynamic Vt using Back Gate Biasing in Ground Plane SOI

Dynamic back bias in bulk CMOS, where the transistor back terminal (well) is forward biased in active-mode and reverse biased in standby-mode (with respect to the source), is a popular way to achieve dynamic-Vt. Similarly, the independent back-gate terminal can be used for Vt modulation in Ground-plane (GP) SOI (Fig. 1-b). In Zero Back Bias mode (ZBB), the NMOS back-gate is tied to Vss and the PMOS back-gate to Vdd. Forward Back Bias (FBB) or Reverse Back Bias (RBB) can be applied at the ground-plane terminal to modulate front-channel Vt [24]. Forward-biased p-n leakage and reverse-biased band-to-band tunneling leakage (from drain to halo) reduce the effectiveness of back biasing in bulk. These problems are eliminated in GP SOI technology because the substrate is insulated from the device by the back oxide layer. Also, with

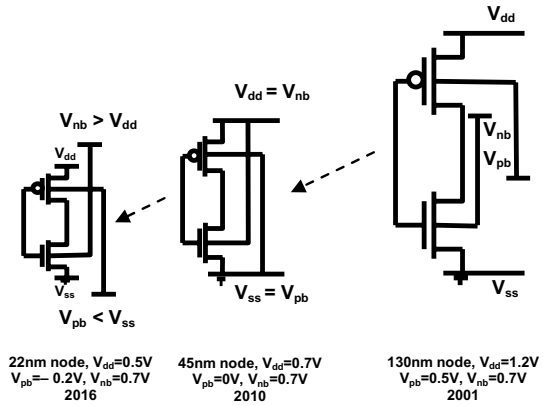


Fig. 13: Scaling scenario for Forward Back Bias

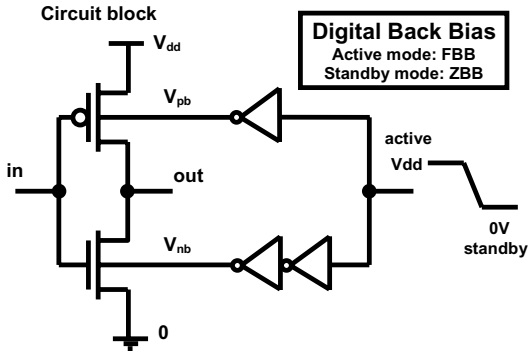


Fig. 14: Equal-to-Vdd Forward Back Bias

scaling, the body factor in bulk decreases with decreasing t_{ox}, while this problem can be solved in GP SOI by using a thinner back oxide and/or a thin body. Further, unlike bulk, junction capacitance is negligible to begin with, and the application of FBB/RBB does not affect it. Finally, unlike bulk, FBB/RBB does not impact front- channel sub-threshold slope (S) because the subthreshold slope S depends only on device structure. Thus, FBB and RBB are more attractive options for GP SOI than for bulk.

As Vdd is scaled to sub-0.7V, applying equal-to- and larger-than-Vdd FBB (Fig. 13) becomes attractive for two reasons. Conventional FBB schemes require the generation and distribution of separate back bias voltage levels using global and local analog bias generation circuitry. The V_{fbb} = Vdd scheme reuses Vdd and Vss rails for back biasing. Simple digital inverters can be used to generate and distribute the back bias signals (Fig. 14). Second, applying larger-than-Vdd FBB enables reverse back bias (RBB) in standby-mode by interchanging the active-mode biases. These schemes are found to achieve 97 − 99.5% standby leakage savings, 58% better performance and 0 − 8% lower active power compared to ZBB, at near-room temperatures [25].

4. Memory Design using Double Gate Devices

DG FinFET (Fig. 1(d) and 15) has emerged as the most manufacturable DG-SOI option. A silicon fin of thickness t_{si} is patterned on an SOI wafer. The gate wraps around either side of the fin (over the gate insulator of thickness t_{ox}). Current flow is parallel to the wafer plane (though occurring in an orthogonal crystal plane), while channel width is perpendicular to the plane (equal to 2h, where h is the height). Device width is quantized in increments of 2h.

4.1) Device Optimization for SRAM Cell

SRAM is likely to remain the largest, leakiest and most process-sensitive circuit block on chip. In this study, the impact of FinFET design choices on device and SRAM circuit metrics is investigated to understand how its unique properties can be suitably harnessed. Width quantization limits SRAM sizing choices, while quasi-planarity allows increased cell current by increasing fin height. Conversely, the latter property can be exploited to increase Vt and/or decrease Vdd to achieve exponential leakage savings at constant area and read access time. One can explore both approaches to selecting the right combination of device structure, Vt and Vdd that achieves maximum stability and minimum leakage over the design space [26-28]. Increasing Vt with fin height and body thickness improves stability, decreases variability and decreases source-drain leakage exponentially (Fig. 16). But this necessitates the use of small t_{ox} to control short channel effect; which in turn increases gate leakage exponentially. On the other hand, increasing Vt and decreasing Vdd allows the use of thicker t_{ox} to maintain short-channel effect and control gate leakage; however, this worsens stability. Therefore, careful co-design of device structure, Vt and Vdd is imperative to optimize SRAM metrics.

DGSOI such as FinFET can also be effective for low-power SRAM circuits [29]. Optimization of the gate sidewall spacer thickness (Fig. 17) is suggested to simultaneously minimize leakage current and gate capacitance to "on" current ratio [29]. Increase in spacer thickness increases the effective channel length resulting in reduced drain-induced-barrier-lowering, reduced gate-to-drain capacitance, reduced gate-to-drain tunneling leakage and reduced subthreshold leakage. Increased spacer thickness can result in gate underlap of the highly doped source/drain junction. This results in reduced gate sidewall fringe capacitance. The suggested optimization method also reduces the sensitivity of the device threshold voltage to the

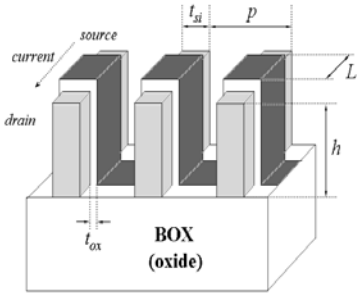


Fig. 15: DG FinFET structure

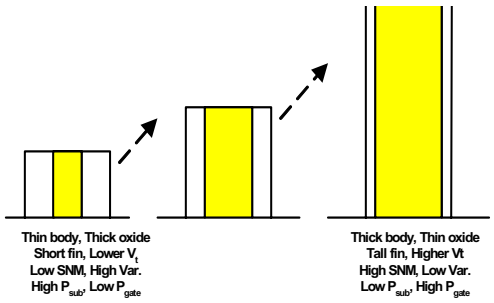


Fig. 16: FinFET design space for SRAM

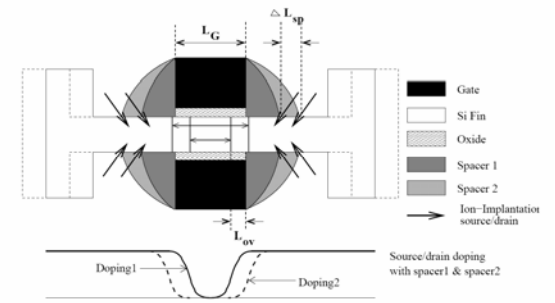


Fig. 17: FinFET schematic showing the effects of increase in spacer thickness.

process fluctuations in silicon thickness and gate length because of reduced short-channel-effects. Our analysis shows that optimization of spacer thickness results in around 70% reduction in SRAM cell leakage and reduced cell read failure probability (by 200X) compared to a conventional FinFET SRAM.

4.2) Sense Amplifier Design in DG SOI

Sense amplifiers are other critical elements in memories. The main design concerns in sense amplifiers include sensing delay, power, and tolerance to mismatch and process variations. It is shown that independent gate operation can be used to improve the design of a sense amplifier [11]. Fig. 18 shows two sense amplifier designs using 3-T and 4-T symmetric DG devices, respectively. Using the independent gate devices, the current difference in the two pull-down paths is achieved by using a single 4-T DGMOS in each path (N1 instead of NI1 & ND1 and N2 instead of NI2 & ND2) (Fig. 18-b). The front gates of N1 and N2 are connected in the cross-coupled inverter configuration whereas bitlines (BLB and BL) are connected to the back gates. When SE is turned "on", the front gates of N1 and N2 are at Vdd but the back gates are at different voltages

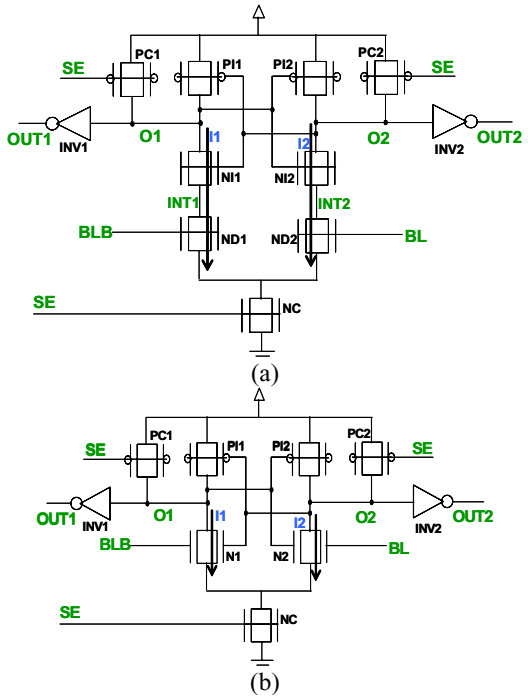


Fig. 18: (a) Directly translated sense amplifier circuit using 3-T DG devices and (b) independent gate sense amplifier using 4-T IG devices thickness.

(V_{BL} and V_{BLB}). This results in a current difference between the two paths which ensures the sensing operation. It can be observed that the Independent Gate control design principally operates as a dynamic threshold (Vt) circuit, where the threshold voltage of N1 and N2 are dynamically controlled by BL and BLB.

In the independent gate control sense amplifier, O1 and O2 are discharged through a 2-Transistor stack (instead of a 3-Transistor stack in 3-T design, Fig. 18a). Reducing the number of transistors in the stack (i.e. stack height) has three impacts, namely, (a) increase in the discharging current, (b) increase in current difference in two branches produced by the bitline voltage differential, and (c) increase in the gain of the cross-coupled inverters. Hence, the sensing delay in the independent gate control design is considerably less than that in the 3-T design. Also, in the independent gate control design, nodes O1 and O2 drive only the front gates of N1 and N2 instead of the front and back gates of NI1 and NI2 as in the 3-T design. This reduces the capacitive load on O1 and O2, thereby increasing the speed and reducing the switching power. It is also evident that the independent gate control sense amplifier has less number of transistors (NI1 and NI2 are eliminated).

Moreover, a voltage mismatch (in the worst-case direction) between nodes INT1 and INT2 in the 3-T design (before the start of the sensing operation) increases the sensing delay and may result in an incorrect operation. Such a mismatch can be due to coupling of noise and/or change in the strength of ND1 and ND2 due to process variations. However, this condition does not occur in 4-T design as nodes INT1 and INT2 are eliminated. Thus, the 4-T design increases the tolerance to noise and process variation.

In the 3-T sense amplifier, after the sensing operation, the back gate of the sensing transistor (N1 or N2) that is connected to the output node at '1', is not completely off (since bitlines are not completely discharged). Hence, that transistor is not completely "off" (V_{FGATE}=0 and V_{BGATE}=V_{BL}) which results in short circuit current through PI2, N2 and NC. The short circuit current increases power dissipation and reduces the voltage at node O2 from Vdd.

One way to prevent short circuit current is to design a circuit that decouples the front gates from the bitlines and discharges them to zero right after the sensing operation. Such a short

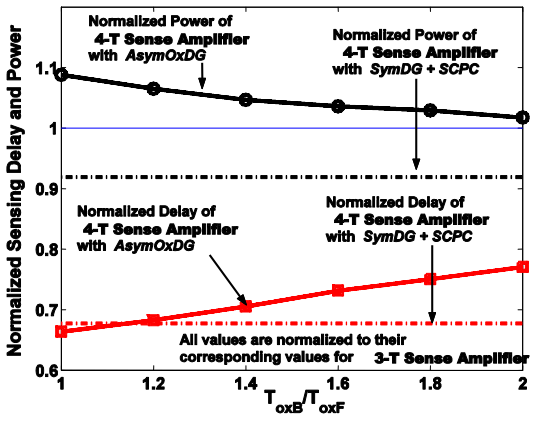


Fig. 19: Sensing delay and power of the 4-T sense amplifier with symmetric device (*SymDG*) + short circuit prevention circuit (*SCPC*) and oxide asymmetric devices (*AssymOxDG*).

circuit prevention circuit is proposed in [11]. The short-circuit power can also be reduced by using asymmetric devices for N1 and N2, and connecting the back gates to BLB and BL. In case of oxide asymmetry as Tox_B / Tox_F increases, the current through N1 with V_{FGATE}=0 and V_{BGATE}=V_{BL} reduces. A reduction in the short-circuit current reduces the short-circuit power and the noise voltage at O2. However, increasing T_{oxB} reduces the current difference between N1 and N2 produced by the difference in back gate bias. It also reduces the discharging current for nodes O1 and O2 by reducing the ON current of the transistors N1 and N2. Hence, the sensing delay increases with an increase in asymmetry (i.e. T_{oxB}). Similarly, the use of work-function asymmetric devices also reduces the short-circuit power and noise voltage at O2 at a cost of higher sensing delay.

The 4-T sense amplifier circuit with the symmetric device and the short circuit prevention results in a 33% reduction in the sensing delay and 10% (at 6GHz) reduction in the dynamic power compared to the 3-T design (sizes of the different transistors in the two designs were kept same). Application of the asymmetric devices reduces the short-circuit power but increases the sensing delay (Fig. 19). With oxide asymmetric *DG* at (T_{oxB}/T_{oxF})=2 the delay improvement is reduced to 24% (negligible power overhead) (Fig. 19). With work-function asymmetric DG at $\Delta\Phi_{MFB}$=1.1eV≈E_g, a negligible power overhead with a 20% delay reduction is observed. Due to the reduction in the number of transistors in the pull-down path, the sensing delay in the 4-T sense amplifier has a lower sensitivity to supply voltage, temperature, and load capacitance at nodes O1 and O2.

5. Conclusions

Due to reduced short channel effects, double gate SOI devices have emerged as the device of choice for nano-scaled technologies. The device characteristic including ON and OFF currents can be optimized by the choice of device geometries, gate material, work-function, etc. Possibility of independent gate double gate technologies (4-T devices) can be of significant advantage for low power and high performance circuit design. The usefulness of independent gate and asymmetric devices is shown in a class of low power and high performance circuits such as dynamic logic circuits, Schmitt trigger, SRAM cells, and sense amplifiers.

Acknowledgement

This work is supported in part by Semiconductor Research Corp. (#1078.001)

References

[1] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, New York: Cambridge Univ. Press, 1998.

[2] J. Jacobs and D. Antoniadis, "Channel Profile Engineering for MOSFET's With 100 nm Channel Lengths," IEEE Transactions on Electron Devices, vol. 42, pp. 870 –875, May 1995.

[3] 2004 International Technology Roadmap for Semiconductors, http://public.itrs.net/

[4] K. Takeuchi, et al., "A study of the threshold voltage variation for ultrasmall bulk and SOI CMOS," IEEE Trans. Electron Devices, vol. 48, pp. 1995–2001, Sept. 2001.

[5] L. Chang et al., "Extremely scaled silicon nano CMOS devices," Proc. of IEEE, vol. 91, pp. 1860–1873, Nov. 2003

[6] H-S.P. Wong, et. al, "Device design considerations for double-gate, ground-plane, single-gated ultra-thin SOI MOSFET at the 25nm channel length generation", in IEDM, 1998, pp. 407-410

[7] E. Nowak, et. al, "Turning silicon on its edge", IEEE Circuits & Device Magazine, Jan/Feb 2004, pp. 20-31.

[8] S. Tang, et al., "FinFET-a quasi-planar double-gate MOSFET," ISSCC, pp. 118-119, Feb. 2001

[9] D. Fried, et. al, "A Fin-type independent-double-gate NFET", Device Research Conference, 2003, pp. 45-46.

[10] L. Mathew, et. al, "CMOS vertical multiple independent gate field effect transistors (MIGFET)", Int. SOI Conf., 2004, pp. 187-188.

[11] S. Mukhopadhyay, et al., "Design of High Performance Sense Amplifier Using Independent Gate Control in Sub-50nm Double-Gate MOSFET," ISQED, pp. 490 – 495, Mar. 2005

[12] H. Mahmoodi, et al., "High Performance and Low Power Domino Logic Using Independent Gate Control in Double-Gate SOI MOSFETs," IEEE International SOI Conf., pp. 67-68, Oct. 2004

[13] T. Cakici, et al., "Independent Gate Skewed Logic in Double-Gate SOI Technology," IEEE International SOI Conference, Oct. 2005

[14] T. Cakici, et. al. "A low power four transistor Schmitt Trigger for asymmetric double gate fully depleted SOI devices," IEEE International SOI Conference, pp. 21-22, Oct. 2003

[15] J. Kedzierski, et. al., "High-performance symmetric-gate and CMOS-compatible asymmetric gate FinFET device", IEDM, 2001, pp. 437-440.

[16] J. Kedzierski, et. al., "Metal gate FinFET and fully depleted SOI devices using total gate silicidation", IEDM, 2002, pp. 247-250.

[17] S. Balasubramanian et. al, "Energy-Delay optimization of thin-body MOSFETs for the sub-15nm regime", IEEE Int. SOI Conference, 2004, pp. 27-29.

[18] S. Mukhopadhyay, et. al, "Modeling and Analysis of Total Leakage Currents in Nanoscale Double Gate Devices and Circuits", to be presented in ISLPED, 2005

[19] L. Chang, et. al., "Direct tunneling gate leakage current in double-gate and ultrathin body MOSFETs", IEEE TED, vol. 49, Dec. 2002, pp. 2288-2295.

[20] H. Ananthan, et al., Analysis of drain-to-body band-to-band tunneling in double-gate MOSFET, IEEE Intl. SOI Conf., 2005.

[21] A. Bansal, et al., "Modeling and Optimization of Fringe Capacitance of Nanoscale DGMOS Devices" IEEE Transactions on Electron Devices, Feb. 2005, vol. 52, no. 2, pp. 256-262.

[22] A. Solomatnikov et al., "Skewed CMOS: noise tolerant high-performance low power static circuit family," IEEE TVLSI, vol. 10, pp. 469–476, Aug. 2002

[23] J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall, 1996, pp 366-367.

[24] C. H. Kim, et al., Effectiveness of using supply voltage as back-gate bias in Ground Plane SOI MOSFET's. Proc. IEEE Intl. SOI Conf., 2004, pp. 69-70.

[25] H. Ananthan, et al., Larger-than-Vdd forward back bias in nanoscale bulk and double-gate SOI CMOS. Submitted to the IEEE Transactions on Electron Devices.

[26] H. Ananthan, et al., FinFET SRAM – device and circuit design considerations, Proc. ISQED, 2004, pp. 511-516.

[27] H. Ananthan and K. Roy, Technology-circuit co-design for width-quantized quasi-planar double-gate SRAM, Proc. ICICDT, 2005.

[28] H. Ananthan and K. Roy, Technology and circuit design considerations for width-quantized quasi-planar double-gate SRAM, Accepted for publication in the IEEE TED.

[29] A. Bansal, et al., "Modeling and Optimization Approach to Robust and Low-Power FinFET SRAM Design in Nanoscale Era," to be presented in the IEEE CICC, 2005.

[30] J.G. Fossum and K. Kim, "Extremely scaled double-gate CMOS performance projections, including GIDL-controlled off-state current", IEEE TED, vol. 46, no. 11, Nov. 1999, pp. 2195-2200.

[31]H. Wong, et al., "Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation," International Electron Devices Meeting, pp. 407 – 410, Dec. 1998.

[32] K. Kim, et. al, "Nanoscale CMOS circuit leakage power reduction by Double-Gate devices", ISLPED, 2004.