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Independent Gate Skewed Logic in Double-Gate SOI Technology

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Introduction:

Due to excellent control of short channel effects, Double-Gate SOI (*DGSOI*) devices have emerged as the device of choice for circuit design in sub-50nm regimes [1]. Reduced short channel effects in *DGSOI* alleviate the issue of leakage power. However, the overall power including the dynamic power still imposes a great challenge in future high performance designs. Therefore, there is a need for innovative low power techniques in *DGSOI* technologies. Double-gate SOI technologies with Independent front and back Gate control (*IGSOI*) have been developed recently [2,3]. We exploit *IGSOI* in noncritical paths to reduce the strength of the non-critical transistors below the minimum size. Such a mode of operation reduces capacitive loading on critical transistors, allowing them to be smaller in size for any target delay. In this paper, we propose an independent gate skewed logic style which achieves high performance and low power by exploiting the dynamic V_t and lower capacitive loading properties of *IGSOI* devices.

Device Characteristics:

In this work, we have designed symmetric double-gate SOI devices for 50nm and 35nm gate lengths (Fig. 1). The devices use metal gates with workfunctions that are within the range of reported manufacturable workfunctions [4]. The device and circuit simulations are done using TAURUS-DS [5]. In thin SOI devices, the quantization of electron energy in the body has a strong impact on V_t and gate capacitance, and hence, we have considered this quantum effect in our simulations.

Independent Gate Skewing:

In a precharge-evaluate logic, relative strengths of pull-up and pull-down transistors are modified in favor of a particular transition direction to achieve better delay. This modification, known as "skewing", increases I_{ON} of critical transistors and changes trip points in favor of the critical transition. Hence, skewing reduces the critical delay. We propose a new way of skewing through use of *IGSOI* (IG skewing in Fig. 2). In Fig. 2, significant skewing is achieved by connecting the back gate of the *PMOS* transistor to V_{DD}. Further skewing can be achieved by upsizing critical transistors. Skewing changes the trip point of a gate in favor of the critical transition.

As observed from Fig. 2, *IG* skewing changes the trip point in favor of the preferred transition (evaluation transition; in this case high-to-low at the output). For any given *NMOS* size, the *IG* skewed inverter has a smaller trip point. In other words, in the *IG* skewing case, a target trip point (skew) can be achieved with a smaller *NMOS* transistor. Hence, compared to *DG* skewing, *IG* skewing results in less switching capacitance, and therefore, less switching energy for the inverter at any target delay (as shown in Fig. 3(b)). The issue, however, is that as the evaluation delay reduces by skewing (Fig. 3(c)), the delay of the other transition direction (precharge delay) increases (Fig. 3(d)). Depending on the application, the precharge delay may not be acceptable beyond some skew, limiting delay reduction on the critical path. In the *IG* skewing, however, skewing can be dynamically changed for any preferred transition (dynamic *IG* skewing in Fig. 3(a)). For the inverter example in Fig. 3, in dynamic *IG* skewed gate, the back gate of the *PMOS* is connected to the clock signal (*CLK*) instead of V_{DD}. *CLK* is set to high and low, if the gate is in evaluation and precharge phase, respectively. Dynamic *IG* skewing significantly reduces the precharge delay (Fig. 3(d)). By dynamic *IG* skewing, the precharge delay is reduced to the precharge delay of the *DG* skewed inverter at any *NMOS* size.

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In the *IG* skewed circuit, the skewing is achieved by control of the strength (effective width and V_t) of the noncritical transistor through back gate bias. The strength of a transistor can be represented by its I_{ON}. The ratio of I_{ON} of double-gate drive (I_{ONDG}) to that of single-gate drive (I_{ONSG}) for a double gate transistor is greater than 2 since $|V_{tSG}|>|V_{tDG}|$, as shown in Fig. 4. This ratio increases by device scaling due to the increase in $V_{dd}-|V_t|$ ratio of *DG* to *SG* as the device is scaled down. Hence, the effectiveness of the proposed *IG* skewing technique improves with technology scaling. An increase in the I_{ON} ratio provides an opportunity to downsize the critical transistor in *IG* skewed circuits. Smaller sized critical transistors result in reduced power dissipation.

Independent Gate Skewed Logic Style:

Based on the proposed *IG* skewing, a new skewed *CMOS* logic style is presented to improve performance and reduce power dissipation. We have used a chain of four inverters to demonstrate the proposed skewed logic style as shown in Fig. 5. As the gates are more skewed, the evaluation delay reduces; however, the precharge delay increases. The precharge delay should be as small as the evaluation delay in order to maximize the performance. This can be achieved by selectively inserting *PMOS* precharge transistors on logic stages along with *NMOS* footers to avoid short circuit current (Fig. 5). As the evaluation delay decreases by skewing, the precharge delay has to catch up, which in turn requires upsizing the precharge transistors and/or inserting precharge transistors on more number of stages. To minimize power dissipation for any target delay, the number, location, and size of precharge transistors should be optimally chosen. The overall delay can be reduced by more skewing (less evaluation delay) and insertion of larger and/or more precharge transistors (less precharge delay). This results in an increase in the overall capacitance of the circuit and hence, larger energy dissipation.

In the *IG* skewed logic (Fig. 5(b)), back gates of noncritical transistors are connected to clock signals (*CLK* or *CKB*) to dynamically change the skew of the gates for the preferred transition in both evaluation and precharge phases. In the evaluation phase when *CLK* is high, back gates of *PMOS* and *NMOS* noncritical transistors are connected to V_{DD} and *GND*, respectively, providing significant skewing. Moreover, in the precharge phase when *CLK* is low, the back gates of these transistors are connected to *GND* and V_{DD}, respectively, resulting in faster precharging. Faster precharging helps in reducing the size of the inserted precharge transistors. The *IG* skewed logic achieves the same skewing as *DG* skewed logic with smaller sizes (less gate capacitance) for critical transistors, and therefore less power dissipation for a given target delay (Fig. 6). In the 50nm node, the *IG* skewed circuit shows savings of 22% in total energy per switching. Moreover, the delay is reduced by 8.5%. Since the *DG* to *SG* I_{ON} ratio increases with technology scaling (Fig. 4), the energy savings of this logic style also increases with scaling (Fig. 6). In the 35nm node, the proposed technique shows a reduction of 25% in total energy per switching and 9.5% in delay.

Conclusion:

Independent gate control of double gate SOI devices [2,3] can be effectively exploited to improve performance and reduce power in sub-50nm circuits. In this paper, we have proposed a skewed logic style using independent gate operation of double gate SOI devices.

References:

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[3] *L. Mathew, et al.*, IEEE SOI Conf., pp. 187-189, Oct. 2004
[4] *C. Cabral et al.*, Symp. on VLSI Tech., pp.184-185, 2004
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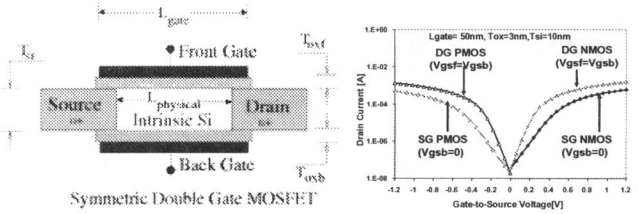

NMOS			PMOS		
Tech. Node	50nm	35nm	Tech. Node	50nm	35nm
L_{gate} (nm)	50	35	L_{gate} (nm)	50	35
$L_{physical}$ (nm)	40	28	$L_{physical}$(nm)	40	28
T_{oxf}=T_{oxb} (nm)	3	2	T_{oxf}=T_{oxb}(nm)	3	2
T_{si} (nm)	10	7	T_{si}(nm)	10	7
Vdd (V)	1.2	1.1	Vdd (V)	1.2	1.1
Workfunc. (eV)	4.55	4.51	Workfunc. (eV)	4.89	4.93
DG Vt (V)	0.28	0.3	DG Vt (V)	0.32	0.34
SG Vt (V)	0.37	0.39	SG Vt (V)	0.41	0.43
I_{ON} (μA/μm)	1470	1850	I_{ON} (μA/μm)	1290	1630
I_{OFF} (nA/μm)	31.9	30.1	I_{OFF} (nA/μm)	17.9	17.5
Sub. Swing (mV/decade)	70	70	Sub. Swing (mV/decade)	74	72
DIBL (mV/V)	55	53	DIBL (mV/V)	57	56

Fig. 1: Double Gate SOI devices and their characteristics

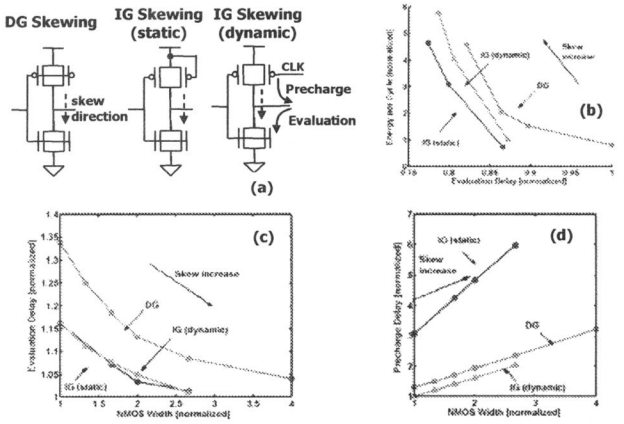

Fig. 3: Energy and delay advantage of Independent Gate (IG) skewing compared to Double Gate (DG) skewing

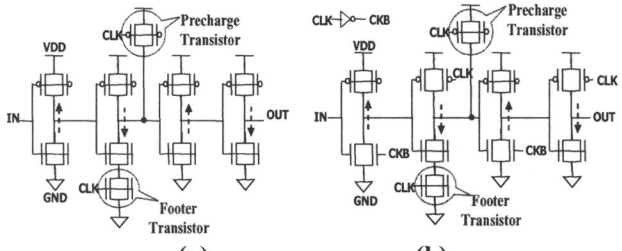

Fig. 5: Schematics of (a) DG and (b) proposed IG skewed logic styles

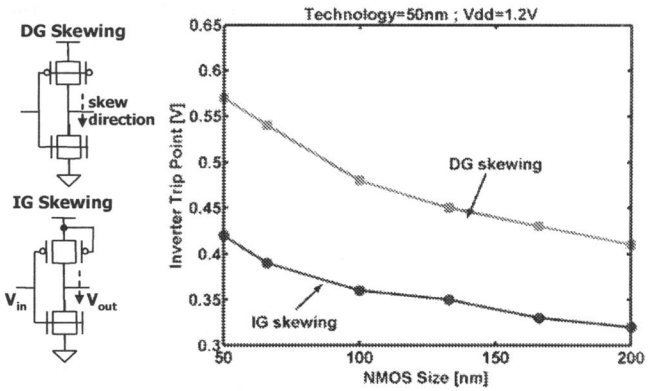

Fig. 2: Trip point of an inverter with Double Gate (DG) skewing and proposed Independent Gate (IG) skewing (PMOS width is kept minimum)

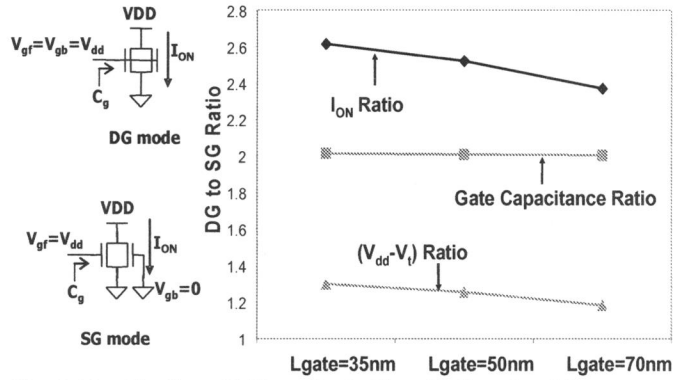

Fig. 4: Double Gate (DG) to Single Gate (SG) ratio of I_{ON}

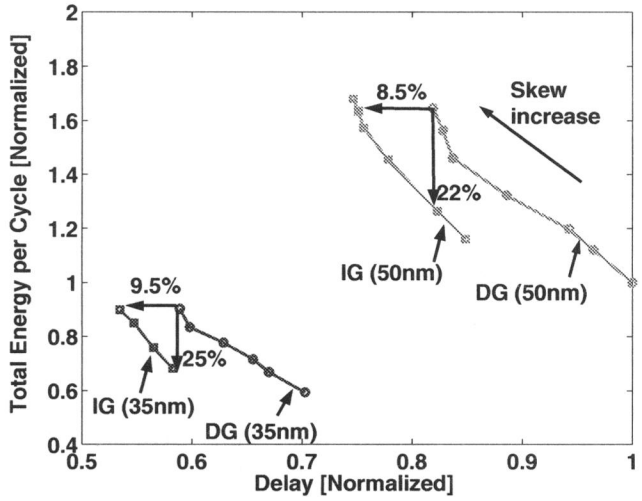

Fig. 6: Comparisons of DG and IG skewed logic styles (clock energy is included in total energy per cycle)