A Leakage Control System for Thermal Stability During Burn-In Test

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Abstract

Increase in leakage current with technology scaling has been a major problem for IC technology. This problem becomes more crucial during burn-in test where stressed voltage and temperature are applied. Due to presence of a positive feedback between major components of leakage and temperature in CMOS circuits, excessive leakage may lead to thermal runaway and yield loss during burn-in test. This paper describes a novel integrated leakage control system to ensure thermal stability during burn-in test for a wide range of ambient temperatures and process variations.

1. Introduction

To achieve higher transistor densities and performance, CMOS IC technology has been scaled aggressively in each generation. Higher integration density is achieved by transistor scaling. Along with scaling of dimensions, supply voltage (V_{dd}) has to be scaled down to meet power and reliability requirements. As V_{dd} is scaled, in order to maintain a sufficient transistor overdrive (V_{dd}-V_{th}) and achieve performance improvement, transistor threshold voltage (V_{th}) should be scaled as well. Lower V_{th} leads to a higher subthreshold leakage current (i.e. the current flowing through the device in its "off" state) [1]. Leakage current increases exponentially with scaling as shown in Fig. 1.1. Moreover, major components of leakage such as subthreshold leakage increase exponentially with temperature.

Due to such trends and the fact that the temperature of a die is high in the active mode of operation, leakage current becomes a major contributor to the total power consumption of a chip in scaled technologies (Fig. 1.2).

Leakage is particularly a major issue during burn-in test.

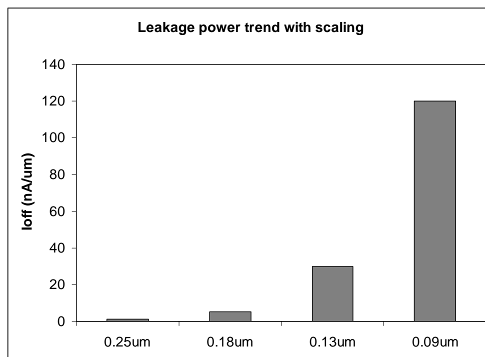

Fig. 1.1 Increase in leakage with technology scaling (Source: Intel Inc.)

Burn-in is an important test technique used to detect infant mortality types of defects which are caused by manufacturing anomalies and responsible for early-life failures. Leakage power is a dominating component of total power dissipation during burn-in test condition due to applied high supply voltage and temperature. By applying stressed supply voltage and temperature during burn-in, the aging of the chip is accelerated and the defects are detected [3]. Typically, the chip operates at low frequencies during burn-in, further reducing the fraction of total power consumption due to switching power. On the other hand, increased supply voltage and temperature further increases the leakage power. Thus leakage power is the dominant component of power consumption during burn-in test [2]. Due to presence of a positive feedback between temperature and leakage and the exponential dependence of (subthreshold) leakage on temperature, thermal runaway can occur during burn-in test if the leakage is not properly controlled.

In scaled devices, there are different leakage mechanisms contributing to the overall leakage. The major leakage mechanisms include [1]:

- Sub-threshold leakage
- Gate leakage
- Reverse biased drain-substrate and source-substrate junction Band-To-Band-Tunneling (BTBT) leakage
- Gate Induced Drain Leakage (GIDL)

Each of these leakage components has different dependence on transistor geometry, material properties, supply voltage and temperature. While gate leakage is relatively insensitive to temperature, sub-threshold leakage is a strong function of temperature. BTBT leakage also has temperature dependence since junction tunneling is a function of the band-gap, which is in turn a function of temperature. Such strong temperature

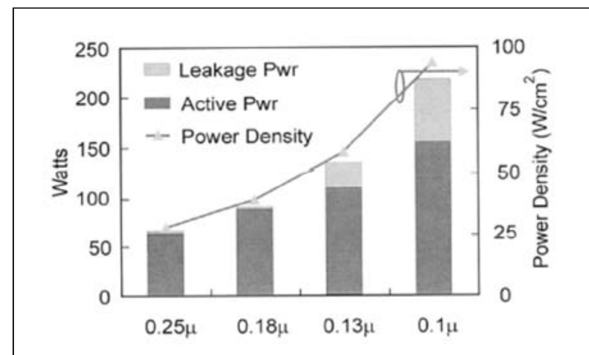

Fig.1.2 Active and Leakage power trend [16]

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dependence of the leakage components causes major thermal stability problems during the burn-in test. Due to stressed temperature conditions in burn-in, leakage components (especially sub-threshold leakage) increase and this further increases the junction temperature. In many situations, this may lead to thermal runaway. Such scenarios may be more common in nanometer technologies and may lead to yield loss and increased cost of burn-in [2], [20].

Another problem with scaled technologies during burn-in is the exponential increase in junction temperature due to drastic stand-by leakage power increase, higher transistor density and die-to-package thermal resistance increase as predicted in [2] and [5]. Since the burn-in temperature is close to reliability limits of temperature for silicon technology, advanced cooling techniques must be developed for each generation to keep junction temperature at an acceptable level [5].

Another important concern in nanometer technologies is process variation. Due to increasing variation of inter-die and intra-die process parameters, such as channel length, oxide thickness and random dopant fluctuations, threshold voltages of transistors vary, resulting in leakage variations across and within different dies [4]. During burn-in test, can will result in over-stress (die temperature higher than required) or even thermal runaway for the chips in the low-V_{th} process corners, or under-stress (die temperature lower than required) for chips in the high-V_{th} process corners.

To compensate for process variations and to prevent thermal runaway, junction temperature should be kept stable during burn-in. To achieve this, different methods have been suggested in literature. In [6] and [7], an electro thermal analysis tool was developed to observe thermal runaway possibilities due to leakage. The thermal runaway is avoided by predicting an ambient temperature which will keep junction temperature around 110ºC at burn-in conditions. However, this method is not reliable under variations in process, supply voltage, and ambient temperatures across the burn-in oven. In another work, different leakage reduction mechanisms are suggested to restrict the increase in leakage during burn-in [2]. In [8], the effectiveness of reverse body bias (the application of negative voltage between substrate and source) has been investigated for reducing the leakage during burn-in conditions. These methods cannot reliably control the leakage to avoid thermal runaway and ensure quality of burn-in test at the same time.

To the best of our knowledge, there has been no work done for stabilizing the junction temperature by controlling the leakage power of a chip. In this paper, we propose a novel negative feedback system to keep the junction temperature constant by controlling the body voltage of the transistors during burn-in. The proposed system continuously monitors the junction temperature and compares it with the target burn-in temperature. If the junction temperature is higher (lower) than the target temperature, the system decreases (increases) leakage current by decreasing (increasing) the reverse body bias of the chip.

The rest of the paper is organized as follows. Section 2 presents models for estimation of junction temperature during burn-in. Section 3 discusses the major leakage components. In section 4, temperature dependence of these leakage components is examined. Major problems in burn-in test are summarized in section 5. In section 6, leakage reduction techniques and the impact of body biasing on each leakage component is studied. In section 8, the proposed system for junction temperature control (and hence, thermal runaway prevention) during burn-in test is presented. Results of our analyses are presented in Section 9. Finally, the conclusions are drawn in Section 10.

2. Junction Temperature Estimation in Burn-in

Junction temperature (T_j) of an integrated circuit is defined as the temperature of the silicon substrate. T_j is formulated as follows [9]:

$$T_j = T_a + P \times R_{ja} \tag{2.1}$$

where T_a is the ambient or set-point temperature, P is the total device power and R_{ja} is the junction-to-ambient thermal resistance in steady-state. Moreover, the total power, P can be written as the summation of leakage and switching power.

$$P = P_{switching} + P_{leakage} \tag{2.2}$$

$$P_{leakage} = I_{leak} \times V_{dd} \tag{2.3}$$

$$P_{switching} = C \times V^2{}_{dd} \times f \tag{2.4}$$

where I_{leak} is the total leakage current, C is the total effective switching capacitance and f is the frequency during burn-in. In a burn-in environment, the chip is usually operated at lower frequency than the nominal frequency. Furthermore, due to stressed supply voltage and temperature, I_{leak}, and hence $P_{leakage}$ is larger than the nominal value. As a result, $P_{leakage}$ dominates the power dissipation during burn-in. Under these conditions, $P_{switching}$ can be neglected and Eq.2.1 can be re-written as follows:

$$T_j = T_a + I_{leak} \times V_{dd} \times R_{ja} \tag{2.5}$$

Expressing I_{leak} in terms of the leakage of a single transistor, $I_{transistor}$, T_j is expressed as:

$$T_j = T_a + \left(I_{transistor} \times N/2\right) \times V_{dd} \times R_{ja} \tag{2.6}$$

where, N represents the effective number of transistors in a chip considering the stacking effect. Assuming a fully

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static CMOS design, half of transistors (N/2) are 'off' and therefore leaking during burn-in.

3. Leakage Components

To effectively control the junction temperature of the chip using leakage power, it is necessary to understand each component of leakage current and its dependence on temperature.

3.1 Sub-threshold Leakage

In the "off" state of a MOS transistor ($V_{gs} < V_{th}$), the diffusion current flowing between source and drain is defined as the sub-threshold current, which can be expressed as [10]:

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L}(m-1)(\frac{kT}{q})^2 e^{q(V_g - V_{th})/mkT}(1 - e^{-qV_{ds}/kT}) \quad (3.1)$$

where V_{th} is the threshold voltage, C_{ox} is the gate oxide capacitance, μ_{eff} is the effective mobility and m is the body effect coefficient (also called sub-threshold swing coefficient).

3.2 Junction Leakage (BTBT)

In CMOS devices, p-n junctions formed by drain-substrate and source-substrate are typically reverse biased. This results in a small minority carrier diffusion/drift current across the junction. In scaled technologies, in order to decrease the Short Channel Effects (SCE) caused by Drain-Induced-Barrier-Lowering (DIBL), higher substrate doping density and "halo" profiles are used [1]. This increases the junction leakage (or band-to-band-tunneling leakage) through the reverse biased drain-substrate and source-substrate junctions. BTBT current density can be expressed as [10]:

$$J_{b-b} = A\frac{EV_{bs}}{E_g^{1/2}}\exp(-B\frac{E_g^{3/2}}{E})$$
$$A = \frac{\sqrt{2m^*}q^3}{4\pi^3\hbar^2}, and\ B = \frac{4\sqrt{2m^*}}{3q\hbar} \quad (3.2)$$

where m^* is the effective mass of electron, E_g is the energy band-gap, E is the electric field at the junction, $\hbar$ is $1/(2\pi)$ times Plank's constant and V_{bs} is the applied reverse bias. Assuming a one-sided junction, the electric field at the junction is given by [10];

$$E = \sqrt{\frac{2qN_a(V_{bs} + \psi_{bi})}{\varepsilon_{si}}} \quad (3.3)$$

where N_a is the concentration of the lightly doped side, ε_{si} is the permittivity of silicon, and ψ_{bi} is the built-in voltage across the junction.

3.3 Gate Leakage

With scaling, in order to maintain reasonable SCE immunity, the gate oxide thickness is reduced, which results in an increase in the electric field across the gate oxide. The thin oxide and the resulting high electric field across the oxide allow significant electron tunneling through the oxide. This leakage component is called Gate Leakage which is given by [11]:

$$J_{DT} = A(V_{ox}/T_{ox})^2 \exp\left[\frac{-B(1-(1-V_{ox}/\phi_{ox})^{3/2})}{V_{ox}/T_{ox}}\right] \quad (3.4)$$

where J_{DT} is the gate leakage current density, V_{ox} is the potential drop across the thin oxide, T_{ox} is the oxide thickness and Φ_{ox} is the barrier height for the tunneling particle (electron or hole). Finally, A and B are the physical parameters given in [11]. During burn-in conditions, due to stressed V_{dd}, gate leakage will increase and its effects should be examined.

3.4 GIDL

As the increased electric field in and around drain junction under the gate results in field crowding, high electric field effects such as avalanche multiplication and band-to-band tunneling become worse. The resulting increased reverse-biased junction leakage current is called gate-induced drain leakage (GIDL) and is given by [12]:

$$I_{GIDL} \propto AE^{5/2}\exp(-B/E) \quad (3.5)$$

where E is the electric field in the gate-to-drain overlap region; $A \propto E_G^{-7/4}$ and $B \propto E_G^{3/2}$ are constants; and E_G is the band-gap energy.

For scaled technologies, typically GIDL is negligible compared to sub-threshold leakage and masked by the presence of junction BTBT current. However, during burn-in, due to stressed V_{dd}, GIDL will increase and its effects should be examined.

4. Temperature Dependence of Leakage Components

In order to use leakage components in stabilizing the temperature of the chip during burn-in, temperature dependence of each leakage component has to be analyzed. Simulations have been performed using HSPICE [17] for a 50nm minimum size NMOS device with zero body bias augmented with voltage controlled current sources to include the effects of gate and BTBT leakage [13]. V_{dd} was increased by 30% which is the stressed supply voltage during burn-in conditions. The nominal V_{dd} value for the simulated technology is 0.9V. Fig.4.1 shows individual components and total leakage vs. temperature.

Sub-threshold leakage is a strong function of temperature due to exponential dependence of this component on temperature (Eq. 3.1). In case of GIDL and BTBT, the electric field across the oxide and the junction does not strongly depend on temperature. However, the band-gap of silicon reduces with increased temperature. This results in an increase in both BTBT and GIDL with temperature (Eq.3.2 and Eq.3.5, respectively). Simulation results confirm this trend for BTBT as shown in Fig.4.1. GIDL for this particular transistor was negligible for all

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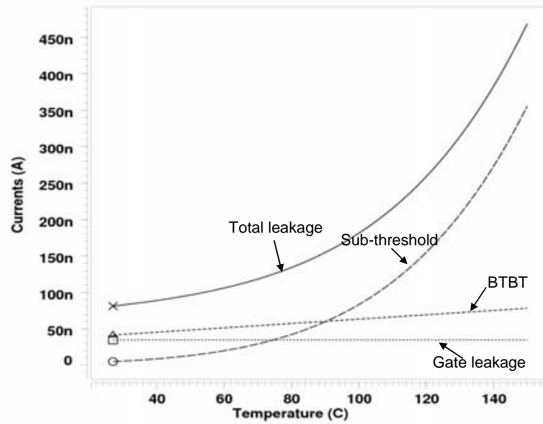

Fig.4.1 Temperature dependence of leakage components

temperatures and hence not shown in the figure. Finally, based on Eq.3.4, gate leakage is insensitive to the temperature (Fig.4.1).

5. Challenges in Burn-in Testing

Typically, during burn-in, temperature is chosen at 110 ºC and supply voltage is raised to 30% higher than nominal supply [7]. As shown in Figure 4.1, total leakage of the chip increases significantly with temperature due to exponential temperature dependence of sub-threshold leakage. Under burn-in conditions (~110ºC), high leakage current will further increase the junction temperature (Eq.2.6). In many cases, this may create a positive feedback between leakage and temperature leading to thermal runaway. As leakage increases with scaling, this problem will become more critical in future technologies. To avoid thermal runaway, a thermo-electrical tool was developed in [7], and a range of ambient temperature was found for any given process technology. As shown in [7], it is impossible to avoid thermal runaway using air-cooled ovens for scaled technologies, and hence, liquid cooled and refrigeration ovens (which have lower R_{ja}) were suggested.

Process variations pose new challenges during burn-in. Chips in the low V_{th} process corner are leakier than those in nominal and high V_{th} corners. Hence, they are more susceptible to thermal runaway because of larger leakage

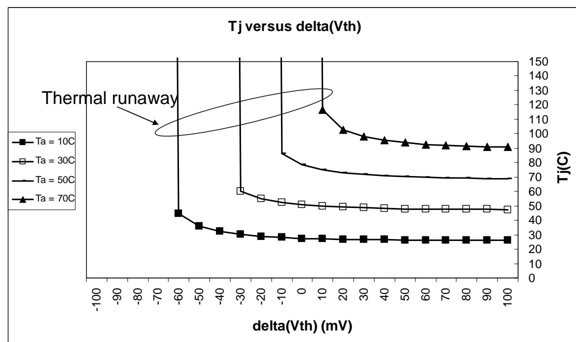

Fig.5.1 Effects of process variations on T_j

currents. Thermal runaway for low V_{th} chips results in yield loss during burn-in. Moreover, since chips with lower V_{th} are faster, losing them due to thermal runaway costs more than losing chips with nominal or high V_{th} leakage [6]. Even if thermal runaway does not occur, lower V_{th} chips will experience more stress (higher temperature) which may again cause yield loss. On the other hand, chips with higher V_{th} may not experience enough thermal stress and may decrease the reliability of burn-in test.

Fig. 5.1 shows that under process variation (inter-die threshold voltage variation), thermal runaway can occur for a large range of ambient temperatures even as low as 10ºC. In order to avoid thermal runaway for a larger range of process variations, the ambient temperature has to be reduced. However, with reduced ambient temperatures, the junction temperature cannot reach the required burn-in temperature (110ºC).

Because of process variations and the difficulty in estimating the total leakage of a microprocessor, the method suggested in [6] is not sufficient. Furthermore, dynamic power which is usually neglected during burn-in is application dependent and not predictable. Therefore, applying a low ambient temperature for stabilizing a high junction temperature is not a reliable solution. Hence, there is a need for a real-time integrated temperature control of the chip to avoid thermal runaway during burn-in.

6. Leakage Control Techniques

To avoid thermal runaway during burn-in, the exponential increase in leakage current has to be prevented. Several circuit techniques such as multi-threshold logic, stack effect, and body bias have been used to reduce the leakage current [1]. In all these techniques, the goal is to reduce leakage. However, to the best of our knowledge, there has been no work which stabilizes T_j at a target temperature.

In our method, we control (not necessarily reduce) the leakage to adjust the junction temperature at the target burn-in temperature. The leakage power is modified depending on the present value of the junction temperature. More specifically, junction temperature of the chip is decreased (increased) by decreasing (increasing) leakage power. Supply voltage scaling is one way of changing the leakage power. However, since supply voltage is a very sensitive parameter in acceleration process, it will affect the time to breakdown parameter of burn-in testing, and hence is not a suitable method of leakage control during burn-in. Another way to control the leakage current is body bias. Since performance is not critical during burn-in, body bias can be applied to the whole chip to control leakage. To use

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body bias in leakage control, it is crucial to understand the body bias dependence of each leakage component.

6.1. Impact of Body Bias on Leakage Components

Threshold voltage (V_{th}) of a transistor can be expressed as [10];

$$V_{th} = V_{fb} + 2\psi_B + \frac{\sqrt{2\varepsilon_{si} q N_a (2\psi_B + V_{bs})}}{C_{ox}} \qquad (6.1)$$

where, V_{fb} is the flat-band potential, ψ_B is the difference between Fermi potential and intrinsic potential and V_{bs} is the applied reverse body bias. From Eq.6.1, application of reverse (forward) body bias increases (decreases) threshold voltage. Hence, sub-threshold leakage reduces (increases) exponentially with reverse (forward) body bias (Eq.3.1).

Junction BTBT leakage however, has opposite dependency on body bias. As reverse body bias is increased, the electric field across the junction will increase (Eq.3.3). Thus, both E and V_{bs} in Eq.3.2 will increase, resulting in an increase in junction BTBT leakage.

Body bias dependence of GIDL can be understood using Eq.3.5. Neither electric field in the gate-to-drain overlap region nor the band-gap depends on body bias. Hence, GIDL is not a function of body bias. Similarly, gate leakage also does not depend on body bias (Eq.3.4).

Simulations are performed to study the impact of body bias on different leakage components and results are plotted in Fig. 6.1.1. A minimum size NMOS transistor with 30% higher V_{dd} is simulated at room temperature (27ºC). Note that GIDL is not shown in the figure since it was negligible for this device.

Simulation results verify the above theoretical discussions. It also demonstrates that there is an optimal body bias voltage for minimum total leakage as presented in [13]. However, this figure does not show the temperature dependence of leakage components together with body bias dependence. In order to analyze the leakage currents at burn-in conditions, the simulations are

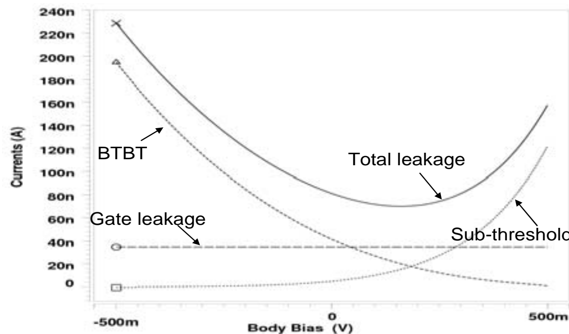

Fig.6.1.1 Body bias dependence of leakage components at 27ºC

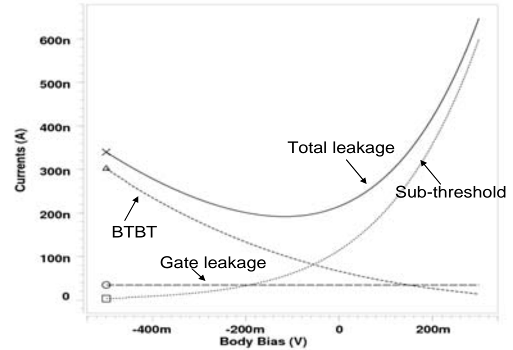

Fig.6.1.2 Body bias dependence of leakage components at 110ºC

repeated at 110ºC (Fig.6.1.2).

Fig.6.1.2 shows that junction BTBT leakage increases linearly with reverse body bias under burn-in conditions. On the other hand, the exponential dependence of both forward body bias and temperature on sub-threshold leakage leads to unacceptable leakage currents during burn-in. Note that, the simulations are performed with -0.5V to 0.3V body bias. In the forward (positive) body bias region, the leakage is dominated by the subthreshold leakage and is too sensitive to body bias. Such strong sensitivity makes leakage control using forward body bias very difficult (the stability of any leakage control scheme using forward-body bias can be a serious problem). In the reverse body bias (RBB) region, however, the leakage is dominated by junction BTBT and the dependence to temperature is almost linear. Therefore, we propose reverse body bias for leakage (temperature) control scheme, described in the next section.

7. Proposed Temperature Control System

The block diagram of the proposed junction temperature control system is shown in Figure 7.1. The temperature sensor measures the junction temperature (T_j) of the chip.

Once the system is calibrated, the measured junction temperature is compared with the desired burn-in junction temperature, T_{ref}. If T_{ref} is larger (less) than T_j, leakage current of the chip is increased (decreased) by increasing (decreasing) the RBB through the body bias generator. This system tries to stabilize the junction temperature of

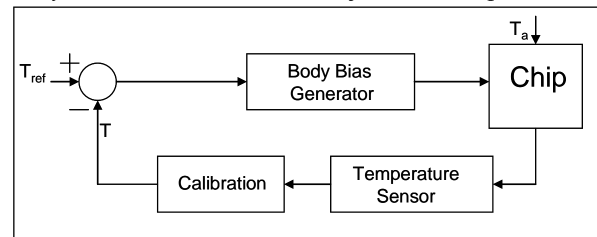

Fig.7.1 Block diagram of proposed leakage control system for thermal stability during burn-in test

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the chip by controlling the leakage current using RBB. The chip is under burn-in test in an environment with constant ambient temperature of T_a. Since the whole system including the temperature sensor is integrated into the chip itself, the measured temperature is the actual junction temperature. In the following sub-sections, each component of the system is explained in detail.

7.1 Integrated Temperature Sensor

The schematic of our temperature sensor is shown in Figure 7.1.1. All transistors are sized and biased such that they are in saturation region of operation. Transistors M_5 and M_6 provide bias for the current mirror PMOS transistors (M_3 & M_4). The currents of the current mirror PMOS transistors drive the NMOS diode-connected transistors (M1 & M2), generating voltages V_1 and V_2. The voltage difference between V_1 and V_2 is amplified using the differential amplifier.

In saturation mode, the drain current of an NMOS transistor is given as follows:

$$I_D = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{th})^{\alpha} \quad (7.1)$$

where, μ is the electron mobility and C_{ox} is the oxide capacitance of the transistor. In Eq.7.1, the parameters which are temperature dependent are μ and V_{th}. As temperature increases, both the mobility and the threshold voltage decrease. Reduction in mobility reduces drain current; however, Vth reduction tends to increase the current. In [20] it is shown that the effect of V_{th} on I_D is stronger than that of μ for scaled technologies. As a result, drain current of a transistor increases with increasing temperature.

Using Eq.7.1 for M_1 and M_2, V_1 ($=V_{gs1}$) and V_2 ($=V_{gs2}$) can be expressed as follows.

$$V_{gs1} = V_1 = \sqrt[\alpha]{\frac{I_1 L_1}{\mu_n C_{ox} W_1}} + V_{th1} \quad (7.2)$$

$$V_{gs2} = V_2 = \sqrt[\alpha]{\frac{I_2 L_2}{\mu_n C_{ox} W_2}} + V_{th2} \quad (7.3)$$

where W and L are transistor sizes. The output of temperature sensor (V_{out}) can therefore be expressed as follows: (assuming $R_1 = R_2$):

$$V_{out} = \frac{R_f}{R_1}(V_1 - V_2) \quad (7.4)$$

Assuming M_1 and M_2 have same μ, L, C_{ox} and threshold voltage, V_{out} can be expressed as follows:

$$V_{out} = \frac{R_f}{R_1}\sqrt[\alpha]{\frac{L}{\mu C_{ox}}}\left(\sqrt[\alpha]{\frac{I_1}{W_1}} - \sqrt[\alpha]{\frac{I_2}{W_2}}\right) \quad (7.5)$$

As observed from Eq.7.5, the threshold voltage dependence of V_{out} through I_1 and I_2 is decreased significantly as a result of subtraction. Hence temperature dependence of threshold voltage does not counter-effect

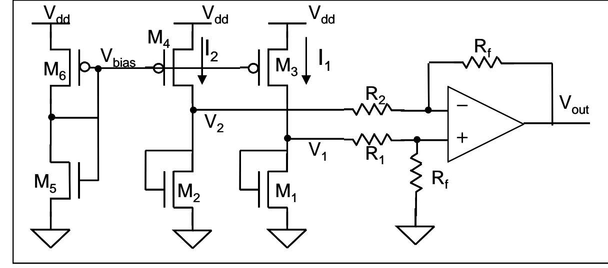

Fig.7.1.1 Integrated Temperature Sensor

the effect of mobility on V_{out}. This results in increase sensitivity of V_{out} on temperature.

The sensitivity of V_{out} on temperature can be further increased by adjusting the temperature dependence of I_1 and I_2 by proper sizing of transistors M_3 and M_4. I_1, drain current of M_3, can be expressed as follows:

$$I_1 = \mu_p C_{ox} \frac{W_3}{L_3}(V_{bias} - V_{dd} - V_{th3})^{\alpha} \quad (7.6)$$

Similarly, I_2 is given by:

$$I_2 = \mu_p C_{ox} \frac{W_4}{L_4}(V_{bias} - V_{dd} - V_{th4})^{\alpha} \quad (7.7)$$

As mentioned earlier and shown in Fig.7.1.2, I_1 (and I_2) increases with temperature due to stronger effect of V_{th} temperature dependence. Such positive temperature sensitivity of I_1 and I_2 enhances the sensitivity of V_{out} to temperature. By choosing W_2 to be larger than W_1 (Eq.7.5) the sensitivity of V_{out} to temperature can be further improved.

By proper sizing of transistors in the temperature sensor, and by choosing proper resistor values for proper gain, the temperature sensor is designed to have sufficient temperature sensitivity. Voltages V_1, V_2 and V_{out} are plotted in Fig.7.1.3 as a function of temperature.

The temperature dependence of V_1 and V_2 in Figure 7.1.3 can be explained as follows: Based on Eq.7.2 and Eq.7.3, since $W_2 > W_1$, temperature dependence of V_2 is more governed by temperature dependence threshold voltage compared to V_1. On the other hand, temperature

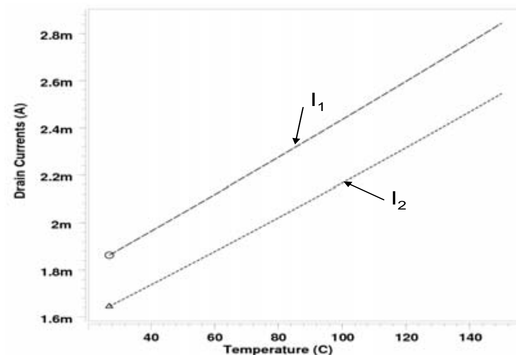

Fig.7.1.2 Drain currents vs. Temperature

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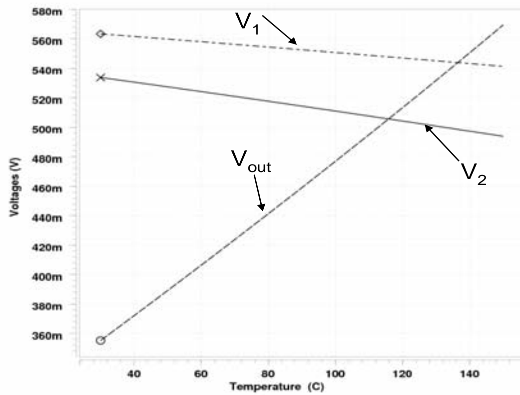

Fig.7.1.3 V_1, V_2 and V_{out} vs. Temperature

dependence of mobility is more effective on V_1. As a result, V_1 decreases slightly with temperature increase, while V_2 decreases more rapidly. Consequently, the difference (V_1-V_2) increases with temperature and this increase is amplified by the amplifier resulting in a reasonably strong temperature sensitivity for V_{out} as shown in Fig. 7.1.3.

The use of differential amplifier has two advantages: First, by canceling the V_{th} dependence of V_{out} and amplifying the mobility dependence, it increases the temperature sensitivity of V_{out}. Secondly, it cancels common mode noise on V_1 and V_2, improving the reliability of the sensor. It should be noted that the proposed temperature sensor circuit is all CMOS which makes it well integrated. Moreover, the usage of relatively large transistors reduces the effect of intra-die process variations on the temperature sensor. The effect of inter-die variations in NMOS transistors (M1 and M2) is automatically cancelled due to the differential nature of the amplifier. The effect of inter-die variation in PMOS can be minimized by enlarging M_6 so that V_{bias} tracks the variation of threshold voltage of PMOS more closely resulting in cancellation of the effect of PMOS threshold voltage variations on I_1 and I_2. The process variation effects on temperature sensor output are further eliminated by the calibration circuit as explained in section 7.2. Finally, temperature dependence of resistors is cancelled since the amplifier gain is proportional to the ratio of resistors.

7.2 Calibration Circuit

Calibration circuit diagram is shown in Figure 7.2.1. When the calibrate signal is activated, the output of A/D is stored in the register. The system can be calibrated at ambient temperature. Once the output voltage of temperature sensor is stored at ambient temperature, this voltage will be subtracted from temperature sensor output during normal operation of the system.

The necessity of the calibration circuit can be explained using Figure 7.2.2. In Fig.7.2.2, the output of temperature sensor is shown for three different threshold voltages as labeled. From the figure, it can be seen that temperature sensor output strongly depends on process variations in spite of enlarging the transistors in temperature sensor circuit. To eliminate process variation dependence, calibration circuit samples the temperature sensor output at ambient temperature (e.g. T_a=60°C) and stores it in the register. The value of stored voltage will be different for different threshold voltages. Finally, the stored voltage is subtracted from temperature sensor output. For the same example, the output of calibration circuit is shown in Figure 7.2.3. As seen in Figure 7.2.3, the process variation dependence of temperature sensor circuit decreases significantly using the calibration circuit. It should be noted that A/D and D/A converters might have their own calibration procedures that can eliminate process variations [19].

7.3 Temperature Independent Voltage Reference Generator and Comparator

The second component in our system is the temperature independent voltage reference generator and comparator. The voltage generated by the voltage reference generator represents the target temperature for burn-in. The main function of this part is to generate a temperature independent voltage to represent the burn-in junction temperature (T_j = 110ºC in our case) and to compare this reference voltage with the present output of the

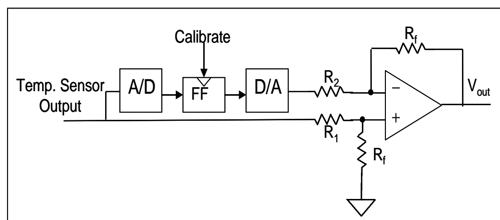

Fig.7.2.1 Calibration Circuit

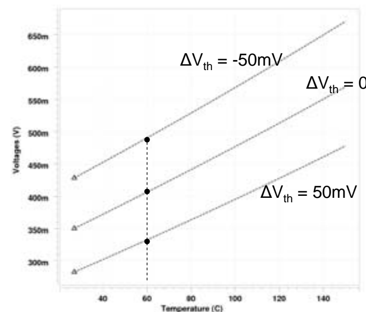

Fig.7.2.2 Temp. Sensor Output for different ΔV_{th} values

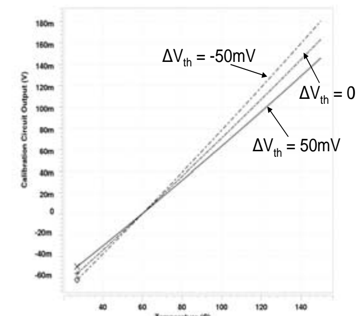

Fig.7.2.3 Calibration Circuit Output for different ΔV_{th} values

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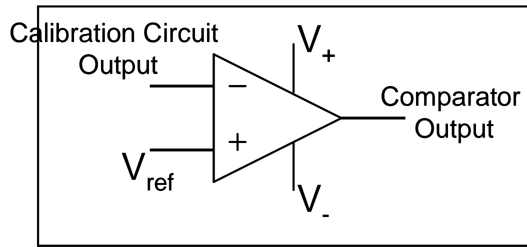

Fig.7.3.1 Comparator Schematic

calibration circuit.

Several techniques have been proposed in the literature for generating temperature independent voltages [14], [15]. It can also be supplied from outside of the chip. The value for the required reference voltage is determined from Fig.7.2.3 (voltage corresponding to 110ºC). A simple op-amp circuit can be used as the comparator (Figure 7.3.1).

The characteristics of our comparator circuit are shown in Figure 7.3.2. As seen in the figure, when the calibration circuit output voltage is lower than reference voltage, the comparator generates a "V_+" voltage and when calibration circuit voltage is larger than reference voltage, the comparator generates a "V_-" voltage. "V_+" and "V_-" are chosen to be 0.3V and -0.5V since these voltages are maximum and minimum body bias bounds, as will be explained in the next section.

7.4 Body Bias Generator (BBG)

The schematic of body bias generator (BBG) circuit is given in Figure.7.4.1. It is basically a charge-pump circuit converting the comparator output to a voltage that controls the body bias (V_x).

The function of this component is to generate the necessary body bias voltage depending on the comparator output. If the comparator output is V_+, which means the temperature of the chip is less than reference temperature, the voltage at V_x is pulled down through the NMOS path when the clock (Φ) is high. V_x is represented by the charge stored in the capacitor. As V_x decreases, the body bias of the chip also decreases (becomes more reverse body biased). This will increase the overall leakage by increasing junction BTBT leakage and therefore, the chip temperature increases. Once the temperature output exceeds the reference voltage, the comparator output switches to V_-. This will result in an increase in V_x (and body bias generator output) through the PMOS path each time the clock is low. As a result, BTBT and overall leakage and the junction temperature will decrease. Eventually after several cycles of clocking in the charge pump circuit, the body bias of the chip is adjusted automatically to keep the junction temperature around the burn-in temperature.

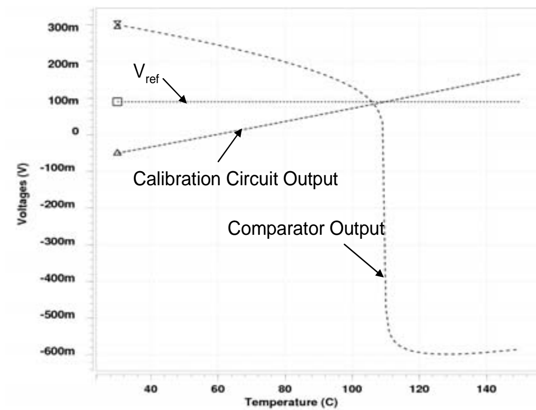

Fig.7.3.2 Comparator Output vs. Temperature

In the body bias generator circuit, the upper (V_+) and lower (V_-) voltage limits are chosen to avoid forward conduction of p-n junctions and reverse junction breakdowns.

The waveforms of the body bias generator circuit are shown in Figure 7.4.2 and 7.4.3. Figure 7.4.2 illustrates the decrease in voltage V_x when $T_j<T_{ref}$ and Figure 7.4.3 illustrates the increase in V_x when $T_j>T_{ref}$.

7.5 Leakage Control Using PMOS and NMOS Body Bias

So far, we have considered controlling the leakage by changing the body bias of only NMOS transistors. However, in a fully static CMOS design, half of the

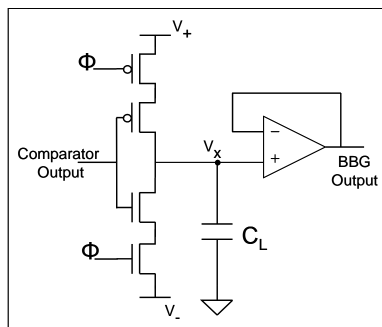

Fig.7.4.1 Body bias generator

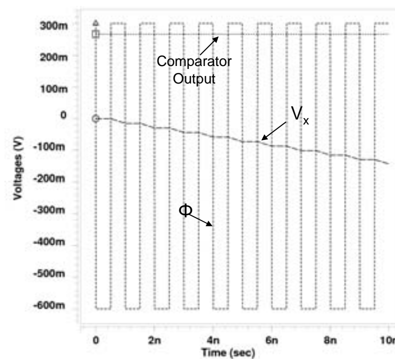

Fig.7.4.2 BBG Output when $T_j < T_{ref}$

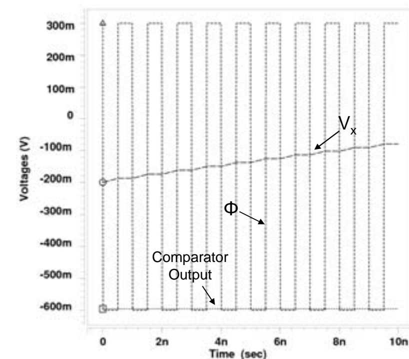

Fig.7.4.3 BBG Output when $T_j > T_{ref}$

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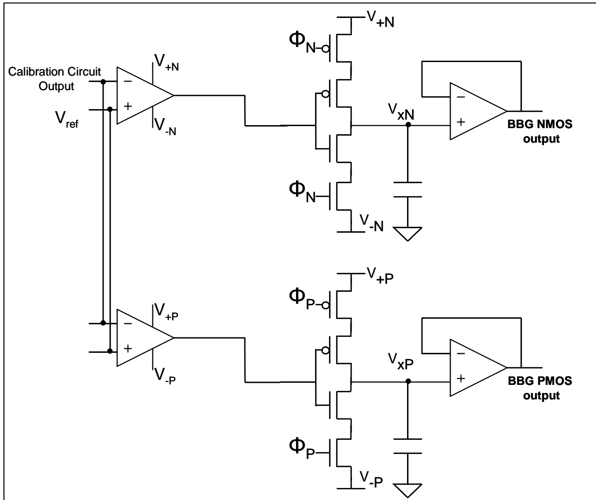

Fig.7.5.1 Circuit diagram for both NMOS and PMOS body control

transistors are PMOS. Thus, controlling body biases of both PMOS and NMOS transistors can provide more controllability to the system.

The circuit diagram for controlling both PMOS and NMOS body biases is shown in Fig.7.5.1. Since the range of body bias voltages is different for PMOS transistors, separate comparators and body bias generators with different V_+ and V_- values are needed.

8. Results

The proposed system was integrated in a predictive 50nm process [13]. The chip was represented as the total number of OFF transistors, predicted from ITRS [18] for such a technology node. System simulation was done in HSPICE. In the simulations, voltage stress of $1.3xV_{dd}$ (V_{dd} = 0.9V) and R_{ja} of 0.3 °C/W are used.

Fig. 8.1 shows the transient junction temperature response for different ambient temperature. Starting with an ambient temperature of 20ºC, the response of the system cannot reach the target burn-in temperature. That is because even with the application of maximum reverse body bias, the generated leakage is not sufficient to raise

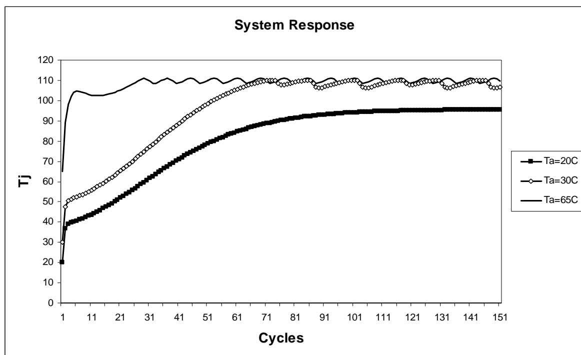

Fig. 8.1 Transient Temperature response

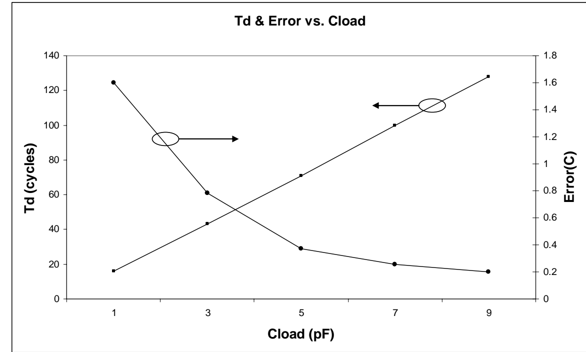

Fig. 8. 2 Steady state temperature error and stabilization time vs. capacitance of charge pump circuit

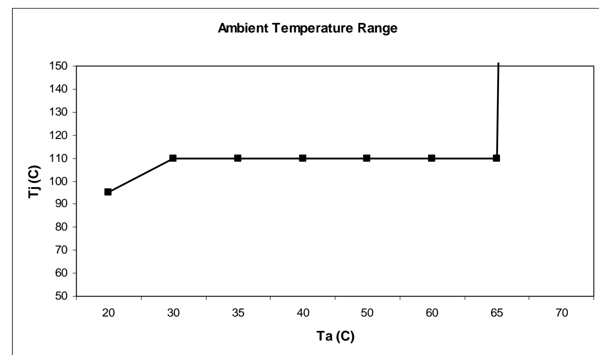

Fig. 8.3 Convergence range of ambient temperature

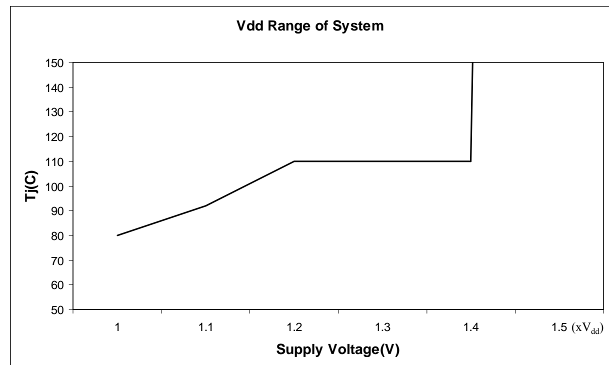

Fig. 8.4 Convergence range of supply voltage

the junction temperate to 110ºC. Starting with higher ambient temperatures however, the system can stabilize the junction temperature at 110ºC. It was observed that for any ambient temperatures greater than 65ºC thermal runaway could not be avoided.

The proposed system can converge to the target temperature with very small steady-state error as shown in Fig. 8.2. This error can be minimized by increasing C_L in the charge-pump circuit (Fig. 7.4.1). It would however increase the convergence time (T_d) of the circuit.

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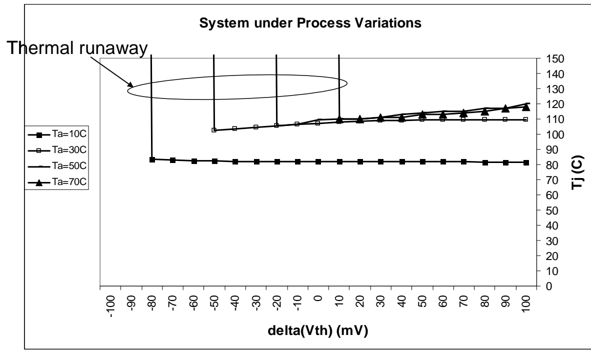

Fig. 8.5 Tolerance to process variations

The converging range of ambient temperature is wide enough as shown in Fig. 8.3. Fig. 8.3 shows the steady state temperature response of the system starting with different ambient temperatures.

The proposed system is not only tolerant to variations in ambient temperature, but also to variations in supply voltage of the chip. Fig. 8.4 shows that the system can converge to the target burn-in temperature for a wide range of supply voltages.

Fig. 8.5 shows the tolerance of the proposed system to process variations. As observed earlier (Fig. 5.1), in the conventional method of burn-in temperature control, starting with any ambient temperature, thermal runaway can occur for a wide range of process variations. The proposed system, on the other hand, provides a large range of tolerance to process variations with thermal stabilization at 110ºC. Higher ambient temperatures reduce the range of tolerance to process variations. If the ambient temperature is chosen to be too low (such as 10ºC in Fig 8.5), the junction temperature may not reach 110ºC. Therefore, under process variations selection of right ambient temperature provides maximum tolerance to process variations along with convergence to junction temperature of 110ºC.

9. Conclusions

Thermal stability during burn-in test is an increasingly important problem in scaled technologies. In this work, we have proposed a novel integrated leakage control scheme for thermal stability during burn-in test. The proposed system employs reverse body biasing in a negative feedback system to maintain the junction temperature at the target burn-in temperature. This system provides junction thermal stability for a wide range of variations in ambient temperature, supply voltage, and process parameter variations. The proposed system is therefore promising for enhancing quality of burn-in test in scaled technologies.

10. Acknowledgements

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