Process Variation Tolerant Online Current Monitor for Robust Systems

Qikai Chen, Saibal Mukhopadhyay, Hamid Mahmoodi, and Kaushik Roy
Purdue University, West Lafayette, IN 47907, USA
{qikaichen, sm, mahmoodi, kaushik} @ purdue.edu

ABSTRACT

Large inter-die and intra-die process variations result in significant uncertainty in delay of circuits. Large delay variations may lead to parametric/functional failures. In this paper we propose a novel leakage-variation-tolerant online current monitor, namely leakage canceling current sensor, to detect completion of operations in logic blocks. The current monitor is applied to self-timed logic to design process variation tolerant circuits. It is observed that, for self-timed circuits, the probability of functional failures can be reduced by 50% with no performance degradation and with same power consumption.

1. INTRODUCTION

With technology scaling inter-die and intra-die variations in process parameters (channel length, width, threshold voltage etc.) have become major obstacles in designing circuits in sub-90nm regime [1]. Variations in the process parameters can result in substantial variations in delay of a circuit. Fig. 1 shows the delay distribution of an ALU implemented in a predictive 70nm technology [2] with $\sigma_{Vt} = 40\text{mV}$. From Fig. 1, it is observed that a considerable variation in delay can result from process variations. Hence, the effective performance of a system can be lower due to variation. Moreover, delay variation in a die can also result in functional failures because some of the chips fail to meet the designed performance.

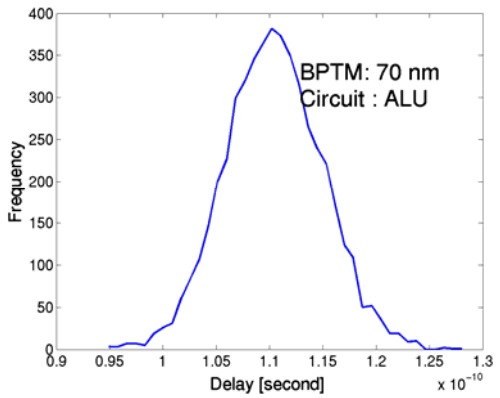

Fig.1: Delay variation of a circuit

The solution to the problem of parameter variation needs to be sought from both process and circuit level. Along with a more stable process (with less parameter variation), there is a need for designing circuits that are less susceptible to delay variations. The synchronous circuits are timed by the global clock and hence, the clock cannot track the local nature of the variation. This makes the synchronous circuits more prone to performance degradation and failure due to delay variation. On the other hand, self-timed circuits (not timed by the global clock) can successfully track the local variations in the circuit itself and hence, will be more robust against delay variations. A major design issue of self-timed systems is to detect the completion of the logic circuit. There exists previous work on completion detection using current sensors [3-5]. However, due to inter-die Vt variations, some dies may have higher leakage current than others. The higher leakage current in the standby mode may lead to a delay or even failure in the completion detection of a current monitor.

In this work, we have proposed a novel online current monitor, namely leakage canceling current sensor (LCCS), which tolerates inter-die leakage variations. Also we show the application of the online current monitor in a self-timed system and explore the possibilities of using self-timed system in improving the robustness of a design. It is observed that, the use of self-timed design can significantly improve the robustness of a system.

The remainder of the paper is organized as follows. In section II, a novel current sensor, namely LCCS, is proposed. Section III introduces the application of the current monitor to a self-timed system. Section VI shows the improvement in robustness of the self-timed design versus its synchronous counterpart.

2. CURRENT MONITOR CIRCUIT

Conventionally, current sensor is used to detect the completion of the asynchronous circuits [3-5]. Fig. 2 shows a conventional current sensor. In this design,

Proceedings of the 11th IEEE International On-Line Testing Symposium (IOLTS'05)
1530-1591/05 $20.00 © 2005 **IEEE**

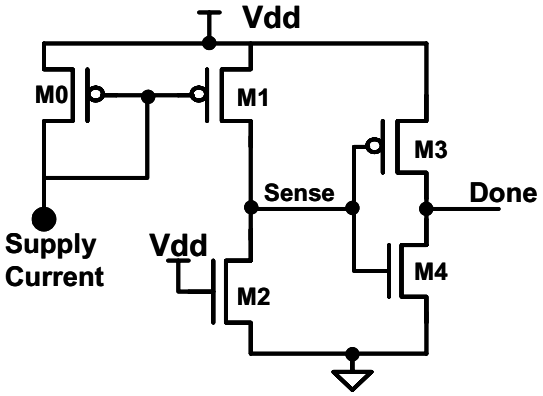

Fig. 2: Conventional current sensing circuit

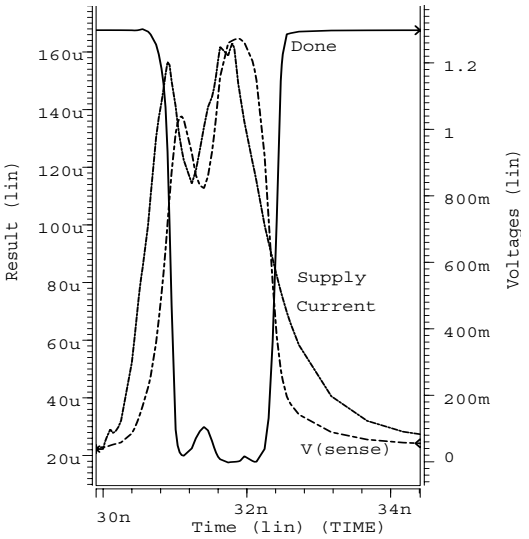

Fig. 4: LCCS waveforms

the supply current of a logic circuit block is mirrored through a current mirror (M0 and M1) to a bias-generation circuit. The bias-generation circuit contains an NMOS biased as a resistor (M2 in Fig. 2). If the supply current is high, the voltage drop across the active load (M2) is high, which is then inverted to generate a low value of the completion-detection signal. As soon as the circuit operation completes, only the leakage current flows through the circuit. This reduces the voltage drop across M2, thereby turning the completion-detection signal to high, which indicates the circuit has finished its operation and is in an idle state.

However, under process variations, there are two major problems with the traditional current sensors:

- The assumption that the sensing and the mirroring PMOS, M0 and M1, match each other perfectly may not be valid, especially under intra-die variations;
- Due to inter-die variations some of the dies may have large leakage current. For a fixed active load (M2), the high leakage current may delay the completion detection signal. Excessive leakage may even lead to functional failure of completion detection.

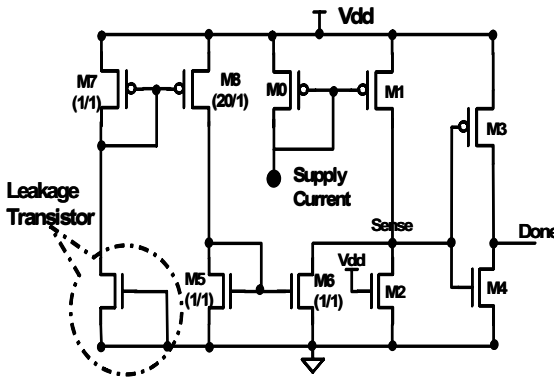

Fig. 3: Leakage Canceling Current Sensor (LCCS)

For sub-100nm technologies, on die transistor threshold (Vt) variations due to the random dopant fluctuations are critical. The standard deviation of the intra-die shift in Vt is modeled as [6]:

$$\sigma_{Vt} = \sigma_{Vt0}\sqrt{(L_{min}/L)(W_{min}/W)} \qquad (3)$$

where, σ_{Vt0} is the standard deviation of a minimal size transistor, which depends on the doping concentration and the oxide capacitance. To minimize the impact of intra-die variations on the mirroring circuit, M0 and M1 can be sized large enough to achieve less σ_{Vt}.

To improve the completion detection in high leakage dies, we propose a novel current monitor in Fig. 3. The proposed circuit, leakage canceling current sensor (LCCS), removes the leakage current from the sensed supply current. An NMOS transistor (*Leakage Transistor* in Fig. 3) is biased in sub-threshold region to generate the reference leakage current for the particular location of that die. This leakage current is then amplified through the current mirror M7 and M8. So as to allow fast response of the voltage at node SENSE to the supply current, the reference leakage current is mirrored again through M5 and M6. M6 can be chosen to be of considerably small size to minimize the RC constant at the node SENSE in Fig. 3. Finally, the reference leakage current is subtracted from the sensed supply current flowing into the active load (M2). Fig. 4 shows the waveform of the operation of the proposed current sensor. Whenever the sensing supply current goes low, the voltage at the node sense drops down. This raises the inverter output to Vdd.

Based on the size of the logic blocks, to which LCCS is applied, the leakage transistor size as well as the

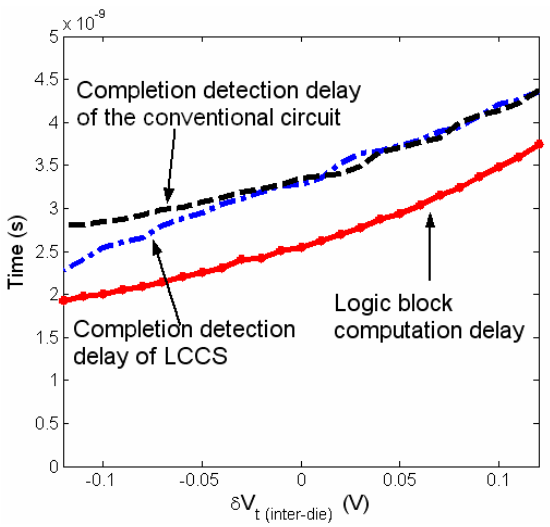

Fig. 5: Delay VS. Inter-Die Variations

M8/M7 ratio can be adjusted to compensate for the inter-die leakage current variation. Also the ratio between M0 and M1 should be carefully adjusted so that the power overhead of the current sensor is minimized.

Simulation is performed to verify the performance of LCCS considering variations in the process parameters. In the simulation, a 4-bit ripple carry adder is chosen as the computation logic block. An intra-die Gaussian distribution of Vt (σ=40 mV) is applied. The delay of the adder circuit and the timing of the generation of the completion-detection (DONE) signal are obtained from the simulation with the inter-die Vt shift ranging from -120mV to 120mV. It is observed that the proposed current sensor successfully tracks the adder delay (Fig. 5) for a wide range of inter-die Vt shift. Particularly, the detection speed with the proposed design significantly improves for low Vt (i.e. high leakage) dies.

3. ROBUST SELF-TIMED CIRCUIT

The abovementioned online current monitor (LCCS) is applied to a self-timed system. The self-timed system is designed by replacing the clock signal in the synchronous design by the DONE signal generated by LCCS. Fig. 6 shows the architecture of the self-timed circuit. To cooperate with the completion detection circuit (current monitor), a Feeder Control Logic is designed. The Feeder Control Logic (Fig. 6) accepts data synchronously while supplies data to the logic blocks asynchronously.

3.1 Design of Feeder Control Logic

An architecture level design of the feeder control logic is shown in Fig. 6. Central to the operation of the logic is the FIFO like storage elements: DATA and VALID. The storage element DATA consists of a set of flip-

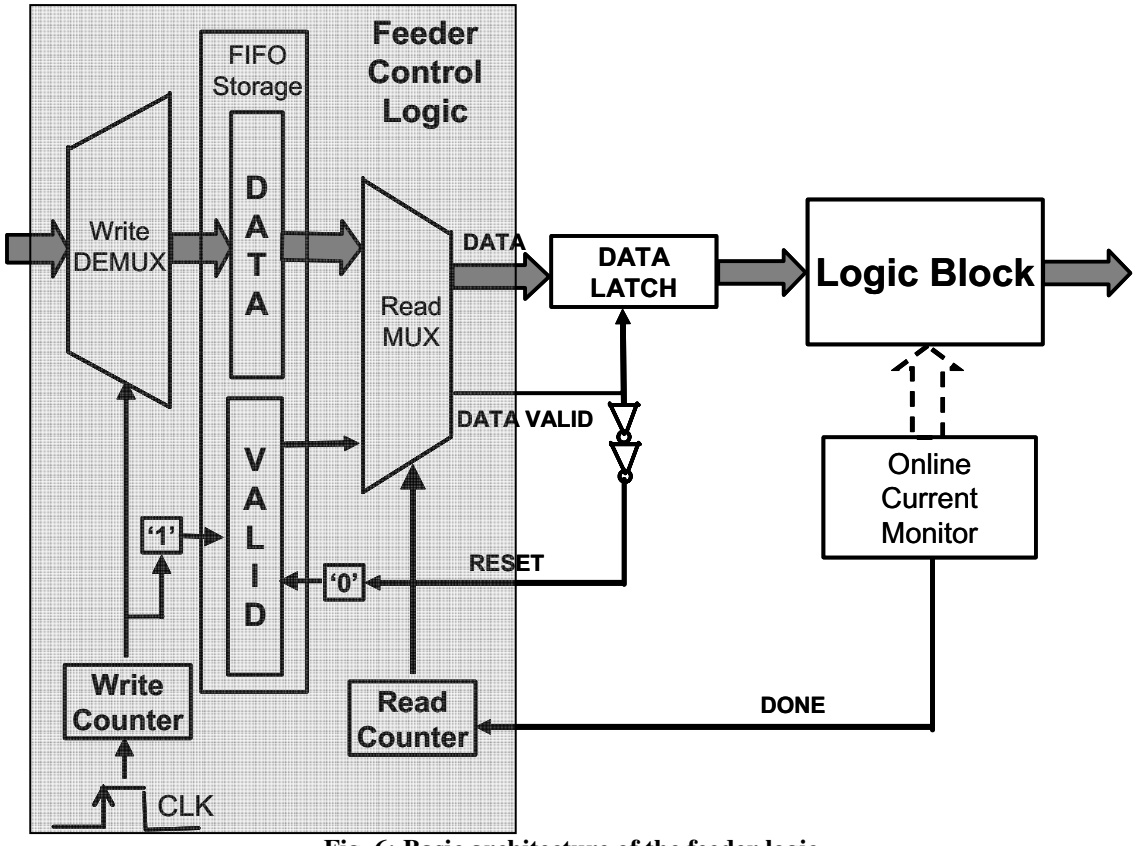

Fig. 6: Basic architecture of the feeder logic

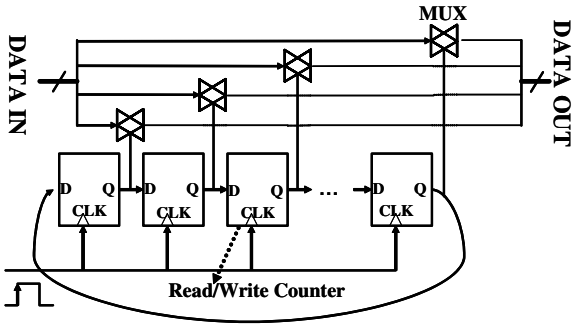

Fig. 7: Read MUX and Write DEMUX

flops to store the input data. Input data are written to a storage location in DATA (Fig. 6) at each positive clock edge using a DEMUX (Write DEMUX in Fig. 6). The DEMUX is controlled by the state of the WRITE COUNTER. The element VALID contains a set of storage elements. Each storage element in VALID determines the state of the stored data in the corresponding location of DATA. Whenever, a new input data is written to a particular location of DATA, the corresponding location in VALID is set to "1". If a location in VALID is "1", it implies that the corresponding location in DATA contains data which has not been processed. On the other hand, whenever a block finishes data processing, the online current monitor detects the completion and raises the DONE signal high. The DONE signal advances the state of the READ COUNTER. Then, the next corresponding bits in DATA and the DATA VALID are read through the READ MUX. A high level DATA VALID signal makes the DATA LATCH transparent. And therefore, the input data is applied to the logic block. The DATA VALID signal is also delayed to generate the RESET signal. After the input is applied to the logic block, the current location in DATA VALID is set to "0" by using the rising edge of RESET signal.

3.2 Circuit Implementations of Feeder Control Logic

We have applied several custom circuit techniques to improve the performance of the feeder control logic circuit. The READ MUX and WRITE DEMUX are implemented using pass-gates (Fig. 7). In Fig. 7, a loop shift register is used as the counter (for both Read Counter and Write Counter). This avoids decoding of the counter outputs for generating control signals for the pass-transistors of the MUX. The shift register has only one of its flip-flops set to one (read or write enabled) and the rest are set to zero. As the counter (loop shift register) is clocked, the 'one' propagates through the shift register loop and therefore individual pass gate (MUX) is activated one after another.

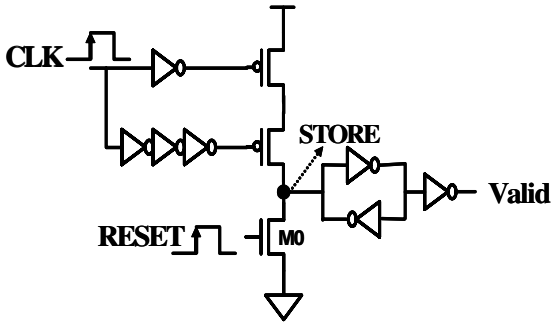

Fig. 8: VALID signal generation circuit

The storage elements in DATA of Fig. 6 can be implemented using single edge triggered flip-flops. However, the storage element in VALID of Fig. 6 is more complicated as it is controlled by two signals. A storage element in VALID is set to "1" at the positive clock edge and reset to "0" at the positive edge of the RESET signal. A circuit implementation of the required storage element is shown in Fig. 8. At the positive edge of CLOCK the node STORE is pre-charged to "1". If a positive edge occurs at the input of M0 (the RESET signal) the node is discharged to "0" and remains "0" till the next positive CLOCK edge.

4. EXPERIMENTS AND RESULTS

The online current monitor discussed in section 2 is applied to an 8 bit adder to form a self-timed circuit with the architecture discussed in Fig. 6 of section 3. The self-timed system was simulated to estimate the improvement in robustness. The failure probabilities of the self-timed system and its synchronous counterpart are obtained from simulation. In this analysis, the data is sent to the logic block at the target frequency. Due to the variation in the delay, a logic block may become slower than the target delay. In that case, for a synchronous design, if data is still sent to the block at the target frequency, new data will be sent to the computational block input before the previous computation is completed. Such a situation will result in a failure and the output of the system will be incorrect. Therefore, in the synchronous design, a failure occurs whenever the delay of a block is higher than the target delay (the clock frequency). However, such a failure does not occur in the self-timed system using the proposed current sensor as a completion detector. In the self-timed system, failure will occur only when the blocks become so slow that there is an overflow in the FIFO storage element. Using a FIFO size of 8 a significant improvement in the failure probability of the self-timed system is observed. Table-I shows the results with different inter-die and intra-die variations. The self-timed system has a failure probability that is roughly half of the failure probability of the synchronous system.

Table-I
Failure probability of the self-timed and synchronous design under different parameter variation

	Sigma of Delay Variation – Inter Die							
	10%				20%			
	Intra-Die				Intra Die			
	2%	10%	20%	30%	2%	10%	20%	30%
Synchronous Design	26%	42%	56%	59%	39%	46%	51%	58%
Self-timed Design	4%	20%	28%	36%	14%	22%	28%	34%

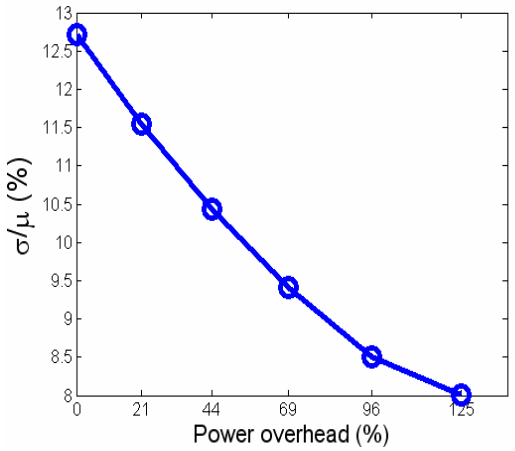

Fig 9: Percentage of delay variation versus power overhead

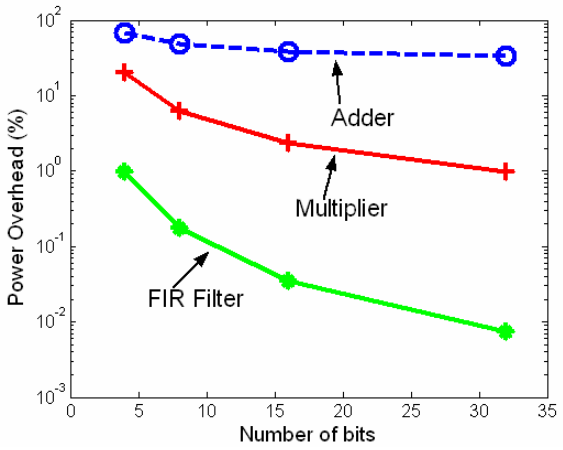

Fig. 10: Power overhead corresponding to different computational logic block

The analysis above has neglected the power overhead of the self-timed system due to the current monitor and the feeder control logic. With the same power overhead, the synchronous counterpart can be run at a higher supply voltage. The delay variation will reduce by increasing the supply voltage. A chain of inverters are implemented by BPTM70 technology [2] and simulated in SPICE. Under different supply voltages, Monte Carlo simulation (5000 trials) is performed with σ_{Vt}(Inter)=40mV and σ_{Vt}(Intra)=40mV . Fig. 9 shows the percentage delay variation versus the percentage power overhead. The results show that even with twice the power consumption, the delay variation reduced from 12.5% to 8.5%. The power overhead of the self-timed system is also estimated. In our experiments we also chose 4, 8, 16 and 32-bit adders, multipliers and FIR filters as the logic blocks. The results are shown in Fig. 10. From Fig. 10 we conclude that as the computation block gets larger and larger, the power overhead decreases. This trend results from the fact that most of the power consumption in the control logic does not scale with computation logic block size. If the computation logic block is as complex as multipliers or FIR filters, the power overhead is negligible.

From the above analysis it is clear that under process variation, self-timed systems show more robustness than synchronous systems under iso-performance and iso-power consumption.

5. CONCLUSION

In this work we have proposed a novel current monitor, which tolerates leakage current variation. We applied

the current monitor as completion detector in self-timed systems. Considerable improvements in robustness of the system were observed under severe parameter variations. We conclude that, under process variation, self-timed systems are more robust than synchronous systems having iso-performance and iso-power consumption.

6. ACKNOWLEDGEMENT

This work is sponsored in part by MARCO GSRC and National Science Foundation (NSF).

7. REFERENCE

[1]. V. De et. al., "Technology and design challenges for low power & high performance", ISLPED, 1999, pp.163-168.

[2] Predictive Technology Model, available at: http://www.device.eecs.berkeley.edu/~ptm/mosfet.htm

[3] H. Lampinen, et. al, "Current sensing Completion Detection method for Standard Cell Based Digital System Design", ISCAS, 2002.

[4] M. Hevery, et. al. "Asynchronous Circuit Completion Detection by Current Sensing", ASIC, 1999.

[5] E. Grass, et. al. ,"Asynchronous Circuits Based on Multiple Localized Current-sensing Completion Detection", Second Working Conference on Asynchronous Design Methodologies 1995.

[6] Y. Taur, et. al. "Fundamental of Modern VLSI Devices", Cambridge University Press, 1998.