A High Speed and Leakage-Tolerant Domino Logic for High Fan-in Gates

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Abstract
Robustness of high fan-in domino circuits is degraded by technology scaling due to exponential increase in leakage. In this paper, we propose a new domino circuit for high fan-in and high-speed applications in ultra deep submicron technologies. The proposed circuit employs a footer transistor that is initially OFF in the evaluation phase to reduce leakage and then turned ON to complete the evaluation. According to simulations in a predictive 70nm process, the proposed circuit increases noise immunity by more than 26X for wide OR gates and shows performance improvement of up to 20% compared to conventional domino logic circuits. The proposed circuit reduces the contention between keeper transistor and NMOS evaluation transistors at the beginning of evaluation phase. This results in less power dissipation for the proposed technique.

Categories and Subject Descriptors
B.6.1 [**Logic Design**]: Design Styles – *leakage tolerance, high fan-in domino logic.*

General Terms
Performance, Design, Reliability.

Keywords
Fan-in, domino, deep submicron, high speed, noise immunity.

1. Introduction
High fan-in compact dynamic gates are often used in high performance critical units of microprocessors. However, the use of wide dynamic gates is strongly affected by subthreshold leakage and noise sources [1]. This is mainly due to decreased threshold voltage that results in exponentially increased leakage currents in scaled technologies. To reduce power consumption, supply voltage scaling is used across technology scaling. However, threshold voltage needs to be scaled down as well to maintain transistor overdrive for large ON currents. Less threshold voltage means smaller gate switching trip point in domino circuits. Smaller trip points make the domino circuit more prone to input noise. Moreover, excessive leakage can discharge the precharge (dynamic) node of a domino circuit resulting in a logic failure (wrong evaluation). In addition to reduced trip point and increased leakage, other noise sources such as supply noise and cross talk noise also increase by technology scaling, further degrading the robustness of domino logic [13].

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A conventional approach for improving the robustness of domino circuits is keeper transistor upsizing. However, as the keeper transistor is upsized, the contention between keeper transistor and NMOS evaluation network increases in the evaluation phase. Such current contention increases evaluation delay of the circuit and increases power dissipation. Thus, keeper upsizing trades off delay and power to improve noise and leakage immunity. Such trade-off is not acceptable because it may make the circuit too slow or too power hungry. There are techniques proposed in the literature to address this issue. High-speed domino logic [11] and conditional keeper [7] are among the most effective solutions for improving the robustness of domino logic.

In this paper, we propose a new domino circuit for high fan-in and high-speed applications in ultra deep submicron technologies. The proposed circuit employs a footer transistor that is initially OFF in the evaluation phase to reduce leakage and then turned ON to complete the evaluation. In order to avoid the delay penalty due to an initially OFF footer transistor, an extra path for evaluation is provided that is controlled by the output. According to simulations in a predictive 70nm process, the proposed circuit increases noise immunity by more than 26X for wide OR gates and shows performance improvement of up to 20% compared to conventional domino logic circuits. The proposed circuit reduces the contention between keeper transistor and NMOS evaluation transistors at the beginning of evaluation phase. This results in less power dissipation for the proposed technique.

The rest of paper is as follows. In section II, existing leakage tolerant domino circuits are reviewed. Section III describes our proposed circuit. The simulation results are presented in section IV. Finally, section V concludes the paper.

2. Existing Leakage Tolerant Domino
Floated dynamic node at the beginning of evaluation phase for domino logic circuits has made these circuits more and more sensitive to noise sources [1]. The dynamic node is very sensitive to noise sources such as crosstalk, leakage current, charge sharing, power supply bump, and ground bounce. Since it is a dynamic node, it cannot be recovered after losing its data by the noise sources. The dynamic node in the evaluation phase is the most important node in domino circuits to be stable to have a right behavior.

Conventional domino logic styles include footless standard domino logic (FLDL) [10], footed standard domino logic (FDL) [10], and high speed domino logic (HSDL) [11], and conditional keeper domino logic (CKL) [7]. The domino logic is primarily proposed for high-speed applications, however, the sensitivity of the dynamic node to noise sources has emerged as a serious design challenge in scaled technologies. This vulnerability to noise increases, especially in ultra deep submicron technologies. Conventionally, the keeper transistor is added to circuit for keeping the state of the dynamic node resistant to noise and leakage. However, adding this PMOS keeper transistor degrades

performance and increases power dissipation in the circuit. Upsizing the keeper transistor is one of the ways to improve robustness, but this causes more increase in power dissipation and delay. In other words, upsizing the keeper increases current contention between the keeper transistor and the evaluation network. Therefore, for high-speed applications using small size keeper is desirable [8].

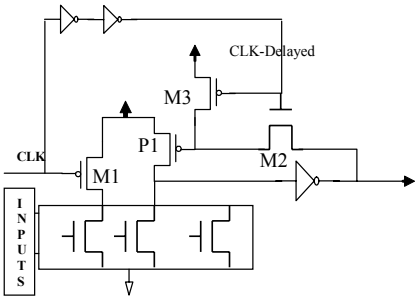

Figure 1. HS domino logic circuit

The footed domino logic (FDL) is more noise immune. FDL works similar to FLDL; however, in FDL, the noise immunity is higher because of using stack effect due to the added footer transistor at the bottom of the evaluation network. In fact, FDL is preferred for noise immune applications, but its speed is lower than FLDL.

A. High Speed Domino Logic (HS Domino):

One of the existing leakage tolerant domino circuits is high-speed domino logic (HS) [11]. Circuit diagram of HS-domino is shown in Fig. 1. At the beginning of the evaluation phase, CLK_Delayed is low and CLK is high. PMOS transistor M3 is ON and therefore it turns off the keeper transistor. After a delay equal to the delay of the inverters, when CLK_Delayed is high, if the output node is high, M2 remains in the off state and P1 remains off too. However, in the other case, when output remains low after that delay (delay of inverters) in the evaluation phase, node A is connected to node OUT. This causes PMOS transistor P1 (keeper transistor) to be turned on to keep the dynamic node strongly connected to VDD for the rest of the evaluation phase. The turned off keeper transistor at the beginning of the evaluation phase helps to remove the contention between the keeper and NMOS evaluation network, thus achieving less power consumption and higher performance. However, the dynamic node is floating at the beginning of the evaluation phase since the keeper is turned off. Therefore, if there is noise at the inputs at the onset of evaluation, the dynamic node can be discharged resulting in wrong evaluation.

B. Conditional Keeper Domino Logic (CKL)

Another existing leakage tolerant domino circuit is conditional keeper domino logic (CKL) [7]. Circuit schematic of the conditional keeper is shown in Fig.2. The circuit works as follows: at the beginning of the evaluation phase, the smaller keeper (P1) is ON for keeping the state of the dynamic node. After delay of inverters, if the dynamic node is still high, the output of the NAND gate goes low to turn on P2. This keeper transistor is sized larger than P1 for keeping the state of the dynamic node for the rest of the evaluation period. However, the conditional keeper remains off, if the dynamic node is discharged to ground. CKL logic has some problems like limitations on decreasing delays of the inverters and the NAND gate for improving noise immunity. Noise immunity can be improved by upsizing delay inverters, but this increases power dissipation significantly [12-14].

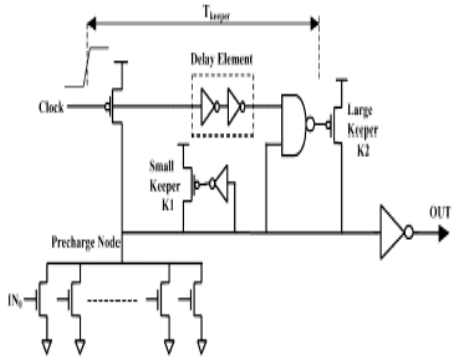

Figure 2. CKL domino circuit

3. Proposed Domino Logic

The schematic of our proposed circuit is shown in Fig. 3. The proposed circuit employs stacking effect (by adding the footer transistor MN1) for noise immunity improvement and uses the steady state voltage of N_FOOT node at the beginning of evaluation phase to reduce leakage of the evaluation network. Let us analyze the operation of the circuit in different modes.

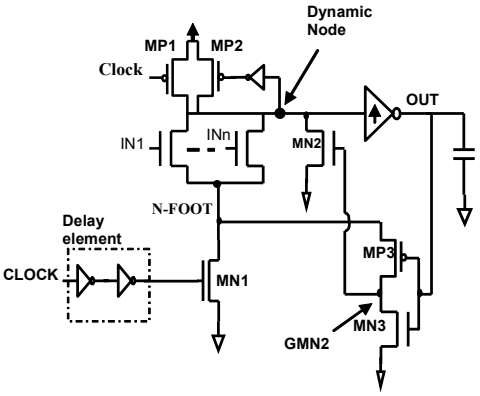

Figure 3. Proposed circuit

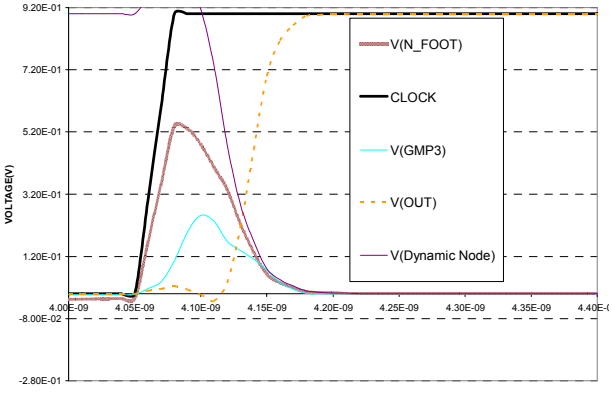

Figure 4 .Waveforms of proposed circuit

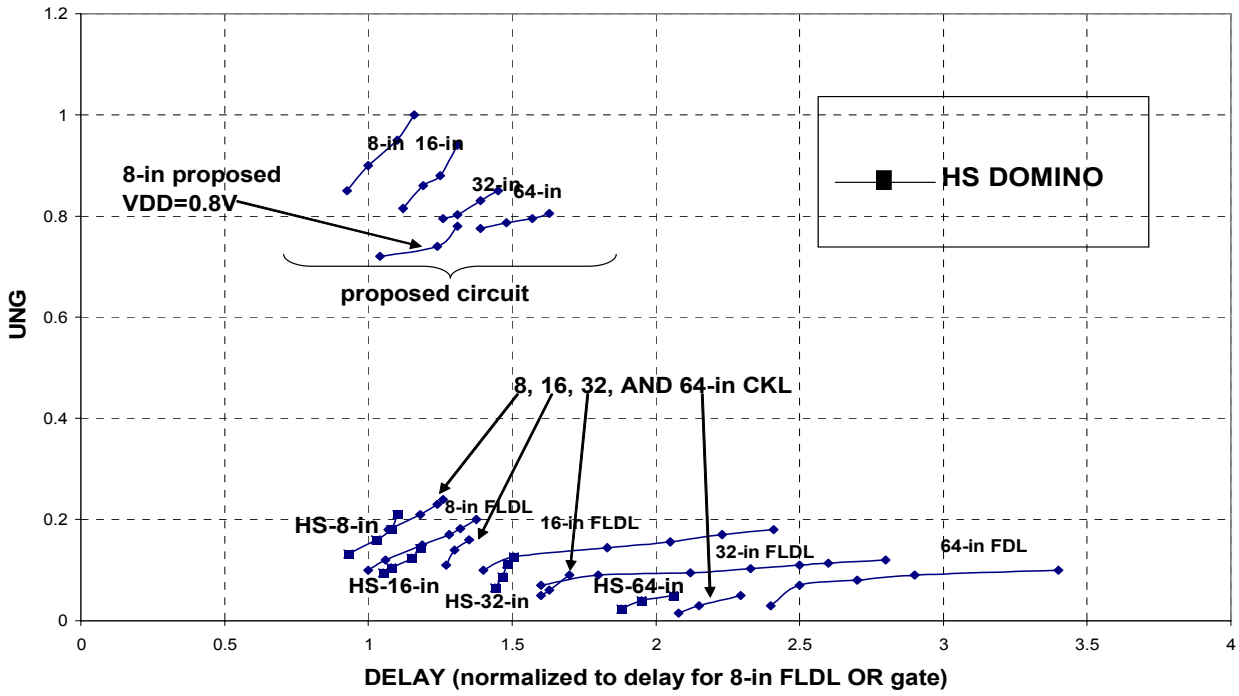

Figure 5 .UNG-delay comparison between our proposed circuit and conventional domino logics (FLDL: footless domino logic, FDL: footed domino logic, HS: high-speed domino logic, CKL: conditional keeper logic)

Table 1: UNG comparison between conventional circuits and our proposed circuit (at same delay)

Fan-in	UNG of standard domino (footless)	UNG of footed SDL	UNG of conditional keeper logic	UNG of proposed circuit	improvement compared to FLSDL	improvement compared to FSDL	improvement compared to CKL
8	0.18	0.21	0.24	0.86	4.78X	4.095X	3.583X
16	0.12	0.15	0.16	0.834	6.95X	5.56X	5.212X
32	0.07	0.13	0.1	0.802	11.457X	3.77X	8.02X
64	0.03	0.1	0.07	0.789	26.3X	7.89X	11.27X

Table 2: Power, delay, and area comparisons for 16-in OR gates (at same UNG condition)

	Power	Delay	Area
CKL	1	1	1
HS	0.72	0.87	0.93
Proposed	0.69	0.887	0.89

a) Precharge mode:

When clock is low, the circuit is in the precharge phase. MP1 is turned on and the dynamic node starts charging to VDD. In addition, PMOS keeper transistor (MP2) is turned on helping the precharge. At the beginning of the precharge phase, MN1 is on. Thus, it pulls the N_FOOT node to ground. Meanwhile,

node GMN2 is low and MN2 is in the off state. After the delay of the inverters (delay element), MN1 is turned off. In this case, the voltage of N_FOOT rises to an intermediate voltage level.

The evaluation transistors are sized such that the DC voltage of GMN2 node does not exceed the threshold voltage of MN2 to avoid any possibility of short circuit current in the precharge phase. We have selected MN2 to be larger than other NMOS transistors.

b) All inputs at zero in evaluation

At the beginning of the evaluation phase, NMOS footer transistor MN1 is off. Thus, N-FOOT node is floating. Therefore, in this case, its voltage reaches a DC voltage. If this voltage exceeds $|V_{tn\text{-}MP3}|+V_{OUT}$, MP3 is turned on. In the other words:

$$if \quad V_{N-FOOT} \geq V_{tp-MP3} + V_{OUT} \qquad MP3 : ON \qquad (1)$$

In that case, the GMN2 node is charged to $V_{N\text{-}FOOT,}$ and therefore:

$$if \qquad V_{GMN2} \geq V_{tn-MN2} \quad MN2 : ON \qquad (2)$$

If condition (2) is satisfied, (MN2 is turned on), a wrong evolution occurs. However, in our design we have sized MN1, MN2, MP3, and MP4 considering the voltage of GMN2. The sidings are done in such a way that condition (1) and (2) do not happen. Therefore, the DC voltage of N_FOOT acts as a source biasing for the evaluation network without affecting the functionality of the circuit. This DC voltage reduces leakage of the evaluation network substantially, resulting in significant leakage tolerance. Our proposed circuit has significant immunity to input noise because due to the DC voltage of sources of NMOS transistors of evaluation network, their threshold voltage increases. Thus, their trip point increases and their subthreshold leakage current reduces significantly, due to stacking effect. In our proposed circuit, performance improvement is achieved by upsizing MN2 transistor. This is further described in the following subsection.

c) An input switching high in evaluation phase:

The waveforms of the circuit in this mode are shown in Fig.4. As observed, the increased voltage of N_FOOT node at the beginning of the evaluation phase causes MP3 to be turned on. Therefore, the GMN2 node is charged to the voltage of N_FOOT node which rises above the threshold voltage of MN2. Therefore, the NMOS transistor MN2 is turned on at the onset of evaluation phase (when the footer transistor MN1 is off), connecting the dynamic node to ground. After delay of the delay element, N_FOOT node is strongly at zero voltage. Thus, the transistor MP3 switches to the off state. Since the output nod is at high now, it turns on the MN3, and connects GMN2 node to ground turning MN2 off. However, the rest of evaluation phase (discharging of the dynamic node) completes through the evaluation network and the footer transistor that is fully on. Here we have more degree of freedom for increasing speed or enhancing noise immunity. For example, for improving speed, upsizing of MP3, MN2, MN1, evaluation transistors, and MN1 are all options.

4. Simulation results

In this section, we study the behavior of our proposed circuit based on simulation results. The results are obtained using predictive technology model of 70nm technology at the temperature of 110C. The noise immunity metric used in our work is unity noise gain (UNG) [8]. UNG is the amount of DC noise at all inputs that result in the same amount of noise at the output nose. Therefore, larger UNG indicate more noise (leakage) immunity. Fig. 5 shows UNG-delay comparisons. UNG of our proposed circuit is shown by varying keeper transistor size from $0.3W_{EVAL}$ to $1W_{EVAL}$ (WEVAL being the width of evaluation transistors). The proposed circuit shows very high UNG compared to other proposed circuits and higher speed than some existing designs. Therefore, the proposed circuit has higher performance and very high UNG over conventional domino circuits. Table 1 shows that the improvement of UNG for our proposed circuit compared to conventional circuits is as large as 26X. In addition, speed of our proposed circuit is acceptable and it shows 20% improvement for some cases. In the evaluation mode with all inputs zero, we observed that the subthreshold leakage current has reduced significantly in our circuit. In our proposed circuit, by sizing transistors precisely, we can get less power dissipation compared to conventional circuits. Table 2 shows the power dissipation of our proposed circuit compared to other domino logic circuits.

The proposed circuit has employed small devices for the evaluation network, and therefore, the area of our proposed circuit is less comparing with conventional circuits. The comparisons of area, power, and delay are shown in Table 2.

In summary, according to the simulation results, the propose circuit shows 3.58X to 26X UNG improvement, 10% to 30% performance enhancement, and 10% to 22% power reduction compared to existing leakage tolerant domino techniques.

5. Conclusions

We have proposed a new leakage-tolerant and high-speed domino logic circuit with reduced power dissipation. In this circuit, we obtained excellent noise immunity and higher speed compared to existing domino circuits. The proposed techniques use a small keeper transistor to reduce power dissipation. It improves leakage tolerance by using a footer transistor.

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