Pre-Capturing Static Pulsed Flip-Flops

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***Abstract*—This paper presents Pre-Capturing Static Pulsed Flip-Flops (PCSPFF), which are composed of a pulse generator and a static flip-flop with equal toggling delays. Pre-capturing technique makes PCSPFF faster than other high-performance flip-flops. Power consumption of the PCSPFF is observed to be the lowest among high-performance flip-flops. HSPICE simulation results at a frequency of 400MHz show that the proposed PCSPFF exhibits 39.7% and 29% reduction in power-delay-product compared to the hybrid-latch flip-flop and conditional-capture flip-flop, respectively. Moreover, the proposed PCSPFF shows more than 50% and 32% power reduction in practical circuits compared to the hybrid-latch flip-flop and conditional-capture flip-flop, respectively. Double-edge triggering feature can be added to the proposed flip-flops to reduce the clock frequency by 50%. Using double-edge triggering in the proposed flip-flops, an energy saving of 94% is achieved on the clock distribution network. Incorporating double-edge triggering technique along with sharing pulse generation among flip-flops presents up to 68% power reduction in an 8-bit counter.**

I. INTRODUCTION

Flip-flops are essential elements of a design from both delay and energy aspects. Since the importance of designing low-power and high performance timing elements has been recognized, many latches and flip-flops have been designed. Hybrid-Latch Flip-Flop (HLFF) [1] is a fast flip-flop and shows negative setup time, which provides soft clock edge property. However, HLFF consumes large amount of power due to redundant transition of internal nodes. Conditional-Capture Flip-Flop (CCFF) [4] is another high-performance flip-flop which can eliminate redundant internal transitions to minimize power dissipation; however, it needs too many transistors which tend to offset the power saving. Moreover, CCFF shows significant power consumption in clock distribution network.

Transparent latches are usually simple and fast but they suffer from race problems. This paper presents simple-structure static pulsed flip-flops which have a small transparency window. Input data is pre-captured before the real transparency window, and the complete capturing occurs during the short window. Hence, the delay decreases considerably. These structures present small data to output latency along with soft clock edge property and low power consumption; therefore they are complete options for high performance and low power applications. The pulse generator of PCSPFF can be shared among a group of flip-flops to reduce the power and area overhead of pulse generation.

The major portion of the total power in highly synchronous systems, such as microprocessors, is dissipated over the clock tree [5]. Proposed flip-flops present low power dissipation in clock distribution network. Double-edge triggering is a technique that has been incorporated into flip-flops for significant clock power reduction [6,7]. Double-edge triggering feature can also be applied to the proposed flip-flops to reduce the clock frequency by 50%, and thereby more energy saving can be obtained on the clock distribution network.

The remainder of this paper is organized as follows. In sections II, the high-performance flip-flops are reviewed. Sections III explains the proposed pre-capturing static pulsed flip-flops. The double-edge triggering feature incorporated into the proposed flip-flops will be explained in section IV. In section V, extensive simulation results of individual flip-flops and their comparisons are presented. Finally, the conclusion of the paper appears in Section VI.

II. HIGH PERFORMANE FLIP-FLOPS

High performance flip-flops used for comparison with the proposed flip-flops are Hybrid Latch-Flip-Flop (HLFF) [1], modified Sense Amplifier-based Flip-Flop (SAFF) [2], differential Conditional-Capture Flip-Flop (CCFF) [4], and Dual-rail Static Edge-Triggered Latch (DSETL) [3]. The major advantage of HLFF is the small data to output latency and the soft-clock edge property which is desirable for robustness to clock skew. HLFF consumes large amount of power due to redundant transition of internal nodes at low data switching activities. SAFF incorporates a pre-charged sense amplifier and a symmetric latch topology that reduces delay and improves driving capability. It has redundant transition of internal nodes at low data switching activities due to the pre-charged sense amplifier structure. CCFF achieves statistical power reduction by eliminating internal redundant transitions. It has negative setup time and thus provides small data-to-output latency [4]. CCFF needs too many transistors for conditional capturing and shows large clock load. DSETL is a simple latch structure which shows low power consumption at low data switching activities due to its static nature, but it consumes large power at high data switching activities. DSETL has relatively large delay time and large data load due to pass transistors on its data inputs.

III. PROPOSED STATIC PULSED FLIP-FLOPS

A static flip-flop such as DSETL has the advantage of low power due to elimination of redundant internal transitions by static operation. However, static flip-flops show long delays. We propose pre-capturing as a technique to be used in static pulsed flip-flops to improve their speed while having their advantage of low power. The pulse generator circuit generates two pulse outputs with a small delay between them as shown in Fig. 2. The second pulse (PULS) which provides the real transparency window can be the inverse of the first pulse (PULSNOT) which is used for pre-capturing. Input capturing begins with the first pulse and the capturing continues during the second pulse window which is the

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main pulse for the flip-flop. In this way, internal and output nodes change their state faster than conventional flip-flops, and therefore, data to output latency decreases. This idea was applied to simple static flip-flop structures. Fig. 1 shows two proposed static pulsed flip-flops. They have the same pulse generator circuit that consists of three inverters generating delayed inverted clock signal *CLKB*, and a *NAND* gate along with another inverter for pulse generation. Clock input and its delayed signal *CLKB* are applied to a logically *AND* circuit and therefore a narrow sampling window is generated, as shown in Fig. 2. The *NAND* gate generates an active-low narrow pulse which is used for pre-capturing data input before the real transparency window is generated by the following inverter. The *PULSNOT* and *PULS* signals are used for pre-capturing and final capturing, respectively. In Fig. 1(a) the *PULS* signal applied to the NMOS transistor *MN1* creates a narrow sampling period in which data inputs can affect and change flip-flop state. *PULSNOT* signal arrives before *PULS* signal and data input capturing is started through PMOS transistors *MP6* and *MP7*. Change of the state of static nodes *SB* and *S* is initiated by data inputs *D* and *DB* during *PULSNOT* and continues via NMOS transistors *MN2* and *MN3* during the pulse window in which *MN1* is ON. The PMOS transistor *MP5 (MP4)* pulls *S (SB)* node up to *Vdd*. By proper sizing of NMOS and PMOS transistors of output inverters and *MN2-MP5*, the proposed flip-flop shows equal low-to-high and high-to-low output delays similar to SAFF and CCFF.

In Fig. 1(b), another pre-capturing static pulsed flip-flop is proposed. The pre-capturing transistors are *MP6* and *MP7* again and pass transistors *MN2* and *MN3* continue capturing during pulse window of *PULS* signal. Since data inputs have direct access through *MN2* and *MN3* to static nodes *SB* and *S*, this structure shows smaller delay than the former one. In order to distinguish between the two proposed flip-flops, the first flip-flop (Fig. 1(a)) is named as Dual Capturing Static Pulsed Flip-Flop (DCSPFF) and the second one (Fig. 1(b)) is named as Pre-Capturing Static Pulsed Flip-Flop (PCSPFF). The node staying at zero voltage (*SB* or *S*) could get floated when the pulse is finished and this could result in short-circuit current on the following inverter or even functional failure. Using two weak NMOS transistors, *MN8* and *MN9*, the nodes *SB* and *S* will not be floated at anytime. In these structures, generated pulse has a little latency relative to clock rising edge. This property provides negative setup time for proposed flip-flops. A narrow sampling period can also be obtained by applying clock input and its delayed signal *CLKB* to two series NMOS transistor, but in this manner the delay of flip-flops increases due to larger stack of transistors in the evaluation path. The pulse generator can be shared among a group of flip-flops to reduce the power and area overhead of pulse generation. Fig. 3 shows simulated waveforms of the proposed PCSPFF. The timing width of the generated pulse is 180ps in a 0.18µm technology.

IV. DOUBLE-EDGE TRIGGERING

Double-edge triggered flip-flops can latch the input data at both rising and falling edges of the clock. Thus, lower clock frequency is used while the data throughput is preserved. Since the proposed pre-capturing flip-flops are pulsed flip-flops, a dual pulse clock generator that generates pulses at both rising and falling edges of clock can be used to make them dual-edge triggered flip-flops. Fig. 4 shows such a dual pulse generator, which is used for both proposed static pulsed flip-flops. The dual edge triggering version of the first flip-flop is named as Double-edge triggered Dual-Capturing Static Pulsed Flip-Flop (DDCSPFF) and the second one is named as Double-edge triggered Pre-Capturing Static Pulsed Flip-Flop (DPCSPFF). As shown in Fig. 5 the dual pulse generator generates two inverse pulse signals at both rising and falling edges of the clock.

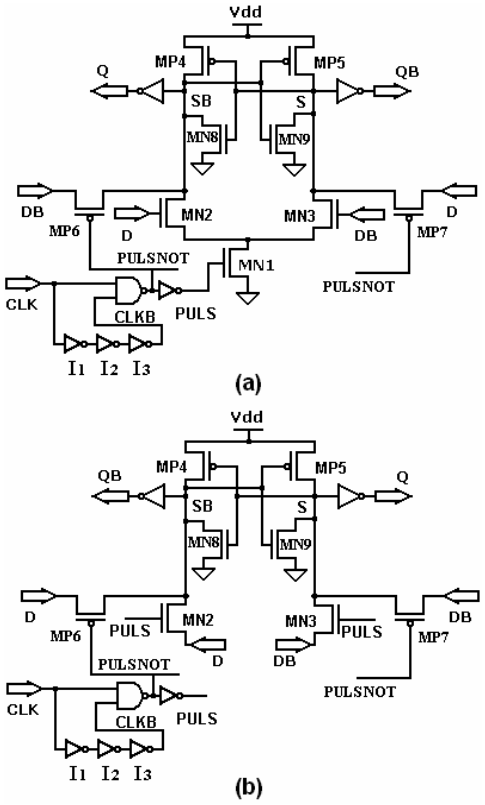

Fig. 1. Proposed static pulsed flip-flops: (a) Dual Capturing Static Pulsed Flip-Flop (DCSPFF) (b) Pre-Capturing Static Pulsed Flip-Flop (PCSPFF).

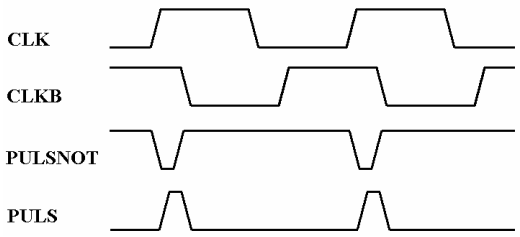

Fig. 2. Pulsed clock generation for proposed flip-flops.

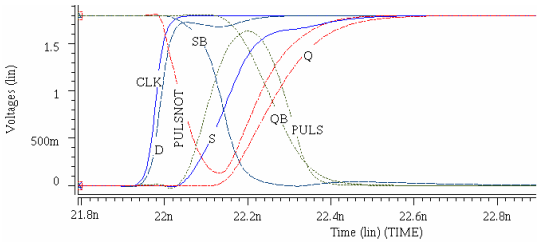

Fig. 3. Simulated waveforms of proposed flip-flops.

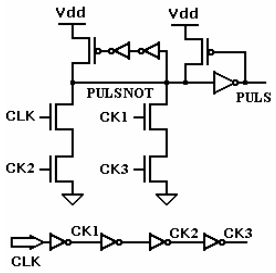

Fig.4. Dual pulse clock generator.

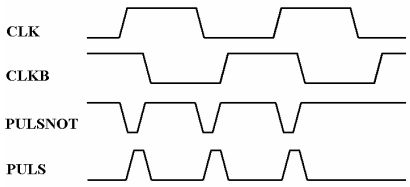

Fig. 5. Dual pulse clock generation for proposed flip-flops.

V. SIMULATION RESULTS AND COMPARISON

All the flip-flops were designed using the Berkeley Predictive Technology Model [8] of a 0.18µm process technology with a supply voltage of 1.8V. The designs were optimized for a clock frequency of 400MHz. A load capacitance of 200fF was used for all outputs. Transistor sizing was optimized using an iterative procedure with the objective of achieving high speed and low power (minimum Power-Delay Product (PDP)) for all high-performance flip-flops.

Table I summarizes the numerical results for all the high-performance flip-flops and the proposed designs. All the proposed static pulsed flip-flops show smaller data to output delay and power consumption in comparison to conventional high-performance flip-flops. The DPCSPFF has the smallest D-Q delay. All Proposed designs show symmetric output transitions similar to CCFF and SAFF. Moreover the negative setup time of proposed designs provides soft-clock edge for overcoming clock skew-related cycle time loss. Therefore, the proposed flip-flops present

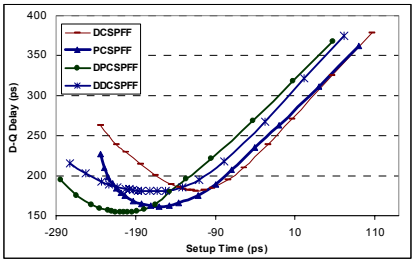

Fig. 6. Data-to-output delay vs. setup time for proposed flip-flops.

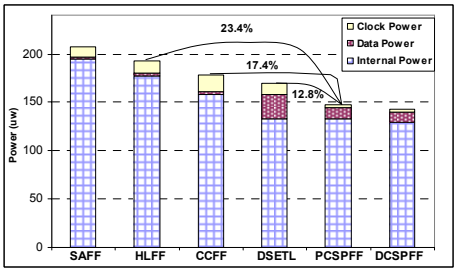

Fig. 7. Detailed power consumption of different flip-flops.

proper timing characteristics for high-performance applications. Power consumption of the proposed flip-flops is also lower than conventional flip-flops and therefore resulting in smaller PDP. In comparison to CCFF which shows the smallest PDP among conventional flip-flops, the PDP reduction of DPCSPFF, PCSPFF, DDCSPFF and DCSPFF are 26.1%, 29%, 13.6%, and 22.1%, respectively. As compared to HLFF, these improvements are 37.2%, 39.7%, 26.5%, and 33.7% respectively. Therefore, the proposed static pulsed flip-flops are right design options for low-power and high-performance applications. Fig. 6 shows data-to-output (D-Q) delay vs. setup time for the proposed flip-flops. The proposed static pulsed flip-flops show more negative setup time than conventional high-performance flip-flops.

Power contribution of three main sources of power dissipation including internal power dissipation, local clock power dissipation and local data power dissipation was measured for 0.5 data switching activity. As shown in Fig. 7, the DCSPFF and PCSPFF present the lowest local clock power dissipation while CCFF consumes large amount of clock power due to its high clock loads. The proposed static pulsed flip-flops show low data power consumption while DSETL dissipates highest local data power since it uses large pass transistors on data inputs. Total power consumption of PCSPFF and DCSPFF are 17.4% and 20% lower than that of CCFF, respectively. These values are 23.4% and 25.7% for comparison with HLFF; and 12.8% and 15.5% for comparison with DSETL, respectively. Proposed pulse generation circuits present significant power saving in clock distribution network. As shown in Fig. 8, PCSPFF and DCSPFF present 83.3% and 76.1% power savings in clock network in comparison to CCFF and HLFF, respectively. DPCSPFF and DDCSPFF present 94.4% and 92.0% power savings in clock network in comparison to CCFF and HLFF, respectively. This improvement is largely due to 50% reduction in clock frequency by using dual-edge triggering feature.

Fig. 9 shows power as a function of data switching activity for different flip-flops. The proposed single edge-triggered static pulsed flip-flops, PCSPFF and DCSPFF, have the lowest power consumption at all switching activities among all flip-flops. That is because they have a static nature of operation. DSETL is also static, and therefore similar to PCSPFF and DCSPFF, it consumes less power in comparison to other conventional high performance flip-flops, but unlike the proposed designs, its power dissipation increases significantly at higher data switching activities due to its large pass transistors. CCFF shows low power consumption at low data switching activities but like DSETL its power consumption increases significantly with increasing data switching activity.

A less power consuming implementation of proposed flip-flops at different data switching activities can be obtained in implementing an 8-bit counter. An 8-bit counter presents different switching activities from low values up to unity. Fig. 10 shows power consumption of a counter implemented using different flip-flops. As shown in Fig. 10(a), the proposed static pulsed flip-flops again show the lowest power consumption while SAFF shows the highest power consumption because of its high power dissipation at all data switching activities. PCSPFF shows 50.3%, 32.1% and 20.6% power reduction in comparison to HLFF, CCFF and DSETL, respectively. The power reduction values are 42.6%, 20.0% and 6.5% for DCSPFF in comparison to HLFF, CCFF and DSETL, respectively. These improvements can be further increased by sharing the pulse generator among the group of flip-flops to reduce the power overhead of pulse generation. In Fig. 10(b), the pulse generator is shared among four flip-flops for DPCSPFF and DDCSPFF. In this case, DPCSPFF shows 68.5%,

56.2% and 48.8% power reduction in comparison to HLFF, CCFF and DSETL, respectively. These power reduction values are 50.5%, 31.1% and 19.5% for DDCSPFF in comparison to HLFF, CCFF and DSETL, respectively. In terms of area, the area of PCSPFF is the smallest among all the high-performance flip-flops (see total width in Table 1). The area of DCSPFF is as low as that of DSETL.

VI. CONCLOUSIONS

Two pre-capturing static pulsed flip-flops are proposed for low-power and high-performance applications. Double-edge triggering can also be incorporated into the proposed flip-flops for significant clock power reduction. Extensive power, delay, and area comparisons between the proposed static pulsed flip-flops and conventional high-performance flip-flops show advantages of the proposed flip-flops in terms of both delay and power. Pulse generation circuits incorporated in the proposed designs show significant power saving on clock networks. The negative setup time, short data to output delay, and low power consumption of the proposed static pulsed flip-flops at all switching activities suggest extensive using of these flip-flops for high-speed and low-power applications.

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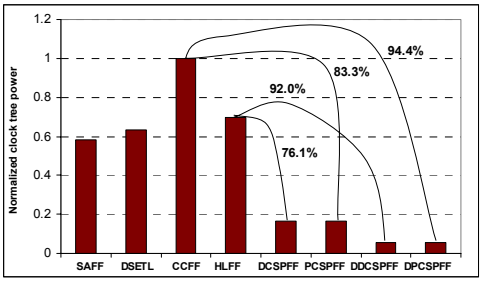


Fig. 8. Normalized clock network power comparisons.

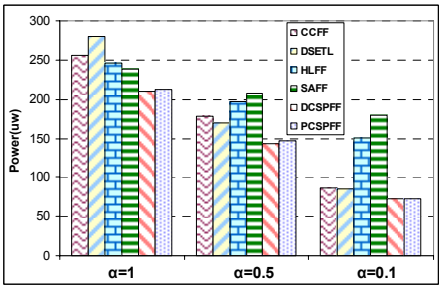
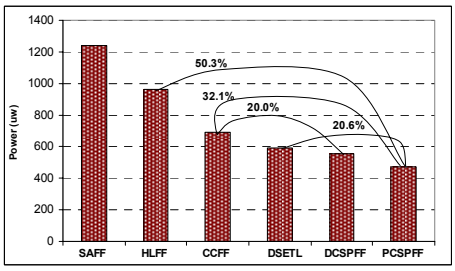
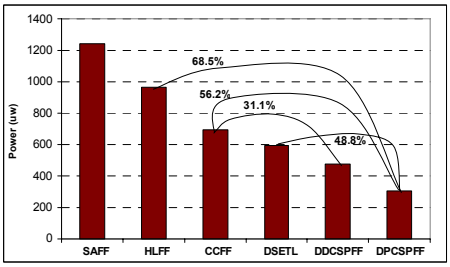


Fig. 9. Power vs. data switching activity at 400MHz



(a)



(b)

Fig. 10. Comparison of power consumption of counters: (a) PCSPFF and DCSPFF (b) DPCSPFF and DDCSPFF with pulse generator sharing along with other flip-flops.

TABLE I
NUMERICAL RESULTS AT DATA SWITCHING ACTIVITY OF 0.5 AND 400MHz CLOCK FREQUENCY

Flip-Flop	D-Q Delay (pS)	Setup time (pS)	Hold time (pS)	Power (μW)	PDP (fJ)	Norm. PDP	Device count	Total Width (μm)
CCFF	189.6	-24.5	85.0	178.6	33.86	0.846	35	57.2
SAFF	193.3	-15.8	53.0	207.0	40.01	1.000	26	46.9
HLFF	200.5	-35.5	109.0	192.6	39.81	0.995	20	46.0
DSETL	209.6	-50.6	181.0	169.2	35.46	0.886	18	40.9
DCSPFF	184.5	-114.8	278.0	143.0	26.38	0.659	25	41.0
PCSPFF	162.8	-160.3	260.0	147.5	24.01	0.600	24	38.5
DDCSPFF	183.9	-181.8	321.0	159.1	29.26	0.731	33	44.6
DPCSPFF	155.0	-198.5	303.0	161.3	25.00	0.625	32	42.1