Design of High Performance Sense Amplifier Using Independent Gate Control in sub-50nm Double-Gate MOSFET

Saibal Mukhopadhyay, Hamid Mahmoodi, and Kaushik Roy
Dept. of ECE, Purdue University, West Lafayette, IN-47907
<sm, mahmoodi, kaushik>@ecn.purdue.edu

Abstract

Double-Gate (DG) transistor has emerged as the most promising device for nano-scale circuit design. Independent control of front and back gate in DG devices can be effectively used to improve performance and reduce power in sub-50nm circuits. In this paper, we propose a high-performance sense-amplifier design using independent gate control in symmetric and asymmetric DG devices. The proposed design reduces the sensing delay of the sense amplifier by 30-35% and dynamic power by 10% (at 6GHz) from the connected gate design.

1. Introduction

Double-Gate MOSFET (DG) devices are known to be the most scalable silicon transistors due to the excellent control of the short-channel effects in the double-gate structure [1-2]. Low subthreshold leakage and higher ON current in DG devices make them very suitable for circuit design in sub-50nm regime [1-2]. There are different structures possible for DG devices (Fig. 1), namely (a) symmetric device with same gate material (e.g. near-midgap metals) and oxide thickness for the front and back gate (*SymDG*) [3-4] (b) asymmetric device with different front and back oxide thickness (*AsymOxDG*) [5] and (c) asymmetric device with materials of different workfunction (e.g. n+ poly and p+ poly) in the front and the back gate (*AsymWfDG*) [4].

A circuit designed in single gate technology (e.g. bulk-CMOS) can be directly translated into the DG technology by replacing each transistor with a connected gate DGMOS (*ConnGateDG*), where the front and the back gates are tied together. However, the *Directly Translated* circuit (*DirTrans*) style does not utilize possibility of independent control (*IndGateDG*) of front and back gates [6-7]. The fabrication of both *ConnGateDG* and *IndGateDG* on the same process has been recently reported [7]. Independent control of the front and the back gate is very attractive for circuit design. In [8-10], authors have demonstrated the use of independent gate control in designing efficient circuits (hereafter referred to as *IndGateControl* circuits). In this paper, we propose a novel Latch Based voltage mode Sense Amplifier (LBSA) [11-12] circuit, based on the independent gate control of DGMOS. Designing high-performance sense amplifiers are extremely important for enhancing the performance of SRAM [12]. In this work, in particular:

- We propose a novel LBSA circuit using independent gate control in DG devices. The proposed circuit is first realized using *SymDG* devices which results in a 30-35% improvement in sensing delay.
- We demonstrate the use of asymmetric DG (*AsymDG*) devices to reduce the power dissipation of the proposed *IndGateControl* deign. We have also proposed a circuit technique using the *SymDG* devices to reduce the power dissipation in the proposed design (a 10% reduction in dynamic power from the *DirTrans* design was observed).

The proposed LBSA successfully demonstrates the advantage of using independent gate control in DG devices for efficient circuit design in sub-50nm regime.

2. Device Characteristics

The symmetric and asymmetric devices (both *AsymOxDG* and *AsymWfDG*) with 50nm gate length (L_{gate}=50nm, L_{eff}=35nm, T_{oxF}=T_{oxB}=2.5nm, T_{si}=10nm) are designed in the device simulator MEDICI [13] (Fig. 2). MEDICI is used to perform device and circuit simulations. The quantum correction models were included in the simulation.

In the *AsymOxDG* device, workfunctions of the two gates are same (Φ_{MF}=Φ_{MB}), but the back gate is thicker than the front gate (T_{oxB}>T_{oxF}) [5]. On the other hand, in the *AsymWfDG* device the workfunction of two gates are different ($\Delta\Phi_{MBF}$=Φ_{MB}-Φ_{MF}) but T_{oxB}=T_{oxF} [4]. Increasing T_{oxB}/T_{oxF} in *AsymOxDG* and $\Delta\Phi_{MBF}$ in *AsymWfDG* increases the asymmetry between the two gates.

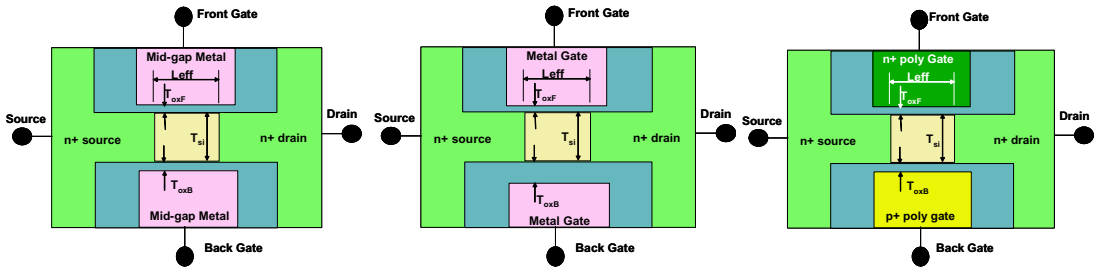

Fig.1: Structures of Double-Gate devices. (a) Symmetric device with near mid-gap metal gates (*SymDG*), (b) Asymmetric device with different front and back oxide thickness (*AsymOxDG*) and (b) Asymmetric device with front and back gate materials of different workfunctions (eg. n+ poly/p+ poly) (*AsymWfDG*) (L_{eff}=physical gate lenegth, L_{gate}=drawn gate length, T_{si}=silicon thickness, T_{oxF}=front oxide thickness, T_{oxB}= back oxide thickness).

Proceedings of the Sixth International Symposium on Quality Electronic Design (ISQED'05)
0-7695-2301-3/05 $ 20.00 IEEE

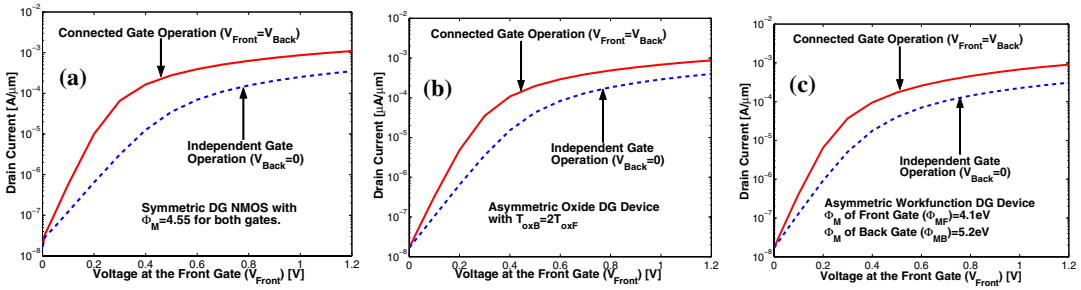

Fig. 2: Id-Vgs characteristics of the (a) *SymDG*, (b) *AsymOxDG*, and (c) *AsymWfDG* devices (with equal I_{OFF}).

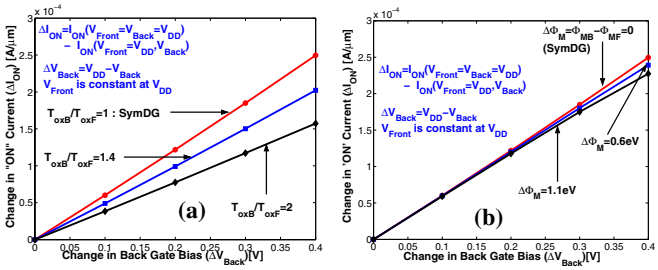

Fig. 3: Change in the "ON" current with back gate bias (a) *AsymOxDG* and (b) *AsymWfDG*.

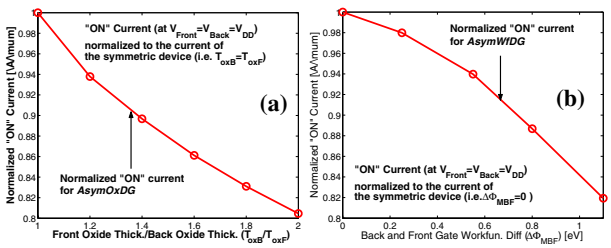

Fig. 4: Variation of "ON" current with asymmetry (a) *AsymOxDG* and (b) *AsymWfDG* devices. I_{OFF} was kept same for different values of T_{oxB}/T_{oxF} and $\Delta\Phi_{MBF}$.

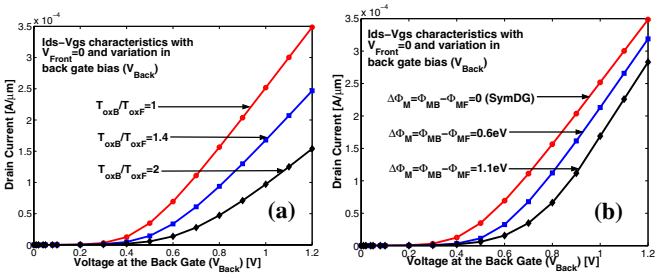

Fig. 5: Drain current with back gate bias (V_{Front}=0V) for (a) *AsymOxDG* and (b) *AsymWfDG* devices.

The long-channel threshold voltage at the front gate of a DGMOS is given by [14]:

$$V_{tF} = \Delta\Phi_{MF} + 2\phi_F + \left(\frac{C_{si}C_{oxB}}{C_{oxF}\left(C_{si}+C_{oxB}\right)}\right)\left[2\phi_F + \Delta\Phi_{MB} - V_{Back}\right] \quad (1)$$

From (1), it can be observed that increasing the back gate voltage in an *IndGateDG* reduces its threshold voltage, thereby increasing its "ON" current (I_{ON}). The sensitivity of V_{tF} (hence, I_{ON}) to the back gate bias depends on T_{oxF}, T_{oxB} and T_{si} as given by [14]:

$$\gamma_F = \frac{\partial V_{tF}}{\partial V_{GB}} = \frac{C_{si}C_{oxB}}{C_{oxF}\left(C_{si}+C_{oxB}\right)} = \frac{3T_{oxF}}{3T_{oxB}+T_{Si}} \quad (2)$$

It should also be noted that in case of *AsymOxDG* the capacitance in the back gate is less compared to the front gate (T_{oxB}>T_{oxF} => C_{oxF}>C_{oxB}). On the other hand, for *AsymWfDG* the Vt of the back gate is much higher than that of the front gate. This is because:

$$\Delta\Phi_{MB} > \Delta\Phi_{MF} \Rightarrow \left(\Delta\Phi_{MB}+\gamma_F\Delta\Phi_{MF}\right) > \left(\Delta\Phi_{MF}+\gamma_F\Delta\Phi_{MB}\right)\left[\because \gamma<1\right] \quad (3)$$
$$\Rightarrow V_{tB} > V_{tF} \quad ; for\ T_{oxF} = T_{oxB}$$

Using the above discussion, let us analyze the effect of V_{Back} on the drain current under the conditions V_{Front}=V_{DD} and V_{Front}=0 for *SymDG*, *AsymOxDG* and *AsymWfDG* devices. These two scenarios are important in analyzing the delay and power of the proposed *IndGateControl* LBSA, respectively.

With V_{Front}=V_{DD}, reduction of V_{Back} from V_{DD} reduces I_{ON} (say by ΔI_{ON}) of the transistor as shown in Fig. 3 [6-7]. This analysis represents the current difference between two identical transistors, both with front gate at V_{DD} but with different back gate bias. The value of ΔI_{ON} at a particular ΔV_{Back} is maximum for symmetric devices. In case of *AsymOxDG*, increasing T_{oxB} reduces the sensitivity of the Vt to the variation in back gate bias (γ_F reduces) (see (2)). Hence, ΔI_{ON} produced at a particular ΔV_{Back}, reduces with an increase in T_{oxB} (Fig. 3(a)). However, for *AsymWfDG* increasing $\Delta\Phi_{MFB}$ does not reduce the sensitivity of the V_{tF} to V_{Back}. Hence, ΔI_{ON} (at a certain ΔV_{Back}) is a weak function $\Delta\Phi_{MFB}$ (Fig. 3(b)). Moreover, increasing the asymmetry also reduces the "ON" current (at V_{Front}= V_{DD} & V_{Back}=V_{DD}) through the transistor (Fig. 4).

The drain current at (V_{Front}=0 & V_{Back}=V_{DD}) is significantly less compared to the current at V_{Back} =V_{Front}=V_{DD} (Fig. 5). In *AsymOxDG*, increasing T_{oxB} increases *Vt* of the back gate and reduces C_{oxB}. Similarly, in *AsymWfDG* increasing $\Delta\Phi_{MBF}$ (by increasing Φ_{MB} and reducing Φ_{MF}), increases *Vt* of the back gate. Hence, current at (V_{Front}=0 & V_{Back}=V_{DD}) reduces considerably with an increase in the asymmetry (i.e. with T_{oxB}/T_{oxF} and $\Delta\Phi_{MBF}$).

3. Latch Based Sense Amplifiers (LBSA)

3.1. Operation of Directly Translated LBSA

Let us first consider the Directly Translated (*DirTrans*) implementation of the LBSA [11-12] with the *ConnGateDG* device (Fig. 6(a)). In the pre-charge mode (SE is low) O1 and O2 are pre-charged to V_{DD} through PC1 and PC2. After the word-line of an SRAM cell attached to the bit-lines BL and BLB is raised high, one of the bit-lines (say BL) is discharged and the other one stays high (say BLB). After the difference between BL and BLB (bit-differential) reaches a pre-specified value ΔMIN (usually 10% of V_{DD}), the sense amplifier is

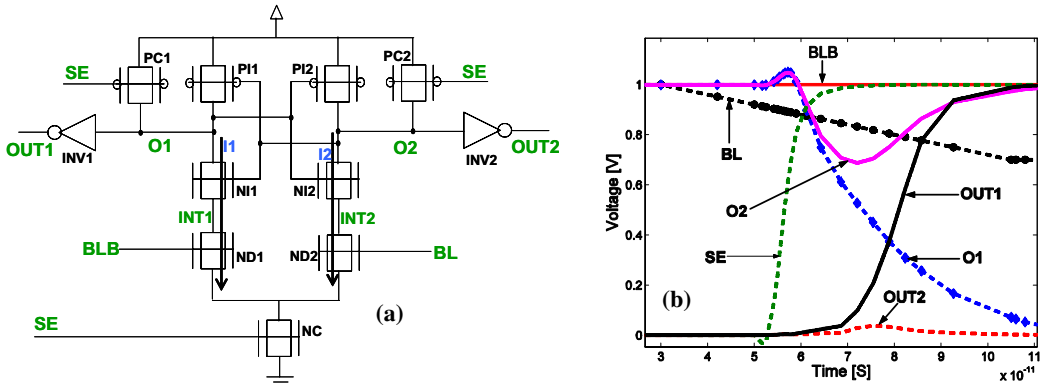

Fig. 6: *Directly Translated* LBSA circuit (a) circuit schematic and (b) waveform of operation.

enabled by raising SE high. This causes both O1 and O2 to discharge from V_{DD} (Fig. 6(b)). However, as V_{BL}= V_{BLB} - ΔMIN, the strength of ND2 is lower than that of ND1 (i.e. I1 > I2). Hence, O1 discharges at a faster rate than O2. In other words, the input voltage difference between V_{BL} and V_{BLB} produces a difference between the currents through ND1 and ND2 (ΔI=I1-I2). After a small difference is built up between the voltages of O1 and O2 (say ΔV_o), due to the cross coupled inverter action O1 reduces to '0' and O2 switches back to '1'(Fig. 6(b)). The sensing delay of the sense-amplifier is defined as the difference between the time SE is turned on (i.e. SE=0.5V_{DD}) to the time O1 (i.e. the node that is finally discharged) is reduced to 0.5V_{DD} [12]. Hence, the sensing delay can be reduced by: (a) increasing the currents through the pull-down path resulting in faster discharge of O1 and O2, (b) increasing ΔI produced by the application of ΔMIN and (c) increasing the gain of the cross-coupled inverters resulting in a faster amplification of ΔV_o to V_{DD}.

3.2. Operation of Independent Gate Control LBSA

Fig. 7 shows the proposed *IndGateControl* LBSA circuit using *SymDG* devices. Using the independent gate operation of DGMOS, the current difference in the two pull-down paths is achieved by using a single DGMOS in each path (N1 instead of NI1 & ND1 and N2 instead of NI2 & ND2) (Fig. 6). The front gates of N1 and N2 are connected in the cross-coupled inverter configuration whereas BLB and BL are connected to the back gates (Fig. 7). When SE is turned "on" front gates of N1 and N2 are at V_{DD} but the back gates are at different voltages (V_{BL} and V_{BLB}). This results in a current difference between the two paths (Fig. 3) which ensures the sensing operation. It can be observed that the proposed *IndGateControl* design principally operates as a dynamic threshold (V_{th}) circuit, where the threshold voltage of N1 and

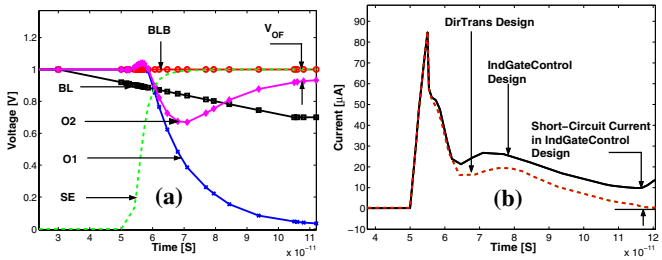

Fig. 8: Operation of the *IndGateControl* LBSA with short-circuit current. (a) voltage waveform and (b) dynamic current waveform.

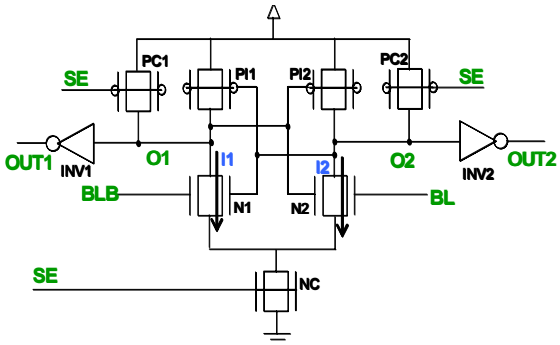

Fig. 7: *Independent Gate Control* LBSA

N2 are dynamically controlled by BL and BLB.

3.3. Advantages of the *IndGateControl* LBSA

In the *IndGateControl* LBSA, O1 and O2 are discharged through 2-Transistor stack (instead of 3-Transistor stack in *DirTrans* design). Reducing the number of transistors in the stack (i.e. stack height) has three impacts, namely, (a) increase in the discharging current (b) increase in ΔI produced by the application of ΔMIN and (c) increase in the gain of the cross-coupled inverters. Hence, the sensing delay in the *IndGateControl* is considerably less than that in the *DirTrans* design. Also, in the proposed *IndGateControl* design, nodes O1 and O2 drive only the front gates of N1 and N2 instead of the front and back gates of NI1 and NI2 as in the *DirTrans* design. This reduces the capacitive load on O1 and O2, thereby increasing the speed and reducing the switching power. It is also evident that, the proposed *IndGateControl* LBSA has less number of transistors (NI1 and NI2 are eliminated).

Moreover, a voltage mismatch (in the worst-case direction)

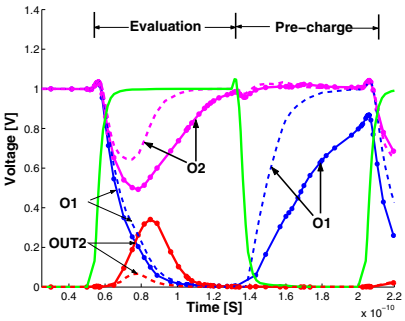

Fig. 9: Merging of pre-charge and pull-up PMOS transistors. Solid lines => merged and doted lines => non-merged.

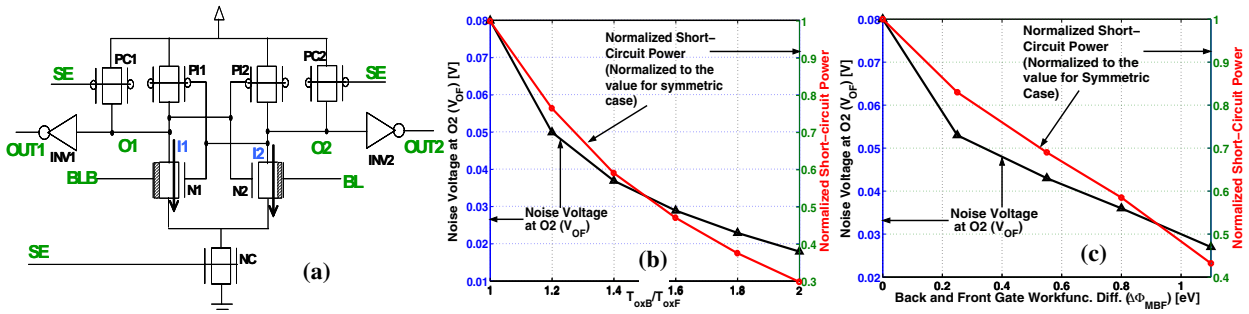

Fig. 10: Output noise voltage and short-circuit power reduction by using asymmetric device: (a) circuit schematic with asymmetric N1 and N2, (b) Asymmetric Oxide thickness and (b) Asymmetric Workfunction difference.

between nodes INT1 and INT2 in the *DirTrans* design (before the start of the sensing operation) increases the sensing delay and may result in an incorrect operation. Such a mismatch can be caused by coupling of noise and/or change in the strength of ND1 and ND2 due to process variations. However, this condition does not occur in the proposed *IndGateControl* design as nodes INT1 and INT2 are eliminated. Thus, the proposed design increases the tolerance to noise and process variation.

3.4. Drawback of the *IndGateControl* LBSA

In the proposed *IndGateControl* LBSA, after the sensing operation, the back gate of N2 (which is connected to BL) is not completely off (as $V_{BL}>0$). Hence, N2 is not completely "off" ($V_{FGATE}=0$ and $V_{BGATE}=V_{BL}$) which results in a short circuit current through PI2, N2 and NC. The short circuit current increases the power dissipation and reduces the voltage at node O2 from V_{DD} (the voltage difference between O2 and V_{DD} is called the *Noise Voltage at O2*=V_{OF}) (Fig. 8).

The *IndGateControl* LBSA designed with *SymDG* device functions correctly with a 35% improvement in speed and a 10% (at 6 GHz) power overhead compared to the *DirTrans* design. The noise voltage at O2 is less than 10% of V_{DD}. However, the short-circuit current needs to be reduced to improve the design.

3.5. Merging of precharge and pull-up transistors

The pre-charge transistors and the PMOS pull-up transistors (i.e. PC1 & PI1, PC2 & PI2) in the *IndGateControl* LBSA can also be merged together. This results in the independent gate operation of the merged transistor. Merging reduces the load on the sense-amp enable driver and on the nodes O1 and O2, thereby improving the speed and the switching power. However, merging reduces the pre-charging speed as only back gate of the merged transistors is used for pre-charging (Fig. 9). Moreover, merging also reduces the strength of the PMOS pull-up transistors PI1 and PI2. A weaker pull-up PMOS enhances the initial voltage swing at node O2 (Fig. 9). This has two impacts, namely, (a) it increases the power dissipation of the sense amplifier, and (b) it results in a voltage swing at the output of the inverter INV2, thereby increasing power dissipation of INV2. Due to these reasons we have not used the merging of the pre-charge and PMOS pull-up transistors in the proposed design. This emphasizes that *selective* use of the *IndGateDG* devices is necessary to obtain maximum benefit from the double gate technology.

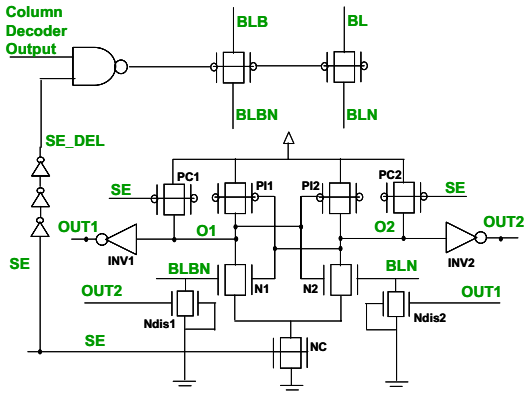

Fig. 11: Independent Gate LBSA with Short-Circuit Prevention Circuit (SCPC).

4. Reduction of Short-Circuit Current

In this section we explore different possibilities for reducing the short-circuit power in the *IndGateControl* LBSA circuit.

4.1. Use of *AsymDG* to reduce short-circuit current

The short-circuit power can be reduced by using *Asymmetric* devices for N1 and N2, and connecting the back gates to BLB and BL (Fig. 10(a)). In case of *AsymOxDG* as (Tox_B / Tox_F) increases, the current through N1 with $V_{FGATE}=0$ and $V_{BGATE}=V_{BL}$ reduces (Fig. 5(a)). A reduction in the short-circuit current reduces the short-circuit power and the *Noise Voltage at O2* (= V_{OF}) (Fig. 10(b)). However, increasing T_{oxB} reduces the current difference between N1 and N2 produced by the difference in back gate bias (Fig. 3(a)). It also reduces the discharging current for nodes O1 and O2 by reducing the ON current of the transistors N1 and N2 (Fig. 4(a)). Hence, the sensing delay increases with an increase in asymmetry (i.e. T_{oxB}). Similarly, the use of *AsymWfDG* devices also reduces the short-circuit power and noise voltage at O2 (Fig. 10(c)) at the cost of higher sensing delay.

4.2. Circuit technique to reduce short-circuit current

In order to eliminate the short circuit power in the *IndGateControl* LBSA, the voltage at the gate of N2 needs to be reduced to "0" after the sensing occurs. This can be achieved by adding NMOS Ndis1 and Ndis2 to the back gates of N1 and N2 (Fig. 11). The front gates of Ndis1 and Ndis2 are controlled by output of the inverters INV1 and INV2 (OUT1 & OUT2) and the back gates are connected to ground (to reduce the load on INV1 and INV2). This added circuit is called Short-Circuit Prevention Circuit (*SCPC*). When OUT1 & OUT2 are "0" (before the sensing) Ndis1 and Ndis2 are

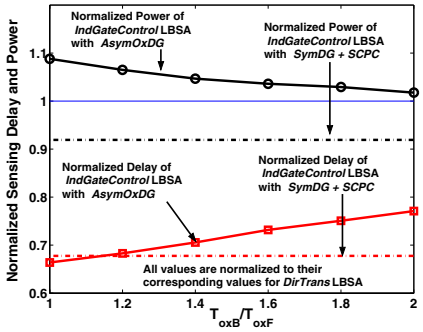

Fig. 12: Sensing delay and power of the *IndGateControl* LBSA with (*SymDG + SCPC*) and *AsymOxDG*.

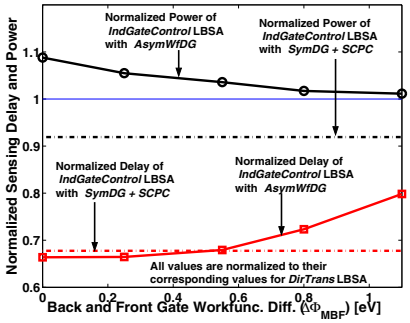

Fig. 13: Sensing delay and power of the *IndGateControl* LBSA with (*SymDG + SCPC*) and *AsymWfDG*.

"off". Hence, the gate voltages of N1 and N2 (i,e. BLBN and BLN) follow BLB and BL. After the sensing, OUT1 switches to "1", which turns on transistor Ndis2, thereby discharging node BLN. To prevent the discharging of the bit-lines (i.e. BL in this case), we modified the column decoder-multiplexer circuit to isolate the bit-lines after the sensing starts (Fig. 11). In this technique, the outputs of the column decoders are controlled by a delayed sense-amp signal (SE_DEL). When SE switches to high, the SE_DEL switches to low (after some delay), which turns "off" the PMOS pass transistors. This isolates the bit-lines BL and BLB from the nodes BLN and BLBN. It should be noted that, after the pass transistors are turned "off" BLBN becomes floated and in the worst case can be discharged to "0" by noise. However, even if BLBN gets discharged, node O1 is strongly held at "0" as the front gate of N1 is at "1" (i.e N1 is "*half* ON"). The proposed technique reduces the short-circuit power. However, it introduces a power overhead due to the control circuit. The delay and power of the inverters INV1 and INV2 also marginally increase as their output load increase due to the introduction of Ndis1 and Ndis2. The implementation of the control circuit will also increase the layout complexity and causes area overhead. However, the control circuit to isolate the bit-lines can be shared by a row of sense-amplifiers.

5. Results and Discussions

The *IndGateControl* LBSA circuit with the *SymDG* device and the *SCPC* results in a 33% reduction in the sensing delay and 10% (at 6GHz) reduction in the dynamic power compared to the *DirTrans* circuit (sizes of the different transistors in the two designs were kept same). Application of the *AsymOxDG* and *AsymWfDG* devices reduces the short-circuit power but increases the sensing delay (Fig. 12, 13). With *AsymOxDG* at (T_{oxB}/T_{oxF})=2 the delay improvement is reduced to 24% (negligible power overhead) (Fig. 12). With *AsymWfDG* at $\Delta\Phi_{MFB}$=1.1eV≈E_g, a negligible power overhead with a 20% delay reduction is observed (Fig. 13). Due to the reduction in the number of transistors in the pull-down path, the sensing delay in the *IndGateControl* LBSA has a lower sensitivity to supply voltage, temperature, and load capacitance at nodes O1 and O2 (Fig. 14). In this context we would like to point out that, through this work we have not tried to compare the effectiveness of two types of asymmetry. The different types of asymmetries have been introduced to illustrate their usage in designing independent gate circuits and to show that the proposed design can work with both.

The *IndGateControl* design has a lower sensitivity to the input bit-differential and mismatch in the load capacitances of nodes O1 and O2 compared to its *DirTrans* counterpart (Fig 15). Moreover, the sensing delay in the *IndGateControl* design is insensitive to the local drop in the supply voltage of the sense amplifier (Fig. 15) (i.e. supply of the sense amplifier is reduced whereas that of the bit-lines remains same). Such a local drop is possible as the supply line for the sense amplifier and that for the bit-line pre-charging circuit are spatially distant from each other. In the *DirTrans* design, drop in V_{DD} of the sense amplifier reduces discharging current by lowering the strength of NI1 and NI2 (in series with ND1 and ND2). However, in case of the *IndGateControl* design, only the strengths of the front gates of N1 and N2 are reduced. But the strength of the back gates remains the same as they are connected to the higher V_{DD} of the bit-lines. Thus the overall reduction in the discharging current is less. On the other hand, nodes O1 and O2 are pre-charged to a lower value. Hence, the sensing delay is much less sensitive to the drop in the supply voltage of the sense amplifier.

Variation in the T_{si} of a DG device modifies its ON current [15] (Fig. 16(a)). Moreover, sensitivity of the ON current to T_{si} variation is minimum in a symmetric device [15]. In *AsymWfDG* variation in T_{si} strongly modifies the threshold

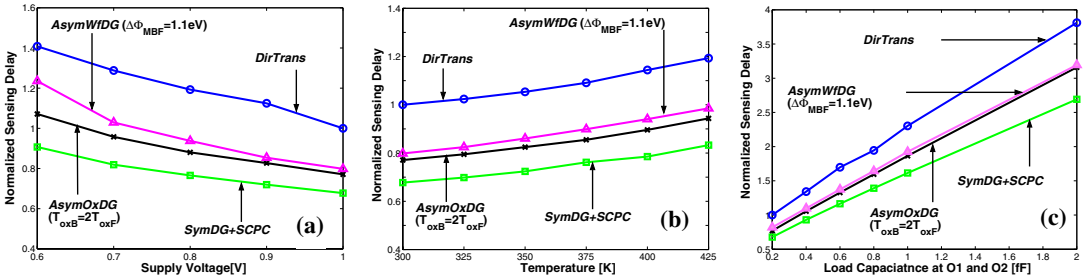

Fig.14: Variation of sensing delay with (a) supply oltage, (b) temperature, and (c) load capacitance. Delays are normalized to the delay of *DirTrans* design at (a) V_{DD}=1V, (b)T=300K and (c) load capacitance=0.2fF.

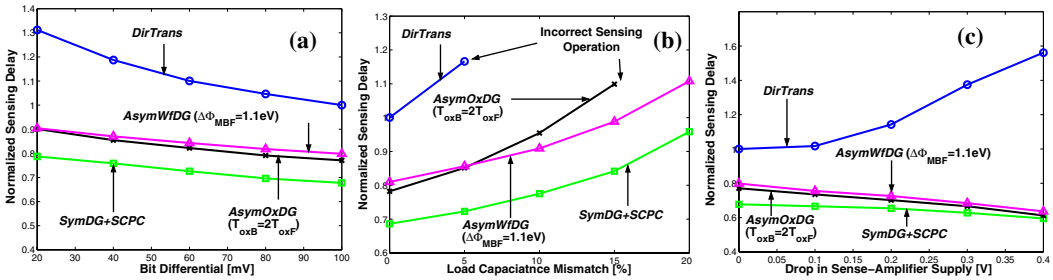

Fig.15: Variation of sensing delay of with (a) input bit-differential, (b) mismatch in load capacitance at O1 and O2 and (c) local drop in sense amplifier supply voltage. Delays are normalized to the delay of DirTrans design at (a) bit-differential =100mV, (b) load mismatch=0% and (c) local supply voltage drop=0V.

voltage resulting in a strong sensitivity of the "ON" current to T_{si} variation (Fig. 16(a)) [15]. If asymmetry is provided by increasing T_{oxB}, it can be observed from (1) that, the sensitivity of the long-channel Vt to the T_{si} variation reduces. However, increasing the T_{oxB} increases the short-channel effect thereby increasing the sensitivity of Vt and I_{ON} to T_{si} variation. For the device structure used in this work, we observed that the current in *AsymOxDG* device has a lower sensitivity to T_{si} than in the *AsymWfDG* (Fig. 16(a)). It is interesting to note that the variation of the current through a 2-T stack due to T_{si} variation is higher than a single transistor (Fig. 16(a)). This can be attributed to the variation in the voltage at the intermediate node. Application of the worst-case mismatch in the T_{si} between the pull-down NMOS transistors increases the sensing delay and may result in an incorrect sensing operation. For example, for the sensing operation described in Fig. 6, worst case occurs if T_{si} of N1 (NI1 and ND1 in *DirTrans* design) reduces (reducing its strength) while that of N2 (NI2 and ND2 in *DirTrans* design) increases (increasing its strength). This increases the sensing delay as I1 reduces (slower discharge of O1) while I2 increases (faster discharge of O2). Hence, the LBSA circuit which has a higher sensitivity of the sensing delay to the worst case mismatch is less robust. It is observed that use of *IndGateControl* design with SCPC or *AsymOxDG* improves the robustness of the sense amplifier compared to the *DirTrans* design (Fig. 16(b)). This is because of the elimination of the intermediate nodes INT1 and INT2 as explained in section 3.3. However, the strong sensitivity of the ON current in *AsymWfDG* to the T_{si} makes the *IndGateContro*l design with *AsymWfDG* more susceptible to the mismatch in silicon thickness. The susceptibility can be reduced by lowering the amount of asymmetry at the cost of increased short-circuit power.

6. Conclusions

In this paper we have proposed a novel design technique for latch based voltage mode sense amplifiers using symmetric and asymmetric DG devices in sub-50nm technology. The independent back gate control of the DG device in the pull-down path (other transistors are kept in the connected gate mode) is used to improve the performance and power in sense-amplifier circuits. The proposed design illustrates the fact that selective use of independent control of the front and the back gates in the DG devices is very effective in designing efficient circuits in nanometer regimes.

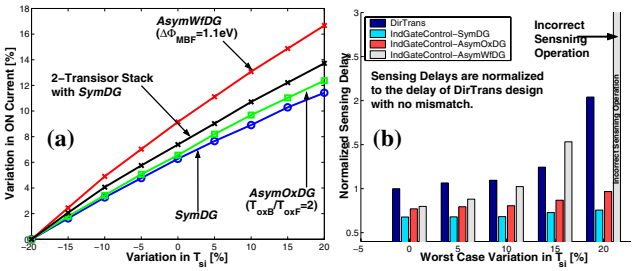

Fig. 16: Variation of (a) "ON" current in a device and (b) sensing delay of LBSA with worst case variation in T_{si}.

Acknowledgement

This work is supported in part by Semiconductor Research Corporation (contract # 1078.001), Intel and IBM corporations.

References

[1] H-S.P. Wong, et. al, "Device design considerations for double-gate, ground-plane, single-gated ultra-thin SOI MOSFET at the 25nm channel length generation", *in IEDM,* 1998, pp. 407-410

[2] E. Nowak, et. al, "Turning silicon on its edge", *IEEE Circuits & Device Magazine*, Jan/Feb 2004, pp. 20-31.

[3] J. Kedzierski, et. al., "High-performance symmetric-gate and CMOS-compatible asymmetric gate FinFET device", *IEDM*, 2001, pp. 437-440.

[4] J. Kedzierski, et. al., "Metal gate FinFET and fully depleted SOI devices using total gate silicidation", *IEDM*, 2002, pp. 247-250.

[5] L. Wei, et. al., "Vertically integrated SOI circuits for low-power and high-performance applications", IEEE Transactions on VLSI Systems, vol. 10, no. 3, June 2002, pp. 351 – 362

[6] D. Fried, et. al, "A Fin-type independent-double-gate NFET", Device Research Conference, 2003, pp. 45-46.

[7] L. Mathew, et. al, "CMOS vertical multiple independent gate field effect transistors (MIGFET)", IEEE Int. SOI Conference, 2004, pp. 187-188.

[8] H. Mahmoodi, et. al, "High-performance and low-power domino logic using independent gate control in Double-Gate SOI MOSFETs", IEEE Int. SOI Conference, 2004, pp. 67-68.

[9] A. Kumar, et. al, "Low voltage and performance tunable CMOS circuit design using independently driven Double-gate MOSFETs", IEEE Int. SOI Conference, 2004, pp. 119-120.

[10] T. Cakici, et. al, "A low power four transistor Schmitt Trigger for asymmetric double gate fully depleted SOI devices", IEEE Int. SOI Conference, 2003, pp. 21-22.

[11] T. Kobayashi, et. al, "A currentcontolled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits*, vol. 28, Apr., 1993, pp. 523–527.

[12] B. Wicht, et. al, "Yield and speed optimization of a latch type voltage sense amplifier", IEEE Journal of Solid-State Circuits, vol. 39, July, 2004, pp. 1148-1158.

[13] MEDICI: 2-D device simulation program, Synopsys Inc.

[14] R. Zhang, et. al, **"**Low-power high-performance double-gate fully depleted SOI circuit design"**,** IEEE Transactions on Electron Devices, vol. 49 May, 2002, pp.852 – 862.

[15] Q. Chen, et. al, "A comparative study of threshold variations in symmetric and asymmetric undoped double-gate MOSFETs", IEEE Int. SOI Conference, 2002, pp. 30 – 31.